CMOS Transconductance Multipliers: A Tutorial

Gunhee Han and Edgar Sánchez-Sinencio, *Fellow, IEEE*

***Abstract*—Real-time analog multiplication of two signals is one of the most important operations in analog signal processing. The multiplier is used not only as a computational building block but also as a programming element in systems such as filters, neural networks, and as mixers and modulators in a communication system. Although high performance bipolar junction transistor multipliers have been available for some time, the CMOS multiplier implementation is still a challenging subject especially for low-voltage and low-power circuit design. Despite the large number of papers proposing new MOS multiplier structures, they can be roughly grouped into a few categories. This tutorial provides a complete survey of CMOS multipliers, presents a unified generation of multiplier architectures, and proposes the most recommended MOS multiplier structure. This tutorial could serve as a starting reference point (and metric) for comparison of new CMOS multiplier circuit configurations. An illustrative CMOS chip prototype verifying theoretical results is presented.**

***Index Terms*—CMOS multipliers, low noise design, low voltage circuits, multipliers.**

I. Introduction

MULTIPLIERS perform linear products of two signals x and y yielding an output $z = Kxy$ where K is a multiplication constant with suitable dimension. Multipliers are often categorized as single-quadrant (x and y are unipolar), two-quadrant (where x or y can be bipolar), and four-quadrant multipliers (where both x and y can be bipolar). Noise and bandwidth are often not optimized for multipliers. Modulator and mixer are particular cases of multipliers that are designed with noise and frequency constraints. The history of the analog multipliers is originated from its use as a mixer and as an amplitude modulator which involves a multiplication of two signals. The basic idea of the multiplier implementation is illustrated in Fig. 1. Two signals, $v_1(t)$ and $v_2(t)$, are applied to a nonlinear device, which can be characterized by a high-order polynomial function. This polynomial function generates terms like $v_1^2(t)$, $v_2^2(t)$, $v_1^3(t)$, $v_2^3(t)$, $v_1^2(t)v_2(t)$ and many others besides the desired $v_1(t)v_2(t)$. Then it is required to cancel the undesired components. This is accomplished by a cancellation circuit configuration.

A multiplier could be realized using programmable transconductance components. Consider the conceptual transconductance amplifier of Fig. 2(a), where the output current

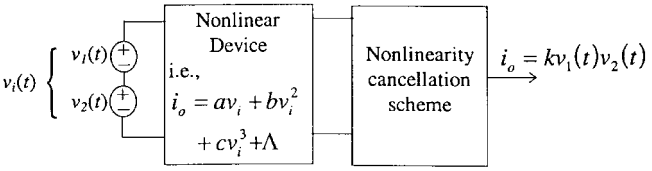

Fig. 1. Basic idea of multiplier.

is simply given by

$$i_o = G_{m1}v_1 \tag{1}$$

where

$$G_{m1} = G_{m1}(I_{\text{bias1}}). \tag{2a}$$

For a bipolar transconductor, G_{m1} becomes

$$G_{m1} = \frac{I_{\text{bias1}}}{2V_t} \tag{2b}$$

where V_t is the thermal voltage (kT/q).

Next, a small signal i_2 is added to the bias current as shown in Fig. 2(b). The second input signal $v_2(t)$ can be converted into a current, $i_2(t) = G_{m2}v_2(t)$, as illustrated in Fig. 2(c). Then, the output current yields

$$i_o(t) = G_{m1}v_1 = \frac{I_{\text{bias1}} + G_{m2}v_2(t)}{2V_t}v_1(t) \tag{3a}$$

$$\begin{aligned} i_o(t) &= \frac{G_{m2}v_1(t)v_2(t)}{2V_t} + \frac{I_{\text{bias1}}}{2V_t}v_1(t) \\ &= \frac{I_{\text{bias2}}v_1(t)v_2(t)}{2V_t 2V_t} + \frac{I_{\text{bias1}}v_1(t)}{2V_t} \end{aligned} \tag{3b}$$

or

$$i_o(t) = k_1v_1(t)v_2(t) + k_2v_1(t). \tag{3c}$$

Thus, $i_o(t)$ represents the multiplication of two signals $v_1(t)$ and $v_2(t)$ and an unwanted component $k_2v_1(t)$. This component can be eliminated as shown in Fig. 2(d). Better cancellation is achieved when the third transconductor (G_{m2}) becomes a fully differential transconductor, and v_1 and v_2 are fully differential inputs as illustrated in Fig. 2(e).

$$i_o(t) = 2k_1v_1(t)v_2(t). \tag{4}$$

This is the basic operation principle of a Gilbert cell [1], [2]. Operational transconductance amplifier (OTA)-based implementations are reported in [3]–[4]. The connection to the Gilbert cell can be seen by substituting the transconductors in Fig. 2(e) by bipolar junction transistor (BJT) differential pairs.

As the digital technology dominates in modern electronics, analog circuits are required to share the same standard CMOS

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G. Han is with the Department of Electronic Engineering, Yonsei University, Seoul, Korea.

E. Sánchez-Sincencio is with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843-3128 USA (e-mail: sanchez@ee.tamu.edu).

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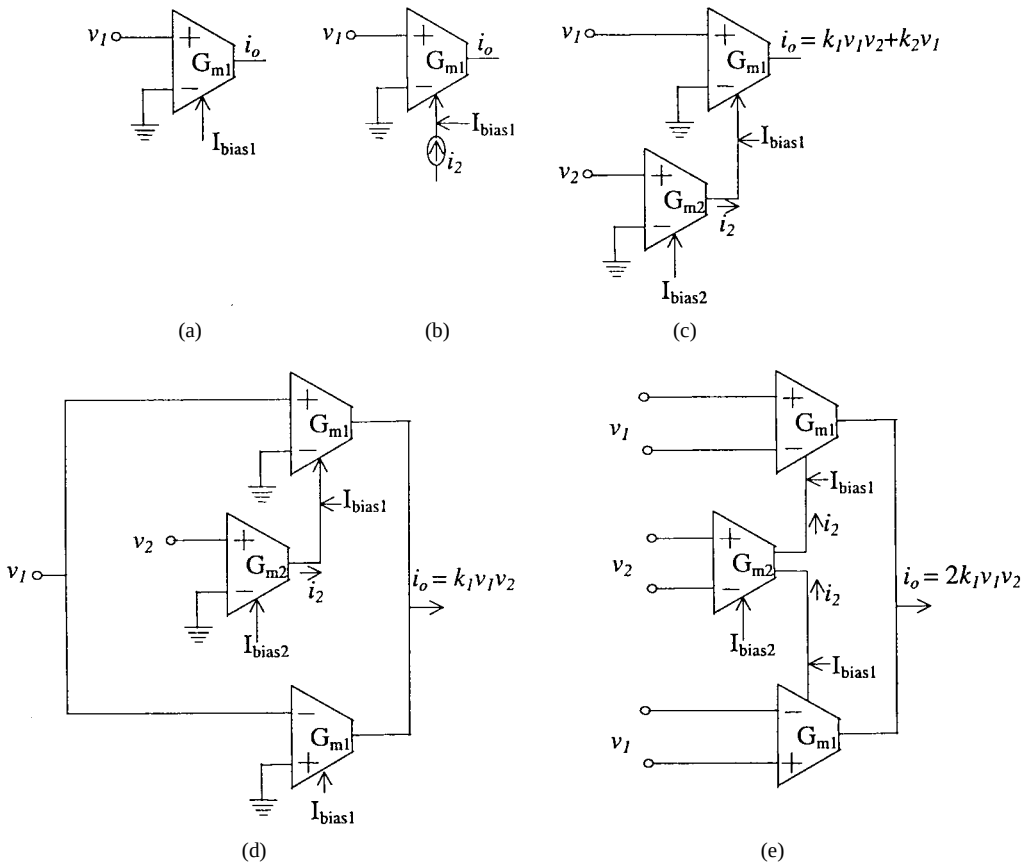


Fig. 2. Multiplication operation using programmable transconductor.

process for low-cost fabrication. Thus, the popular BJT Gilbert Cell is not suitable in a standard digital process, and designers must address low power supply voltage requirements. One problem that circuit designers often encounter is how to select the best multiplier architecture for their applications. Unfortunately, designers who propose multipliers in the literature often do not make reference to or comparison to other multipliers. This lack of comparison causes the same basic multiplier architectures to be, from time to time, reported as "new" architectures.

In this tutorial, we cluster transconductance multipliers into eight types. They can be categorized into two groups based on its MOS operating region, linear [5]–[21] and saturation [22]–[51]. It should be emphasized that the fundamental multiplier circuit topology for many of the multipliers is the same. Besides the above major multiplier structures, multipliers operating in the weak inversion region [52]–[54], dynamic multipliers for sampled signal system or neural networks [55]–[61], voltage–current, and current–current multipliers [62]–[64] have been reported.

In what follows, we attempt to classify a number of multiplier architectures according to different criteria, i.e., transistor region of operation, nonlinearity cancellation schemes, and signal injection method. Table I summarizes these results, more details are discussed next.

TABLE I
SUMMARY OF MULTIPLIER OPERATING MODES

Operating region	Input signal injection method	Active term	Cancellation method	Type	Comment
Linear	$\pm y$, $\pm x$, i_d	$V_{gs}V_{ds}$	single-quadrant	I	
	$\pm x \pm y$, i_d	V_{ds}^2	square device	II	Not practical
	i_d, $\pm x$, $\pm y$	$V_{gs}V_{ds}$	single-quadrant	III	Not practical
Saturation	$\pm x \pm y$, i_d	V_{gs}^2	square device	IV	Not practical
	i_d, $\pm x$, $\pm y$	V_{gs}^2	square device	V	
	i_d, $\pm x$, $\pm y$	V_{gb}^2	square device	VI	Not practical
	i_d, $\pm x \pm y$	V_{gs}^2	square device	VII	
	i_d, $\pm x$, $\pm y$	V_{gs}^2	Gilbert cell (single-quadrant)	VIII	

II. Operation Modes and Circuit Topologies

Despite many reported circuits, only two cancellation methods for the four-quadrant multiplication are known. Since a single-ended configuration cannot achieve complete cancellation of nonlinearity and has poor power supply rejection ratio (PSRR), a fully differential configuration is necessary in

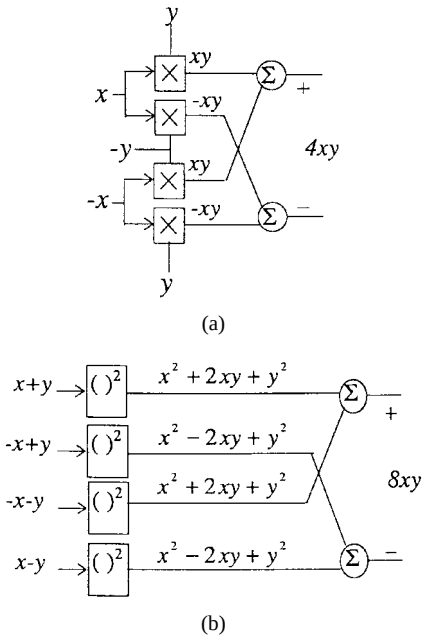


Fig. 3. Four-quadrant multiplier basic architectures. Common mode components X and Y are not shown in the figure for simplicity. (a) Using single-quadrant multipliers. (b) Using square devices.

a sound multiplier topology. The multiplier has two inputs, therefore there are four combinations of two differential signals, i.e., (x, y), $(-x, y)$, $(-x, -y)$, and $(x, -y)$. The topology of Fig. 3(a) is based on single-quadrant multipliers. Fig. 3(b) is based on square law devices. These topologies achieve multiplication and simultaneously cancel out all the higher order and common-mode components (X and Y) based on the following equalities:

$$[(X+x)(Y+y)+(X-x)(Y-y)] - [(X-x)(Y+y)+(X+x)(Y-y)] = 4xy \quad (5)$$

or

$$\lfloor\{(X+x)+(Y+y)\}^2+\{(X-x)+(Y-y)\}^2\rfloor - [\{(X-x)+(Y+y)\}^2+\{(X+x)+(Y-y)\}^2] = 8xy \quad (6)$$

respectively. Note that, throughout the paper, lower case letters, i.e., x, y, v_i, i_o, represent small signals.

MOS transistors can be used to implement these cancellation schemes and the fundamental operation is a transconductance multiplier because the MOS FET is a transconductance device. The simple MOS transistor model is expressed as

$$I_d = K\left[V_{\rm gs} - V_T - \frac{V_{\rm ds}}{2}\right]V_{\rm ds} = K\left[V_{\rm gs}V_{\rm ds} - V_T V_{\rm ds} - \frac{V_{\rm ds}^2}{2}\right], \quad \text{for } V_{\rm gs} > V_T,\ V_{\rm ds} < V_{\rm gs} - V_T \quad (7)$$

$$I_d = \frac{K}{2}[V_{\rm gs} - V_T]^2 = \frac{K}{2}\left[V_{\rm gs}^2 - 2V_{\rm gs}V_T - V_T^2\right], \quad \text{for } V_{\rm gs} > V_T,\ V_{\rm ds} > V_{\rm gs} - V_T \quad (8)$$

for N MOS FET in its linear and saturation regions, respectively. $K = \mu_o C_{ox}\frac{W}{L}$ and V_T are the conventional notation

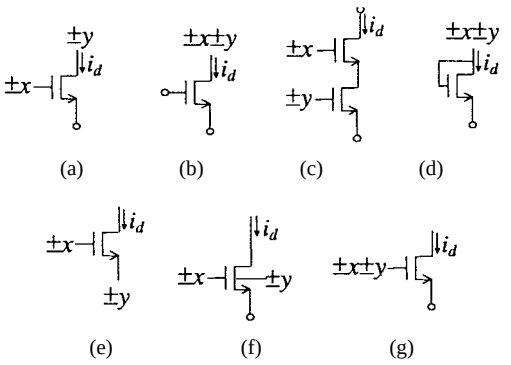


Fig. 4. Voltage signal injection methods.

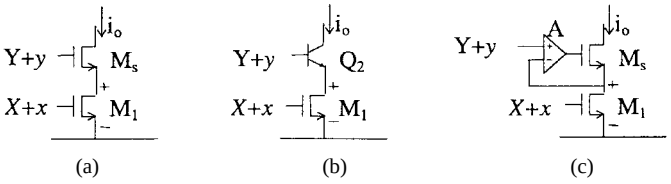


Fig. 5. Programmable transconductor.

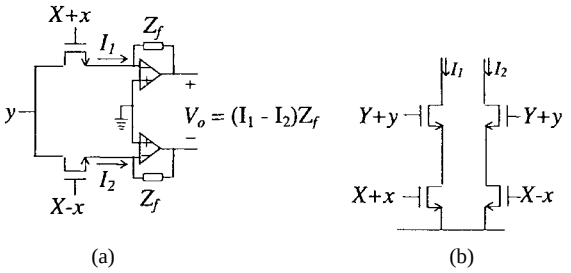


Fig. 6. Four-quadrant multipliers with two transistors operating in linear region.

[65] for the transconductance parameter and the threshold voltage of the MOS transistor, respectively. The terms $V_{\rm gs}V_{\rm ds}$ in (7), $V_{\rm ds}^2$ in (7), or $V_{\rm gs}^2$ in (8) can be used to implement (5) and (6), respectively. More details follow in Sections II.1 and II.2.

Fig. 4 shows the application methods for two signals (x and y) in a MOS FET (See Table I, column 2). The small circle on the transistor terminal represents a fixed biasing voltage. x and y are time-variable voltage signals, disregarding the bias. The first three methods are used for FET's operating in their linear region and the rest are for transistors operating in saturation. The signal injection methods (b), (d), and (g) in Fig. 4 require a voltage summing circuit. This voltage summation can be implemented in many different ways [66]–[67], although the performance of the summer directly affects the performance of multiplier. In this tutorial, it is assumed that these signals are available.

In the following subsection, multiplier topologies are categorized based on the signal injection method. All the multiplier types are summarized in Table I.

II.1. MOS Multipliers Operating in Linear Region

A. Using $V_{\rm gs}V_{\rm ds}$ (TYPE I)

First we introduce a programmable linear transconductor and show how it can be used to yield a multiplier. In Fig. 5

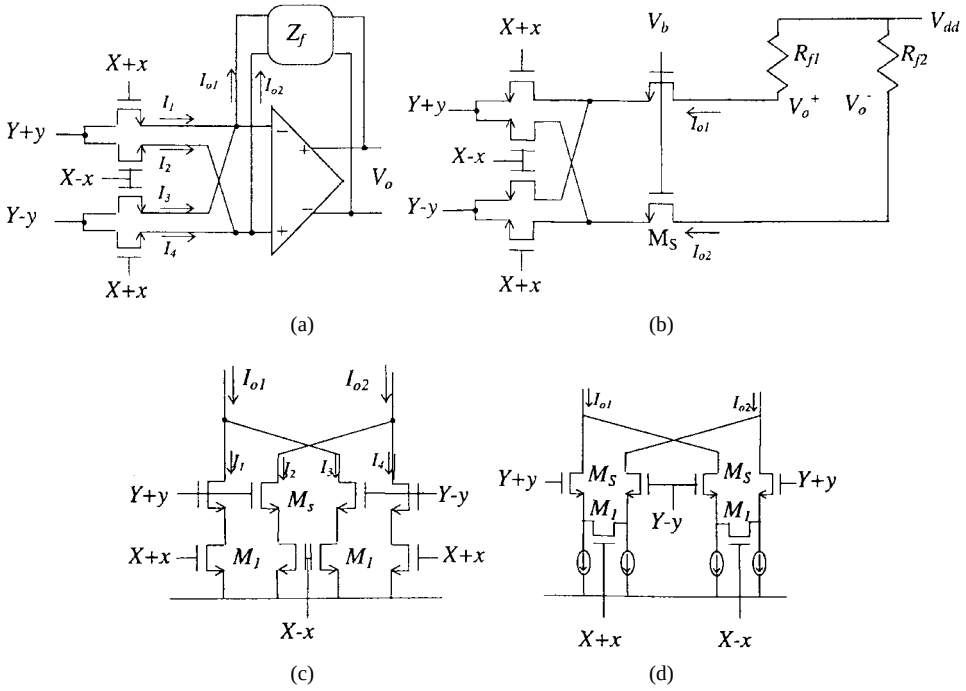


Fig. 7. Fully differential four-quadrant multipliers using $V_{\rm gs}V_{\rm ds}$ term (Type I).

[68], M_1 operates in the linear region while M_2 operates in the saturation region when proper bias voltage X and Y are provided. If the transconductance K_2 is much larger than K_1, then M_2 behaves as a source follower and $V_{\rm ds}$ of M_1 is controlled by y through the source follower M_2. The source follower can be replaced with a BJT emitter follower [69] [Fig. 5(b)] or a gain-enhanced MOS source follower [70], [71]. The configuration shown in Fig. 5(c) enhances the effective transconductance of the source follower. In the case of gain-enhanced MOS source follower, the auxiliary feedback may cause some stability problem [72] degrading transient behavior unless the amplifier $\mathbf{A}$ is properly designed.

A multiplier can be realized by combining two programmable transconductors as shown in Fig. 6(a). The output currents are obtained from (7) where $X \pm x = V_{\rm gs}$ and $y = V_{\rm ds}$.

$$\begin{cases} I_1 = K\left(X + x - V_T - \frac{y}{2}\right)y \\ I_1 = K\left(X - x - V_T - \frac{y}{2}\right)y \end{cases} \tag{9}$$

The difference of output current yields a multiplication as

$$I_o = I_1 - I_2 = 2Kxy. \tag{10}$$

In Fig. 6(a), the op amps keep the sources of the FET virtually grounded. This approach has been used in conjunction with switched-capacitor circuits to implement a weighted-sum or a weighted-integrator [5]–[8]. The configuration in Fig. 6(b) uses MOS source followers and achieves multiplication in the same way in (9) except y in (9) is replaced with $Y \pm y - V_T$. This configuration is reported in [9]–[13] with gain-enhanced source follower.

A fully differential configuration improves the linearity and PSRR further because a better nonlinearity cancellation is obtained. The fully differential configuration using four MOS transistors operating in the linear region is shown in Fig. 7. These configurations are based on the topology in Fig. 3(a) and correspond to (5), yielding

$$I_o = I_{o1} - I_{o2} = (I_1 + I_3) - (I_2 + I_4) = 4Kxy \tag{11}$$

or

$$V_o = -Z_f I_o = -4KZ_f xy. \tag{12}$$

The op amp in Fig. 7(a) [14]–[16] can be replaced by the source followers shown in Fig. 7(b) [17]. This is possible because the purpose of the op amp is to keep the source potential of transistors constant. The circuit shown in Fig. 7(c) [18] is the fully (pseudo) differential extension of the circuit shown in Fig. 6(b) for a complete implementation of (5). The $V_{\rm ds}$ of M_1, which is operating in linear region, also can be applied as shown in Fig. 7(d) [19], [20].

B. Using $V_{\rm ds}^2$ (TYPE II)

The MOS FET operating in the linear region has a square term, $V_{\rm ds}^2$ as in (7). This term can be used to realize the cancellation method in (6). In Fig. 8, sum and difference of two input signals are applied to the gate of source followers, M_s, and they control the drain voltage of M_1 that operates in the linear region. The summer indicated at the gate of M_s can be implemented using an active circuitry or passive components such as resistors or a floating gate [66]. This circuit, based on (6), yields

$$I_o = I_{o1} - I_{o2} = Kxy \tag{13}$$

However, the linearity of this configuration is poor.

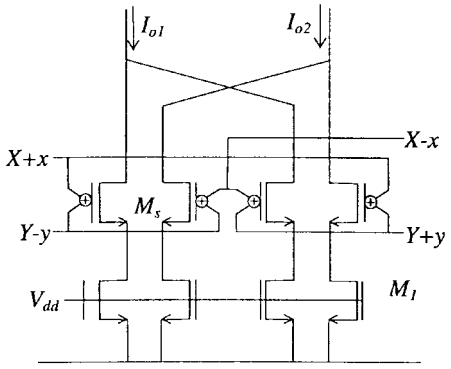


Fig. 8. Multiplier using $V_{\rm ds}^2$ (type II).

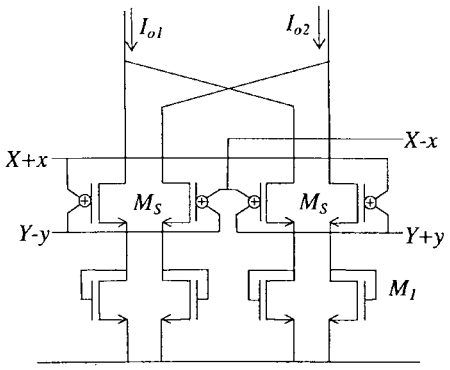
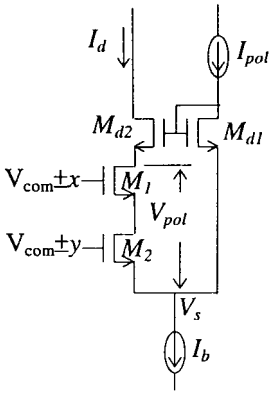
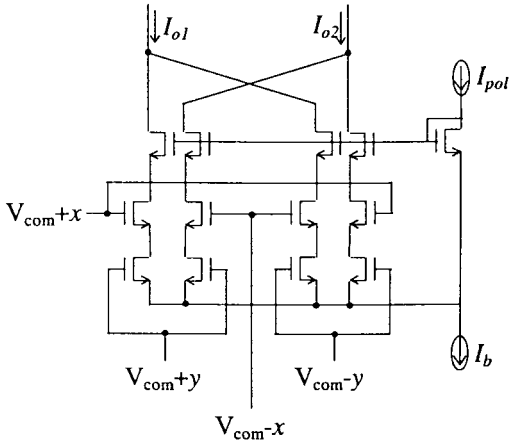


Fig. 10. Multiplier using $V_{\rm gs}^2$ with diode connection (type IV).



(a)



(b)

Fig. 9. Four quadrant multiplier using dual gate (type III).

C. Dual Gate in Linear Region (TYPE III)

Another method to inject $V_{\rm ds}$ signal is by modulation [21] [see Fig. 9(a)]. Note that $M_{d1} = M_{d2}$ operate in the saturation region while the others (M_1, M_2) are in the linear region. The output current of circuit Fig. 9(b) can be obtained as

$$\begin{aligned} I_o &= I_{o1} - I_{o2} \\ &= 8KV_{\rm pol}Cxy\frac{x^2+y^2-2C^2}{(4C^2-(x+y)^2)(4C^2-(x-y)^2)} \\ &\approx \frac{KV_{\rm pol}}{C}xy \end{aligned} \tag{14}$$

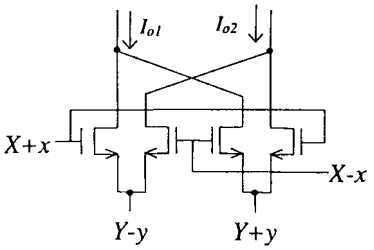


Fig. 11. Four cross-coupled FET's multiplier using $V_{\rm gs}^2$ term.

where

$$V_{\rm pol} \approx \sqrt{\frac{I_{\rm pol}}{K_d}} \quad \text{for } I_d \ll I_{\rm pol},$$
$$C = V_{\rm com} - V_s - V_T - V_{\rm pol} \quad \text{and} \quad C \gg x, y. \tag{15}$$

However, it does not have clear advantage over other multiplier types.

II.2. MOS Multipliers Operating in Saturation Region

A. Using $V_{\rm gs}^2$ with Diode Connection (TYPE IV)

The drain current of a diode-connected MOS FET depends on $V_{\rm ds}^2$ in the saturation region. Thus, this signal can be applied using source follower whose gate input is the sum and difference of two input signals as shown in Fig. 10. The topology is similar to type II. However, the linearity of this configuration is often poorer.

B. Using $V_{\rm gs}^2$ with Gate and Source Injection (TYPE V)

A four-quadrant multiplier based on Fig. 3(b) can be realized by four cross-coupled transistors as shown in Fig. 11. The output current I_o yields

$$I_o = I_{o1} - I_{o2} = 4Kxy \tag{16}$$

based on (6) and (8). Varieties of source signal application methods are reported in the literature. Fig. 12(a) uses an op-amp [22], (b) uses a linear differential amplifier [23], (c) uses source followers (M_s). A separate source follower, as shown in Fig. 12(d) [24], can be provided to each transistor in cross-coupled transistors. A gain-enhanced source follower [25]–[30] or a BJT emitter follower [31] can be used to apply the source signal. This type is the most widely implemented multiplier structure.

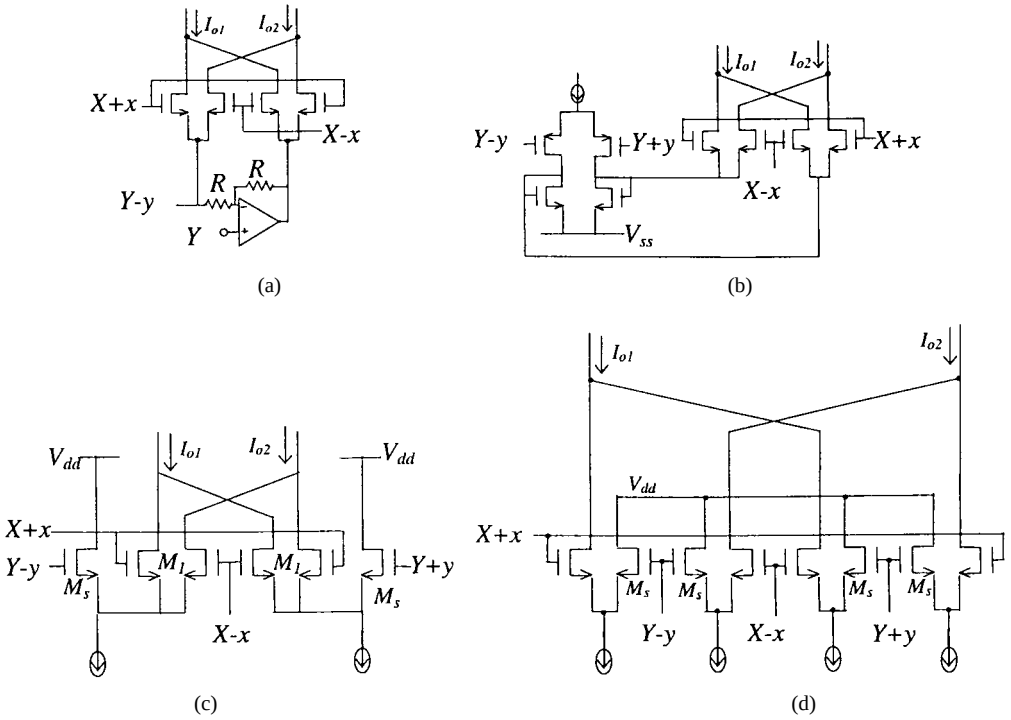


Fig. 12. Source signal injection methods for multiplier using term $V_{\rm gs}^2$ (type V).

C. Using $V_{\rm gs}^2$ with Substrate Terminal (TYPE VI)

The substrate of a MOS FET can be used as an additional input terminal as long as the substrate-source junction is kept reverse biased. The substrate potential controls the threshold voltage for an NMOS transistor as

$$V_T = V_{TO} + \gamma[\sqrt{2|\phi_F| - V_{\rm bs}} - \sqrt{2|\phi_F|}] \tag{17}$$

where V_{TO} is the threshold voltage when $V_{\rm bs} = 0$, γ is the body effect coefficient, and ϕ_F is the Fermi potential. Substituting V_T in (8) with (17), the configuration shown in Fig. 13, based on topology Fig. 3(b) and (6), gives

$$I_o = \frac{4K\gamma}{2|\phi_F| - Y + s}\left[y\sqrt{2|\phi_F| - Y + s} + \left\{\frac{y}{2(2|\phi_F| - Y + s)}\right\}^3 + \Lambda\right]x$$
$$\approx \frac{4K\gamma}{\sqrt{2|\phi_F| - Y + s}}xy. \tag{18}$$

The approximation is valid only if $2|\varphi_F| - Y + s \gg y$. However, the linearity of this configuration is poor.

D. Using $V_{\rm gs}^2$ with Voltage Adder (TYPE VII)

This multiplier architecture is based on the nonlinearity cancellation of Fig. 3(b) and voltage summing circuits. Four cross-coupled transistors with voltage summer realize a four-quadrant multiplier as shown in Fig. 14(a). The tail current can be removed as shown in Fig. 14(b). The output current is obtained as

$$I_o = 4KK_a xy \tag{19}$$

based on (6) and (8).

This configuration is reported in [32]–[34] using a capacitive adder, in [35] using a resistive adder, and in [36]–[39] using an active adder. The floating voltage source can be used as shown in Fig. 15 to realize the voltage summation [40]–[42].

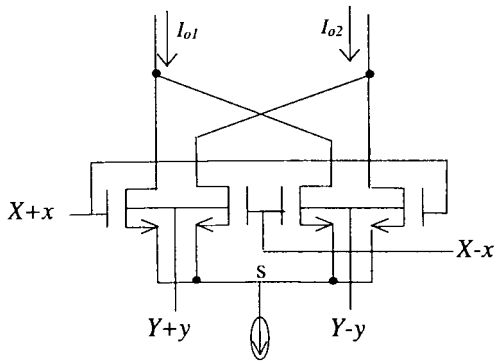


Fig. 13. Using substrate signal injection (type VI).

Reference [43] provides a summary of this multiplier type. The structure of this type is similar to type IV. As type IV requires an additional transistor, it does not have any advantage over type VII.

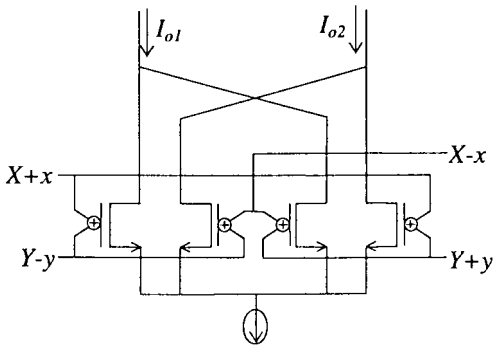
E. MOS Gilbert Cell (TYPE VIII)

A MOS differential pair operating in saturation region generates a differential output current characterized by

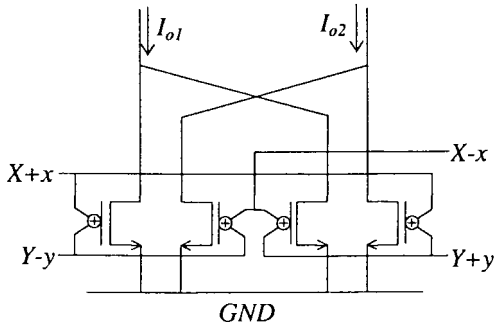
$$I_{\rm od} = I_1 - I_2 = I_s\left[\frac{K}{I_s}(2x)^2 - \frac{K^2}{4I_s^2}(2x)^4\right]^{1/2}$$
$$= 2\sqrt{KI_s}x\left[1 - \frac{K}{I_s}x^2\right]^{1/2} \tag{20}$$

for $Kx^2 < I_s$ where I_s is the tail current and x is half of the differential input voltage.

The topology shown in Fig. 16 is the same as the one shown in Fig. 11. However, here x is a voltage signal and



(a)



(b)

Fig. 14. Multipliers using voltage adder (type VII) (a) with the tail current and (b) without the tail current.

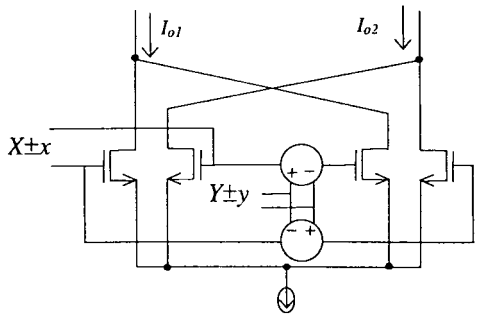


Fig. 15. Multiplier using floating voltage source (type VII).

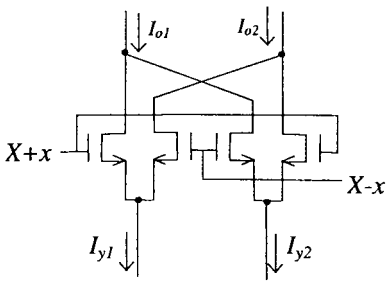
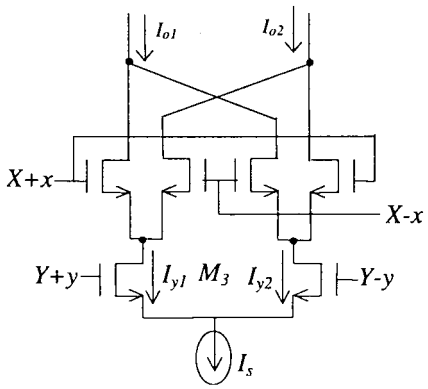
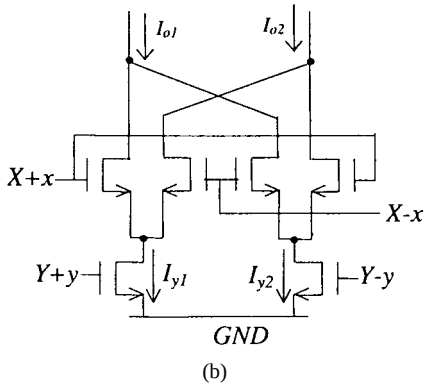


Fig. 16. Current steering circuit.



(a)



(b)

Fig. 17. MOS Gilbert multipliers (type VIII) (a) with tail current. (b) without tail current.

I_y is a current signal. The differential output currents from two differential pairs are subtracted yielding

$$I_o = I_{o1} - I_{o2} = 2\sqrt{K}x\left[\sqrt{I_{y1}} - \sqrt{I_{y2}}\right]. \tag{21}$$

The input current $\sqrt{I_{y1}} - \sqrt{I_{y2}}$ is generated by another differential pair as shown in Fig. 17(a) as

$$\sqrt{I_{y1}} - \sqrt{I_{y2}} = \sqrt{2K_3 y} \tag{22}$$

where $2y$ is the differential input voltage and K_3 is the transconductance constant of the transistor in the third differential pair. Thus, the MOS Gilbert multiplier shown in Fig. 17(a) yields

$$I_o = I_{o1} - I_{o2} = 2\sqrt{2KK_3}xy \tag{23}$$

where x and y are both voltage signals.

Note the similarity of Fig. 17(a) to Fig. 2(e) when the transconductors are replaced by differential pair. The tail current can be removed [44] as shown in Fig. 17(b). As in (20), wider input range or higher linearity is obtained with higher bias current.

Note that this cancellation scheme follows (5). The Gilbert cell is implemented using lateral BJT in CMOS process in [45]. The MOS version of Gilbert multipliers is reported in [46]. As its linearity is poor, several modified versions including linearization schemes [46]–[48], folded structures [48]–[50], and active attenuators [51] have been reported.

III. Remarks on Multiplier Structures and Fabrication Result

None of the above analyses includes higher order effects of MOS device [65] such as γ-effect, λ-effect, and mobility degradation effect. Besides the higher order effect of MOS in the multiplier core, the nonidealities of source follower

TABLE II
SUMMARY OF GENERAL COMPARISON OF 15 MULTIPLIER TOPOLOGIES

NO	Type	Circuit Diagram Figure	Worse than	Remark
1	I	7(a), 7(b)	2	Require additional circuitry.
2	I	7(c), 7(d)		
3	II, III, IV	8, 9, 10	2	Require additional circuitry. Poor linearity
4	V	12(a)	5	Require OP Amp
5	V	12(b), (c), (d)		
6	VI	13	5	Poor linearity
7	VII	14, 15	5	Require additional circuitry
8	VIII	17	2	High power supply voltage, Poor linearity

and voltage adder were not considered. Another practical limitation of the multiplier is the component mismatch that causes nonlinearity and offset.

1) General Comparison: The measurements of the multiplier performance can include input range, linearity, common-mode effects, minimum power supply voltage, power consumption, silicon area, frequency range, noise, and so on. Since all these performance measures are strongly application dependent, there is not an absolute standard comparison metric. Some limited qualitative comparisons are summarized in Table II. From this table, we can observe that the circuits shown in Figs. 7(c), (d), 12(b), (c), and (d) have properties above the "average multiplier."

2) Comparison by Simulation: These five multipliers [circuit in Figs. 7(c), (d), 12(b), (c) and (d)] are designed without optimizing a specific performance for a rough comparison through simulation. All the transistor's $W/L = 10\ \mu\text{m}/10\ \mu\text{m}$ are equal for all five multipliers. Power supply is a single 6 V. The output current is measured using 1.5 V voltage source between the output nodes and V_{dd}. The common-mode input voltage X and Y are set to allow ± 2 V differential input range for both x and y signal. Fig. 18 shows dc analysis for $x = -1 \sim 1$ and $y = -1 \sim 1$. All multiplier's differential input range $2x$ is extended to ± 2 V. Note that circuits Figs. 7(d) and 12(b) have low transconductance. Fig. 19 shows the power supply current in transient analysis for sinusoidal x input. This current can be interpreted as power consumption. Circuit Fig. 12(d) consumes significantly higher power than any other circuit. Fig. 20 shows Monte Carlo analysis of device mismatch sensitivity when one of the input signals is kept constant. The output current of circuit Figs. 7(d) and 12(b) show high sensitivity on device mismatch. Fig. 21 shows total harmonic distortion (THD) when the other input signal is fixed to be 1 V. In this Fig. 21, we can observe that the circuit Fig. 12(d) shows the worst linearity for both input signals. Circuit Fig. 7(d) and the circuit Fig. 12(d) show poor linearity for y input signal.

Note that this tendency is generally true, although the above results are dependent on the transistor size ratio, process

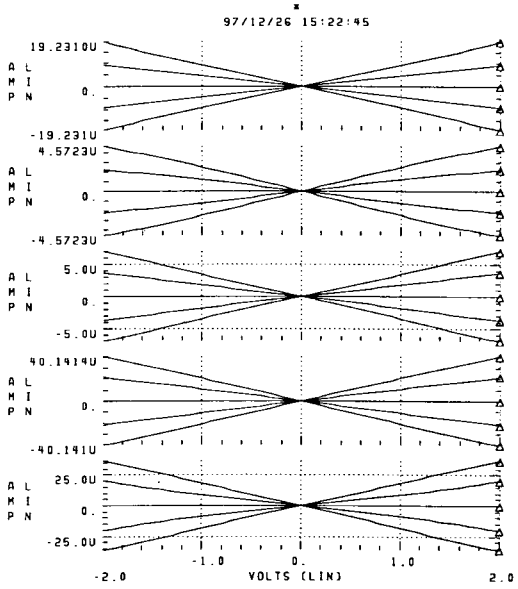


Fig. 18. DC analysis: I_o versus $2x$.

parameters, and bias conditions. From the above simulation results summarized in Table III, and complexity of circuit topologies, circuits of Figs. 7(c) and 12(c) might be considered to have better performance than others because:

1. the circuit Fig. 7(d) has low transconductance, is sensitive to mismatch, and has poor linearity;
2. the circuit Fig. 12(b) is sensitive to mismatch and has low transconductance;
3. the circuit Fig. 12(d) consumes high power and has poor linearity.

Now we focus our attention to these two multipliers with good properties [Figs. 7(c) and 12(c)].

3) Detailed Linearity Simulation: For comparison between circuits Figs. 7(c) and 12(c), the effect of source follower's transistor size is simulated. All other transistors have W/L $= 10\ \mu$m/10 μm. Fig. 22 shows that the linearity of circuit Fig. 7(c) improves as the source follower uses larger W/L ratio. On the contrary, this effect is not clear in the case of

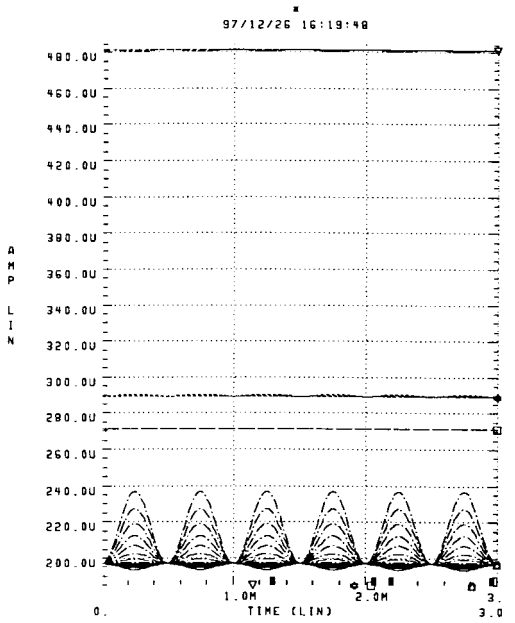


Fig. 19. Power supply current for $2x = 1$ $2y = 1$ V_{p-p}.

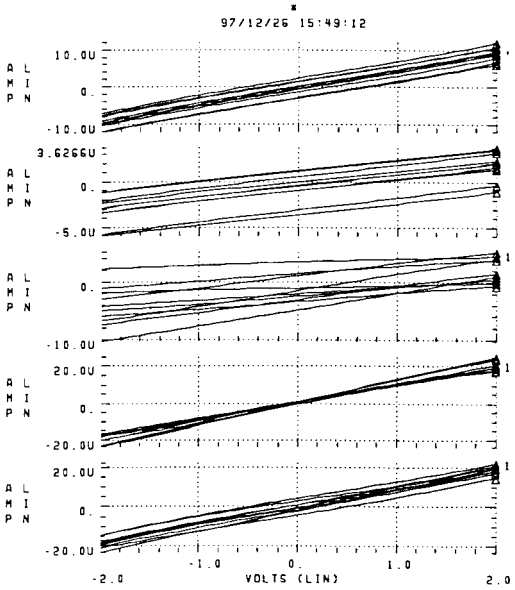


Fig. 20. Monte Carlo analysis for fixed $2x = 1v$.

circuit Fig. 12(c). This simulation result implies that circuit Fig. 7(c) can outperforms circuit Fig. 12(c) when K_s (or $(W/L)_s$) is large enough (at least three times larger than K_1).

4) Comparison by Experimental Result: Considering the above simulation result, circuits Figs. 7(c), (d), and 12(c) are fabricated using Orbit 2μm N-well process. These multipliers were designed with identical transistor size ($(W/L)_1 = 4\mu/17\mu$ and $50\mu/10\mu$ for all others), transconductance (10 μA/V), and power consumption (360 μW). The input common-mode voltages (X and Y) are set to allow approximately ± 2 V differential input range for both x and y.

Fig. 23(a) and (c) show the output differential currents (for simplicity, only one quadrant is shown in the figures) from three fabricated multipliers. The linearity errors are shown in Fig. 23(b) and (d). The linearity error of the circuit Fig. 7(c) is

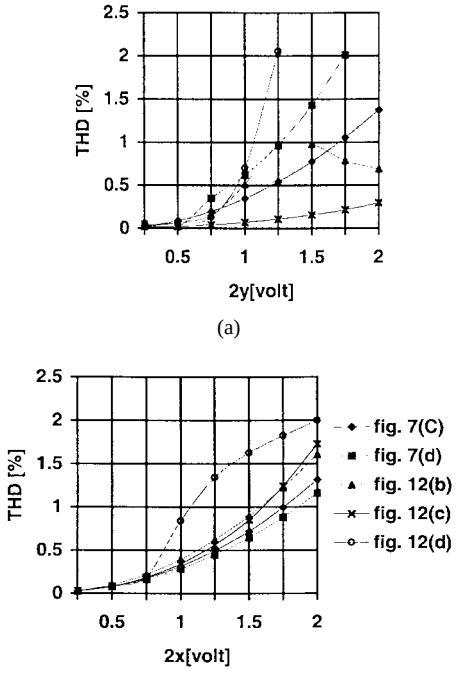


Fig. 21. Simulated total harmonic distortion (THD) for W/L = 10 μm/10 μm for all transistors. (a) $2x = 1$ V and (b) $2y = 1$ V.

TABLE III
SUMMARY OF A COMPARATIVE MULTIPLIER STUDY FOR EQUAL SIZE TRANSISTORS

Circuit	Max G_m [μA/V]	Power Consumption[mW]	Mismatch Sensitivity	Linearity x	Linearity y
Fig. 7(c)	20	238	Good	Good	Bad
Fig. 7(d)	4.6	270	Bad	Good	Bad
Fig. 12(b)	5	200	Worst	Bad	Bad
Fig. 12(c)	40	295	Best	Bad	Best
Fig. 12(d)	25	480	Good	Worst	Worst

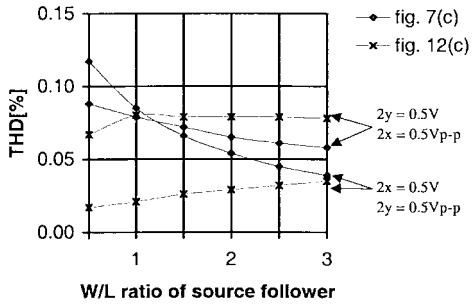


Fig. 22. Effect of source follower's W/L ratio on THD.

lower than 0.5% and much better than the others because the W/L ratio of the source follower is much larger than that of M_1. Note that circuit Fig. 7(d) has poorer linearity than circuit Fig. 7(c) and circuit Fig. 12(c) due to device mismatch. These results agree well with the simulation results discussed before.

5) Input Range and Minimum Power Supply Voltage: Input range of circuits Figs. 7(c) and 12(c) are obtained from their bias conditions shown in Fig. 24. The conditions for circuit

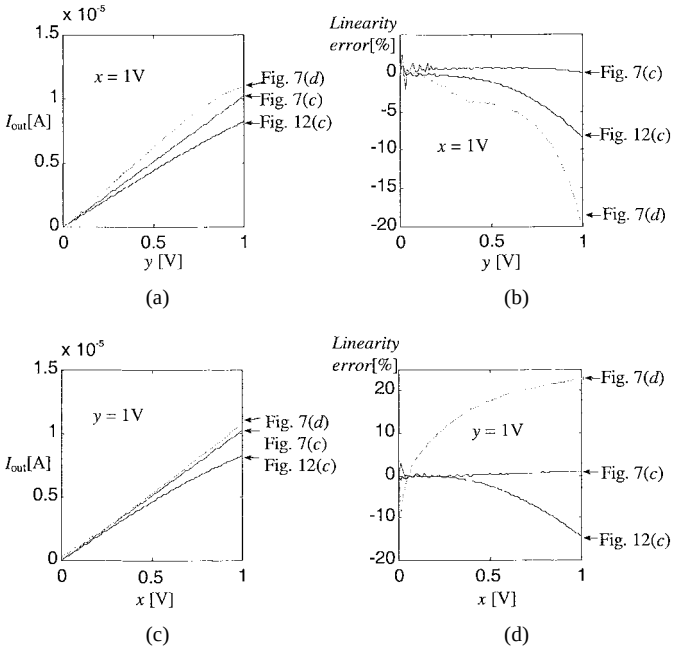


Fig. 23. Measurement results for $W/L_{m1} = 5\ \mu$m/17 μm and $W/L_{\text{sourcefollower}} = 50\ \mu$m/10 μm. (a) Output current for fixed x, (b) Linearity error for fixed x, (c) output current for fixed y, and (d) Linearity error for fixed y.

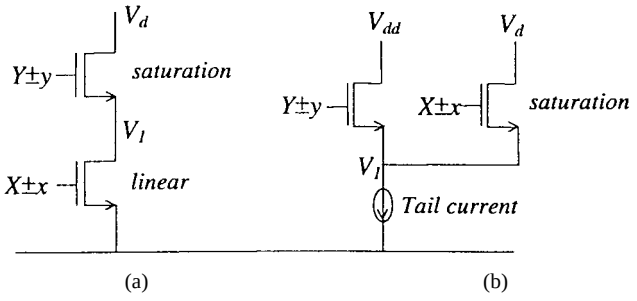


Fig. 24. Bias conditions. (a) Circuit Fig. 7(c) and (b) circuit Fig. 12(c).

Fig. 7(c) are

$$\begin{cases} V_T < X \pm x \\ V_1 = Y \pm y - V_T < X \pm x - V_T \\ V_T < Y \pm y \\ Y \pm y - V_T < V_d \end{cases} \tag{24}$$

and they are depicted in Fig. 25(a). The conditions for circuit Fig. 12(c) are

$$\begin{cases} V_{\text{ds sat;tail}} < V_1 = Y \pm y - V_T \\ V_1 + V_T = Y \pm y < X \pm x \\ X \pm x - V_T < V_d \end{cases} \tag{25}$$

and they are depicted in Fig. 25(b). For the same input range and output node voltage swing V_o, circuit Fig. 7(c) requires much lower power supply voltage than Fig. 12(c). For instance, for a 1-V input range for both x and y input signal, threshold voltage $V_T = 1$ V and a 2 V output signal swing, the circuit Fig. 7(c) requires 3 V power supply while the circuit of Fig. 12(c) requires more than 4 V power supply.

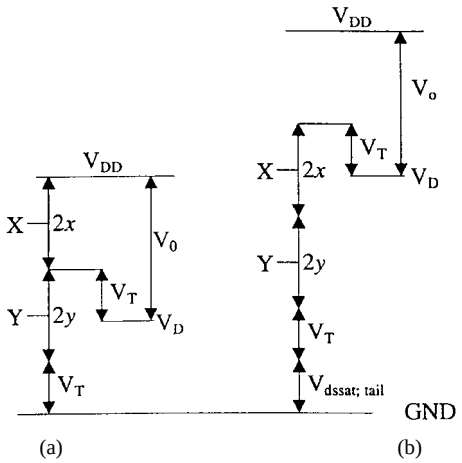


Fig. 25. Input range and power supply voltage. (a) Circuit Fig. 7(c) and (b) circuit Fig. 12(c).

6) Remarks on Noise: Another performance measure of a multiplier is noise, especially for small signal applications where the input range is not a major concern. A thermal noise current power density of a MOS transistor is conventionally modeled as

$$\begin{cases} \overline{i_{n;\text{lin}}^2} = 4kTg_{\text{ds}}\,df \\ \overline{i_{n;\text{sat}}^2} = \frac{8}{3}kTg_{m1}\,df \end{cases} \tag{26}$$

for transistor operating in linear and saturation, respectively [73]. In the case of circuit Fig. 7(c), total output noise current is given

$$\begin{aligned} \overline{i_{n;o}^2} &= 4\left(\overline{i_{n;\text{lin}}^2} + \overline{i_{n;\text{sat}}^2}\right) = 4\left(4kTg_{\text{ds}1}\,df + \frac{8}{3}kTg_{m2}\,df\right) \\ &= 16kT\left(g_{\text{ds}1} + \frac{2}{3}g_{m2}\right)df \end{aligned} \tag{27}$$

where

$$\begin{aligned} g_{\text{ds}1} &= K_1(V_{\text{GS}1} - V_T - V_{\text{DS}1}) \\ &= K_1(X - V_T - (Y - V_T)) = K_1(X - Y) \end{aligned} \tag{28}$$

$$\begin{aligned} g_{m2} &= \sqrt{2K_2I_{\text{DQ}}} \\ &= \sqrt{2K_2K_1\left(X - V_T - \frac{Y - V_T}{2}\right)(Y - V_T)}. \end{aligned} \tag{29}$$

In the case of circuit Fig. 12(c), if the current source has the same transistor size as the source follower, then the total output noise current is given

$$\overline{i_{n;o}^2} = 4\left(\overline{i_{n;Ms}^2} + \overline{i_{n;M1}^2}\right) = 4 * \frac{8}{3}kT(g_{\text{ms}} + g_{m1})\,df. \tag{30}$$

If $g_{ms} = g_{m2}$, then circuit Fig. 12(c) has higher output noise because g_{m1} in (30) is much larger than $g_{\text{ds}1}$ in (27). The output noise floors of fabricated multipliers are measured with 1-kΩ resistor at 1 kHz. The circuit Fig. 7(c) showed 26 dB lower noise floor than circuit Fig. 12(c).

TABLE IV
SUMMARY OF COMPARISON BETWEEN CIRCUIT FIG. 7(c), FIG. 7(d), AND FIG. 12(c)

Circuit	Linearity	Minimum Power Supply	Noise
Fig. 7(c)	Good	Good	Good
Fig. 7(d)	Bad	Bad	Bad
Fig. 12(c)	Good	Bad	Bad

IV. DESIGN CONSIDERATION OF CIRCUIT FIG. 7(C)

Table IV summarizes the above comparison and proposes the circuit Fig. 7(c) as the most recommended analog MOS multiplier structure. The circuit Fig. 7(c) has clear tradeoff between noise and linearity.

The input reflected equivalent noise voltage of circuit Fig. 7(c) is obtained by dividing (27) by the square of transconductance of multiplier G_m, which is determined by K_1 as in (11), yielding

$$\overline{v_{n;i}^2} = \frac{\overline{i_{n;o}^2}}{G_m^2} = \frac{\overline{i_{n;o}^2}}{16K_1^2} = \frac{kT}{K_1^2}\left(g_{\mathrm{ds1}} + \frac{2}{3}g_{m2}\right) df \qquad (31)$$

when other input is unity. Substituting g_{ds1} and g_{m2} in (31) with (28) and (29) results in

$$\overline{v_{n;i}^2} = \frac{kT}{K_1}\left((X-Y) + \frac{2}{3}\sqrt{2\frac{K_2}{K_1}\left(X - \frac{Y+V_T}{2}\right)(Y-V_T)}\right) df. \qquad (32)$$

This analysis suggests that $(X-Y)$ and K_2/K_1 should be reduced to improve the noise performance for the given K_1. This is the direct tradeoff with linearity and input range because K_2/K_1 should be increased to improve linearity as illustrated in Fig. 22, and $(X-Y)$ determines the input range shown in Fig. 25(a).

The noise performance of circuit Fig. 7(c) is verified through simulation. In the simulation, the output noise is measured at the one of the output node with 50-Ω load resistor and integrated within 1 MHz–2 MHz range. For all simulation, the transistor length is 10 μm for all transistors. Fig. 26(a) shows that the total output noise is almost a linear function of $(W/L)_1$ as expected from (27), (28), and (29) when the source follower's transconductance is large enough $((W/L)_s = 20)$. The input reflected equivalent noise is inversely proportional to $(W/L)_1$ as shown in Fig. 26(b). This result agrees with analysis in (32). However, if the source follower is not large enough $((W/L)_s = 10)$, (32) is no longer valid as shown in Fig. 26(b) because (32) is based on the assumption that the source follower is an ideal one. The noise performance starts to be degraded when K_2/K_1 is smaller than around three ($(W/L)_s = 10$ and $(W/L)_1 = 3$). Fig. 27 shows the noise dependency on source follower size and suggests K_2/K_1 ratio larger than around three ($(W/L)_s = 3$ and $(W/L)_1 = 1$). These analyses are conflicting each other as follows.

1) From Figs. 26(b) and 28, the K_2/K_1 ratio should be larger than three to make (32) valid.

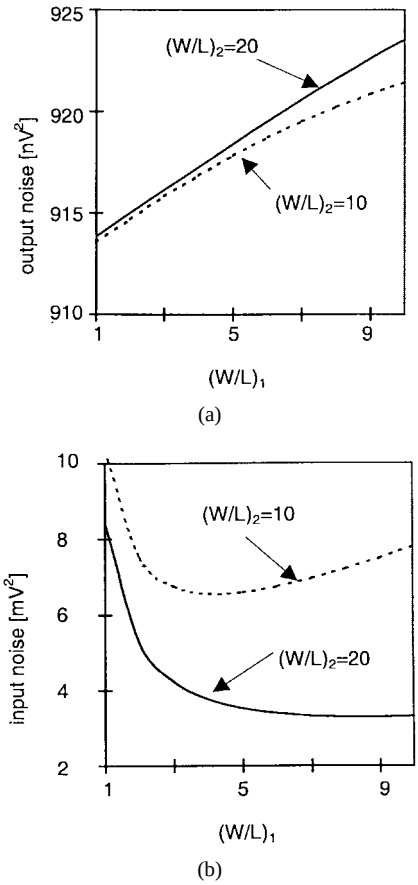


Fig. 26. Noise dependency on $(W/L)_1$ for $(X+Y)/2 = 4$ V and $X-Y = 2$ V.

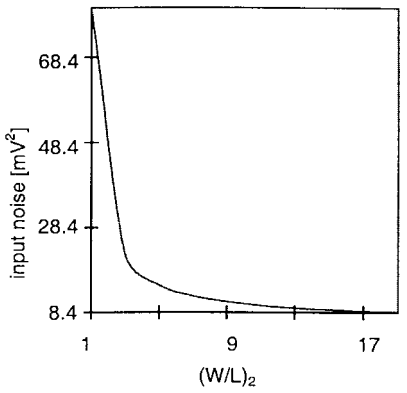


Fig. 27. Input noise dependency on $(W/L)_2$: $(W/L)_1 = 1$, $V_{com} = (X+Y)/2 = 4$ V and $X-Y = 2$ V.

2) From (32), the K_2/K_1 ratio should be minimized for low input reflected noise.

These two observations lead us to the conclusion that the optimal K_2/K_1 ratio for low noise design is around three for this specific process. Remember that K_2/K_1 ratio should be maximized for high linearity as shown in Fig. 22.

Fig. 28 shows that the input noise is almost a linear function of the difference of two input common-mode voltages, $(X-Y)$, as expected in (32). This difference is the summation of two input ranges. Therefore, for low noise design, the input range should be sacrificed.

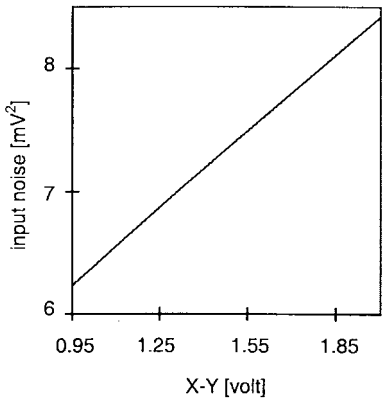


Fig. 28. Noise dependency on $(X-Y)$ for $W_1 = 10\ \mu$m, $W_2 = 200\ \mu$m, $L = 10\ \mu$m and $V_{com} = 4$ V.

In designing the circuit Fig. 7(c), K_2/K_1 ratio and $(X-Y)$ are the most important design parameters that determine the tradeoff among noise, linearity, and input range.

V. Conclusion

Although a large number of transconductance multipliers are reported in the literature, they fall into eight categories described in this tutorial and are summarized in Table I.

Several multiplier architectures do not have any clear advantage over others. As the current trend of circuit design is low voltage and low power, the circuit shown in Fig. 7(c) seems to be one of the most attractive low-voltage and high-performance MOS multiplier structures. A BiCMOS version that uses BJT instead of the source follower will improve its performance. Several design considerations of the circuit Fig. 7(c) were provided.

A reader should be aware that this comparison might not hold for all cases. The choice of circuit topology is completely dependent on design specifications.

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Gilbert cell

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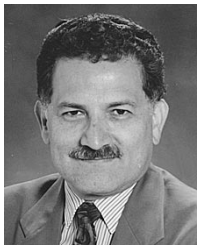
Gunhee Han received the B.S. degree from Yonsei University, Seoul, Korea, in 1990 and the Ph.D. degree from Texas A&M University, College Station, in 1997.

He was a Visiting Assistant Professor in Texas A&M University during the 1997–1998 academic year. He is an Assistant Professor in the Department of Electronic Engineering in Yonsei University as of August 1998. His research interests include mixed-signal circuit design, neural network, and digital signal recovery.



Edgar Sánchez-Sinencio (F'92) was born in Mexico City, Mexico, on October 27, 1944. He received the degree in communications and electrical engineering (professional degree) from the National Polythecnic Institute of Mexico in 1966. He received the M.S.E.E. degree from Stanford University, Stanford, CA, and the Ph.D. degree from the University of Illinois at Champaign-Urbana, in 1970 and 1973, respectively.

He did an industrial Post-Doctoral with Nippon Electric Company, Kawasaki, Japan, in 1973–1974. Currently he is with the Department of Electrical Engineering at Texas A&M University, as a Professor. He is the co-author of *Switched-Capacitor Circuits* (New York: Van Nostrand-Reinhold, 1984) and co-editor of *Artificial Neural Networks: Paradigms, Applications, and Hardware Implementation* (Piscataway, NJ: IEEE Press, 1992).

Dr. Sánchez-Sinencio has been the Guest Editor or Co-Editor of three special issues on Neural Network Hardware (IEEE TRANSACTIONS ON NEURAL NETWORKS, March 1991, May 1992, and May 1993) and one special issue on Low Voltage Low Power Analog and Mixed-Signal Circuits and Systems (IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I, November 1995). His present interests are in the area of solid-state processing circuits, including BiCMOS, CMOS RF communication circuits, data converters, and testing. He was the IEEE/CAS Technical Committee Chairman on Analog Signal Processing (1994–1995). He has been Associate Editor for different IEEE magazines and transactions from 1982 till the present. He was the IEEE Video Editor for the IEEE TRANSACTIONS ON NEURAL NETWORKS. He was IEEE Neural Network Council Fellow Committee Chairman 1994 and 1995. He was a member of the IEEE Circuits and Systems Society Board of Governors (1990–1992). He was the 1993–1994 IEEE Circuits and Systems Vice-President-Publications and a member of the IEEE Press Editorial Board. Currently, he is the Editor-in-Chief for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II. He has been co-recipient of the 1997 Darlington Award for his work on high-frequency filters and also a co-recipient of the 1995 Guillemin-Cauer Award for his work on cellular networks. He was awarded with a Halliburton Professorship in 1993. In 1992 he was elected as a Fellow of the IEEE for contributions to monolithic analog filter design. In 1995, he received an Honoris Causa Doctorate from the National Institute for Astrophysics, Optics and Electronics, Puebla, Mexico.