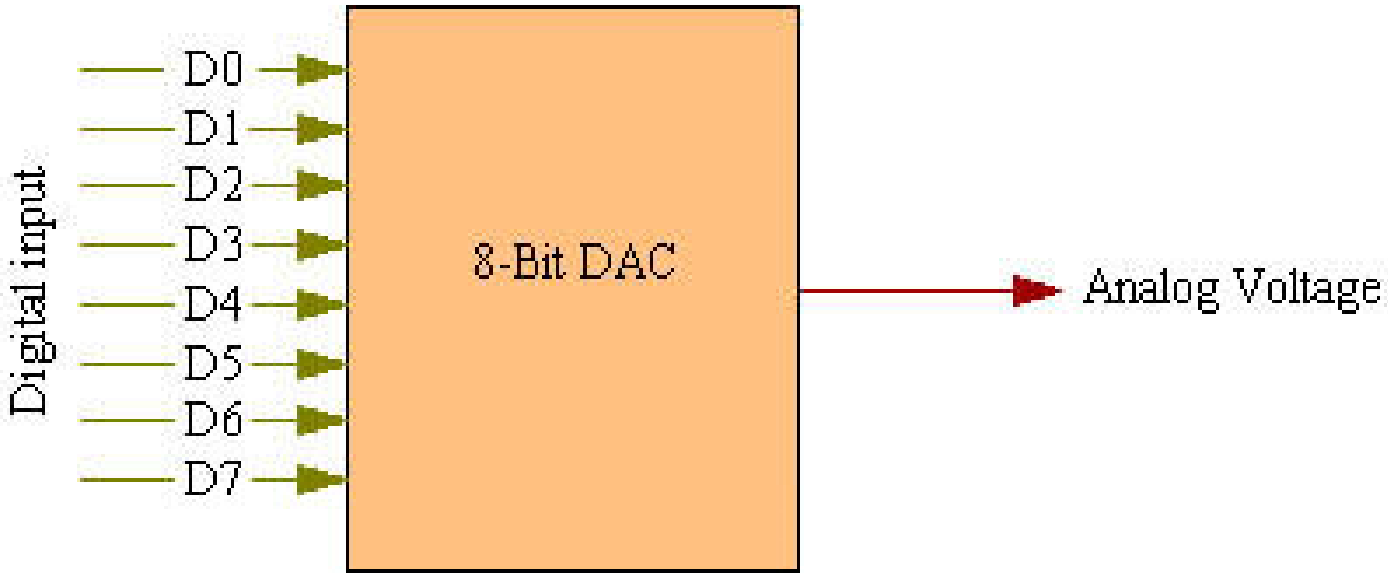
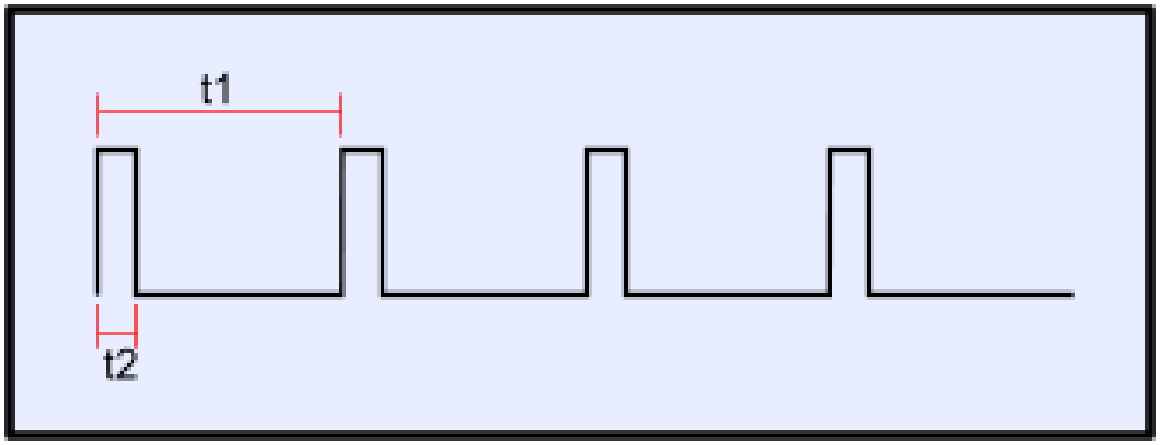
Digital to Analog Converter

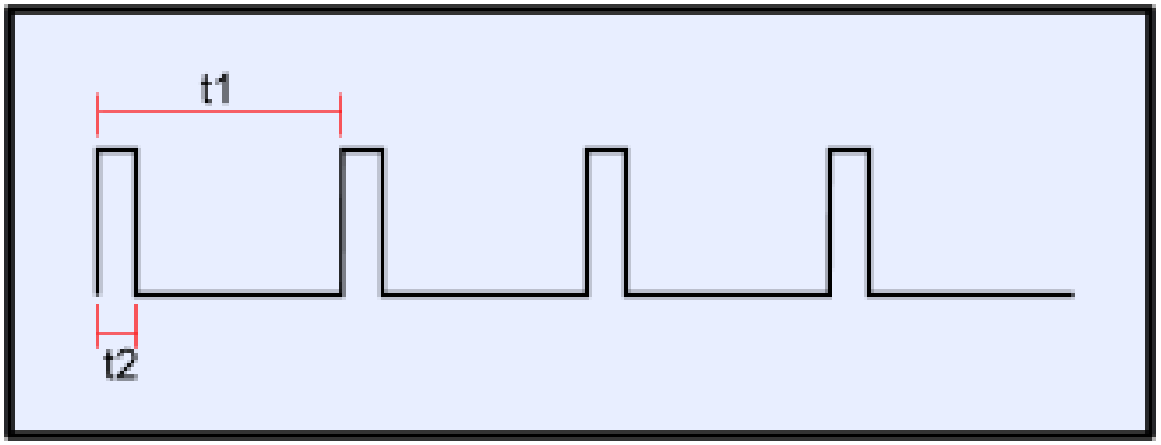


Pulse Width Modulation (PWM)

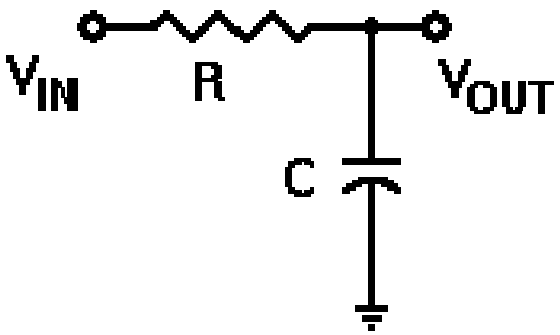


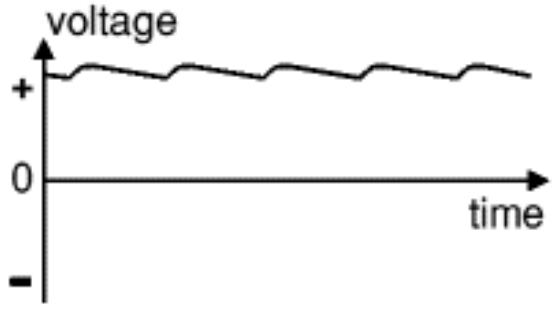
Duty cycle = **t2 / t1**

Pulse Width Modulation (PWM)



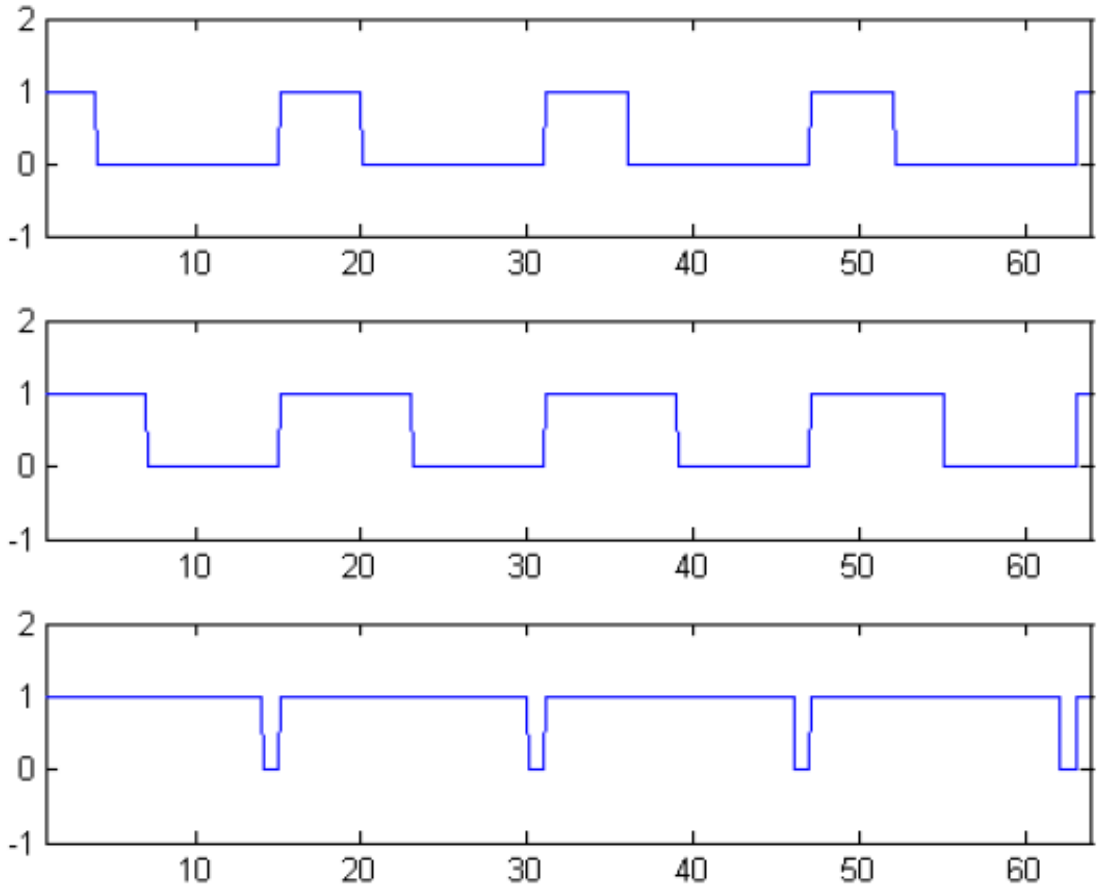
Duty cycle = **t2 / t1**



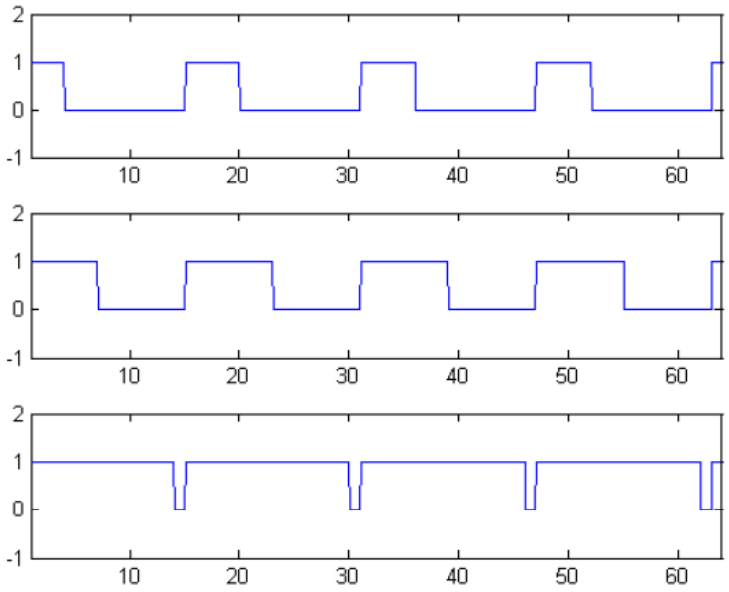


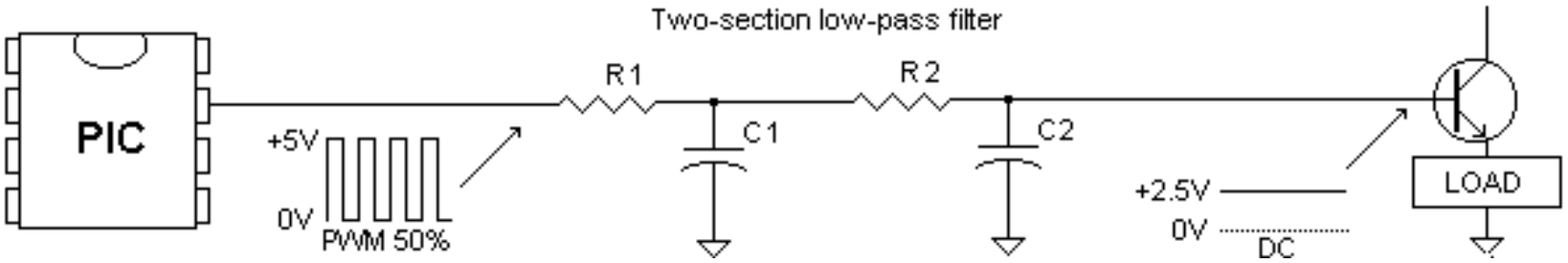
Output: smooth DC

Pulse Width Modulation (PWM)



Pulse Width Modulation (PWM)





Resistor String DAC

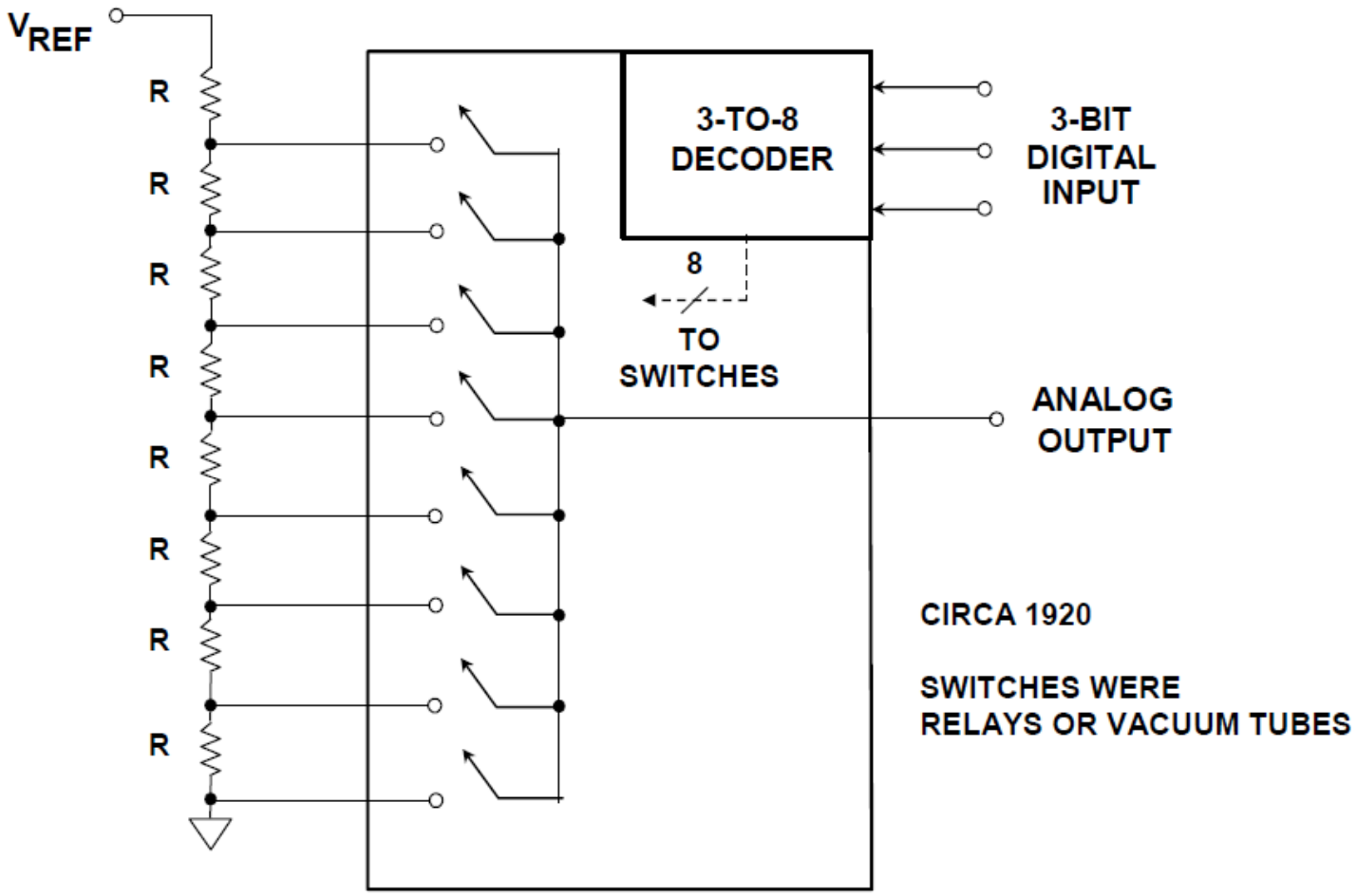


Figure 2: Simplest Voltage-Output Thermometer DAC: The Kelvin Divider ("String DAC")

Resistor String DAC

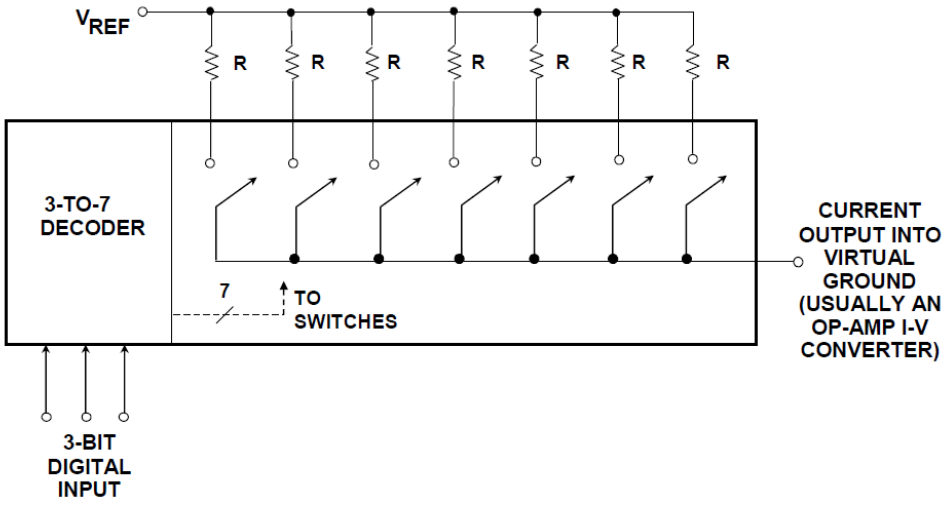


Figure 4: The Simplest Current-Output Thermometer (Fully-Decoded) DAC

Resistor String DAC

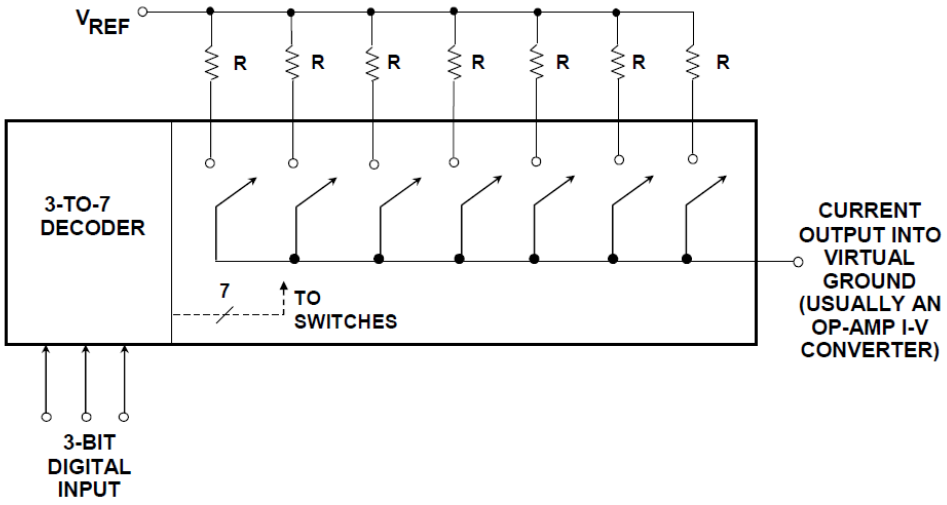


Figure 4: The Simplest Current-Output Thermometer (Fully-Decoded) DAC

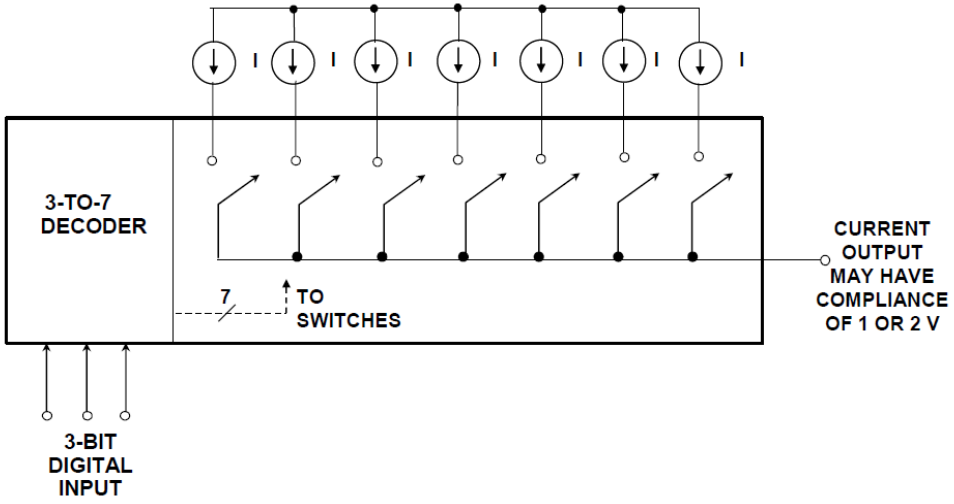


Figure 5: Current Sources Improve the Basic Current-Output Thermometer DAC

Resistor String DAC

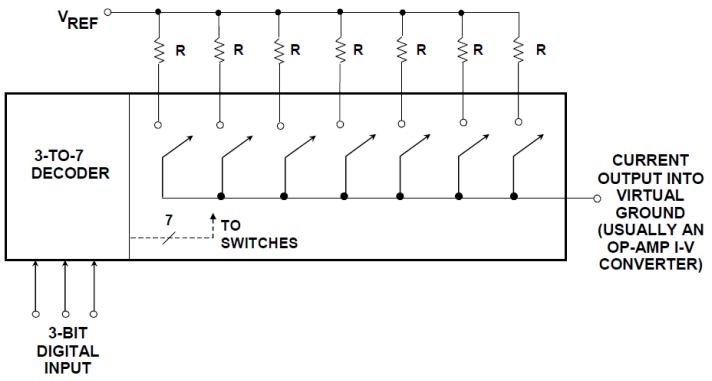


Figure 4: The Simplest Current-Output Thermometer (Fully-Decoded) DAC

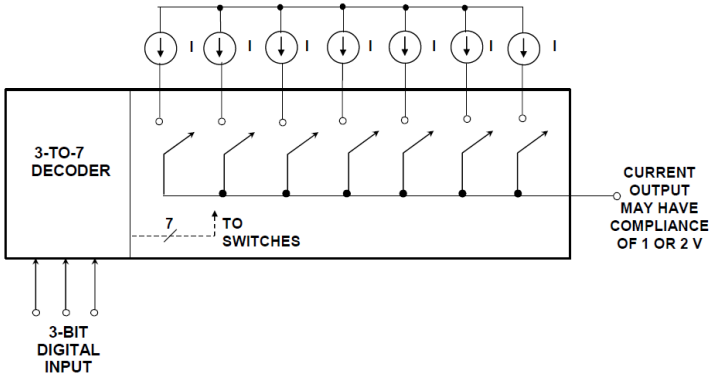


Figure 5: Current Sources Improve the Basic Current-Output Thermometer DAC

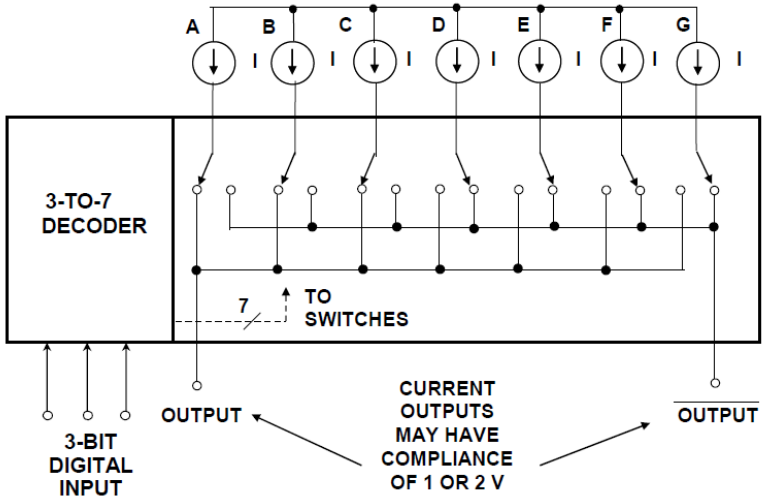


Figure 6: High Speed Thermometer DAC with Complementary Current Outputs

Resistor String DAC

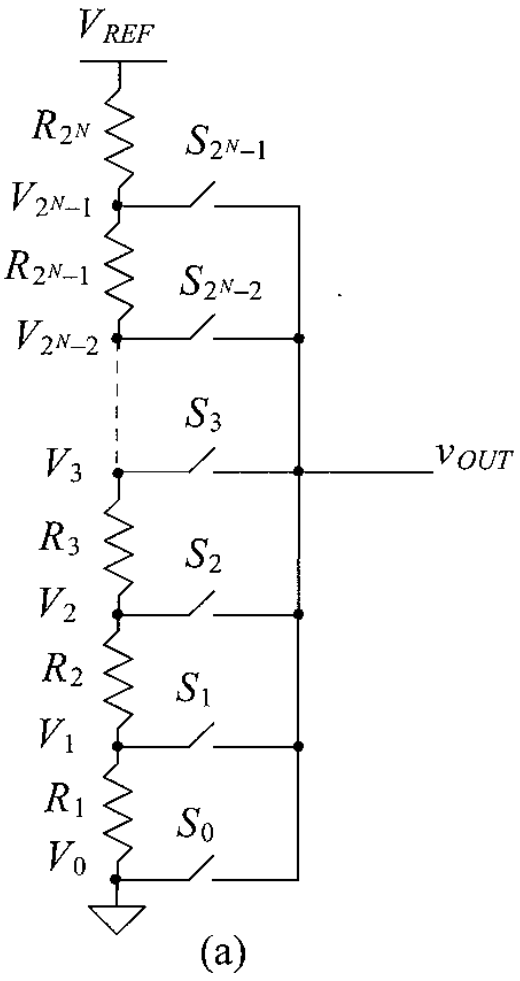


Figure 29.2 (a) A simple resistor-string DAC

Resistor String DAC

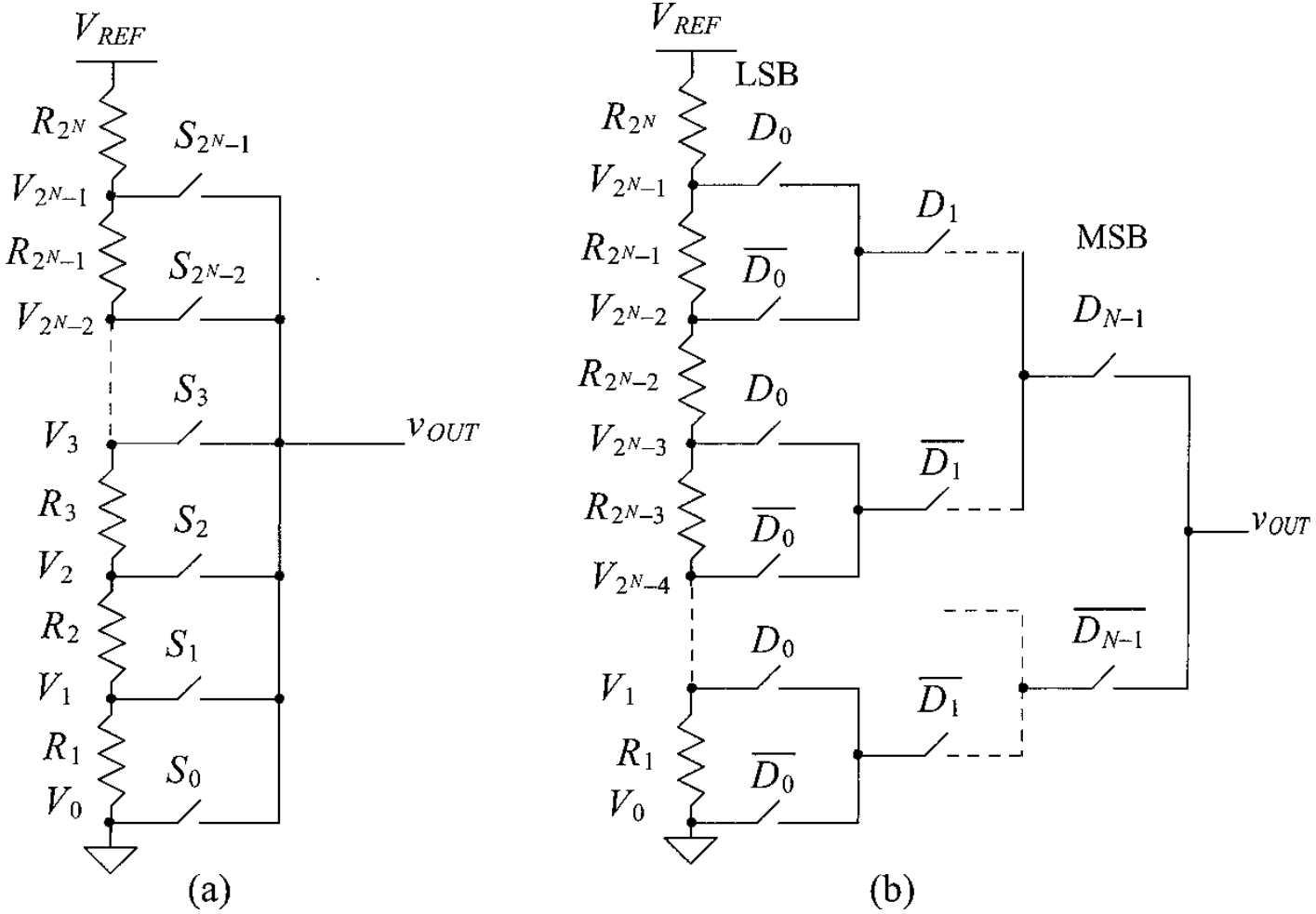
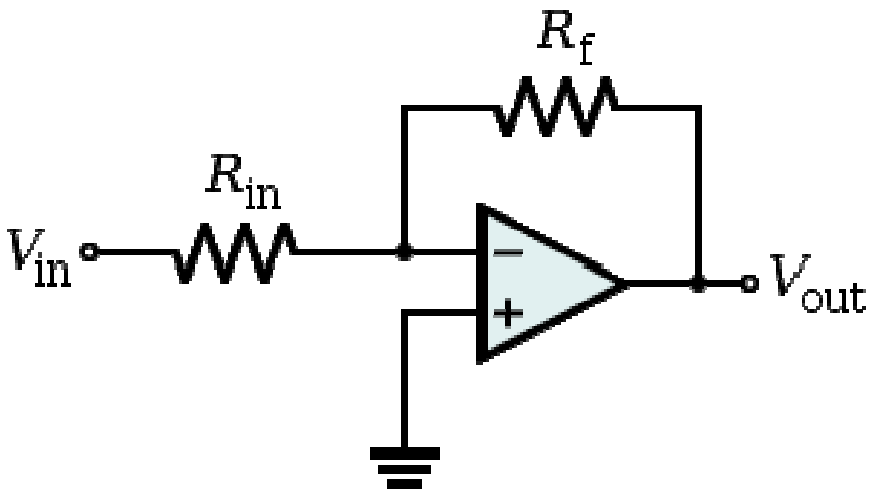
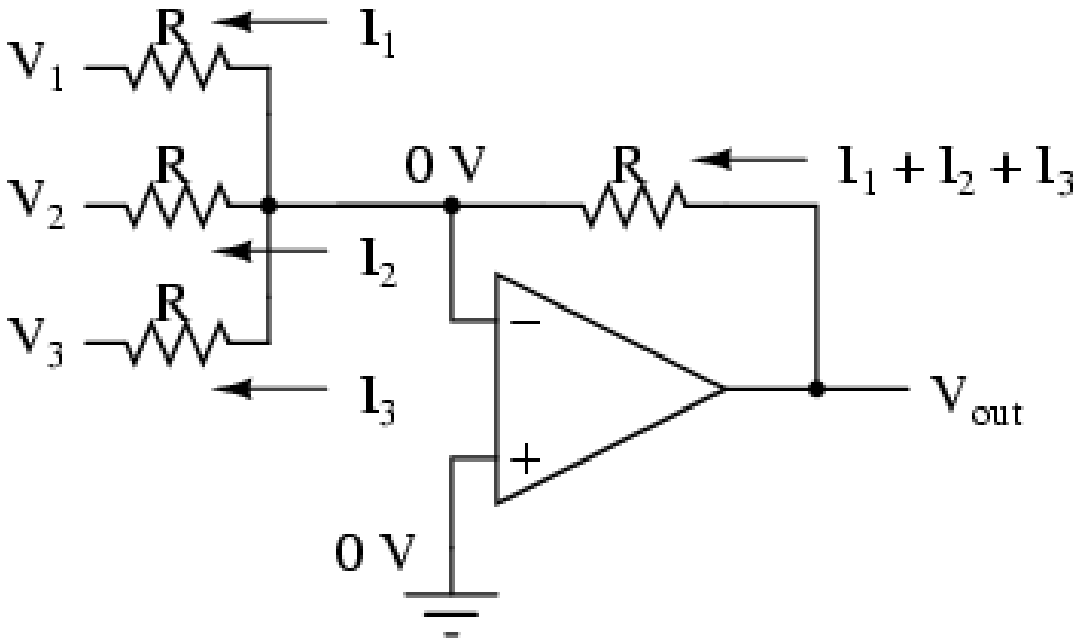


Figure 29.2 (a) A simple resistor-string DAC and (b) the use of a binary switch array to lower the output capacitance.

Inverting Op Amp

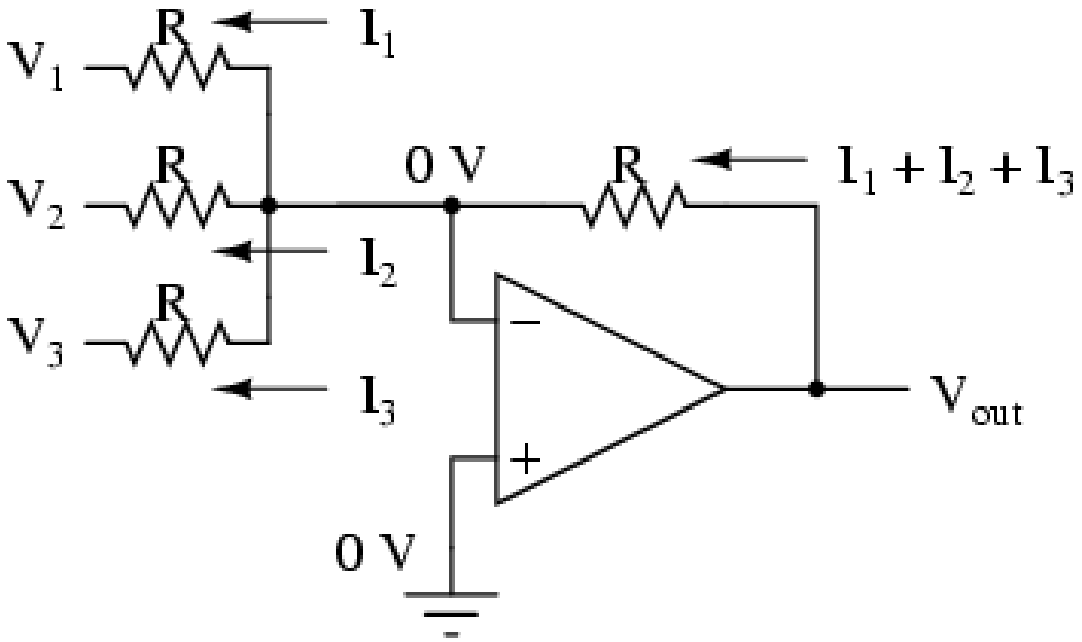


Inverting summer circuit



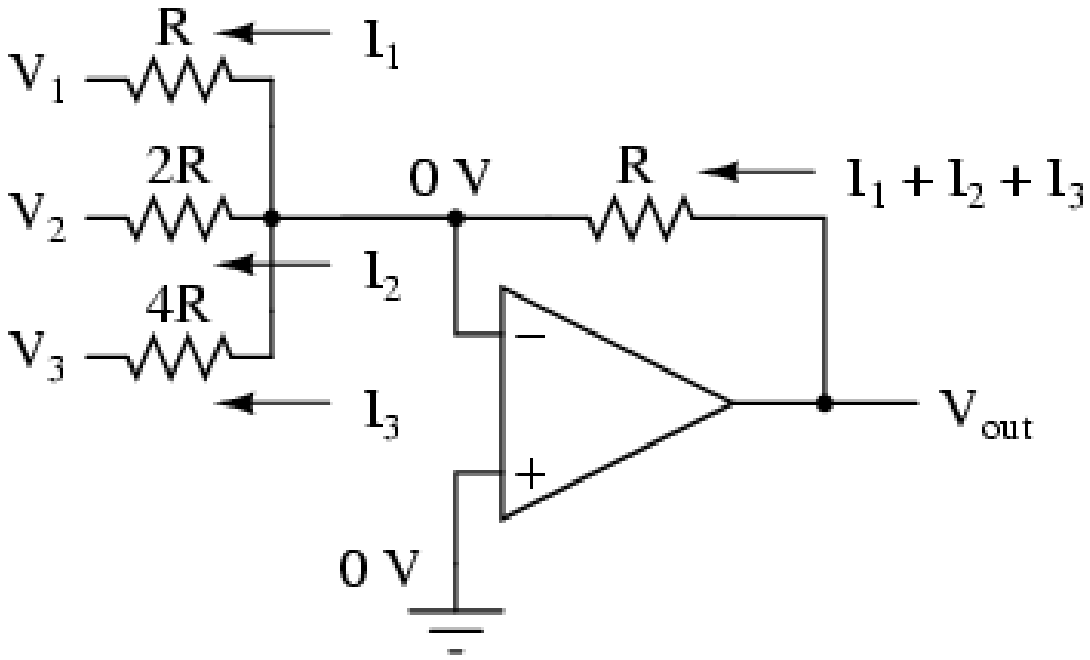
Vout =

Inverting summer circuit



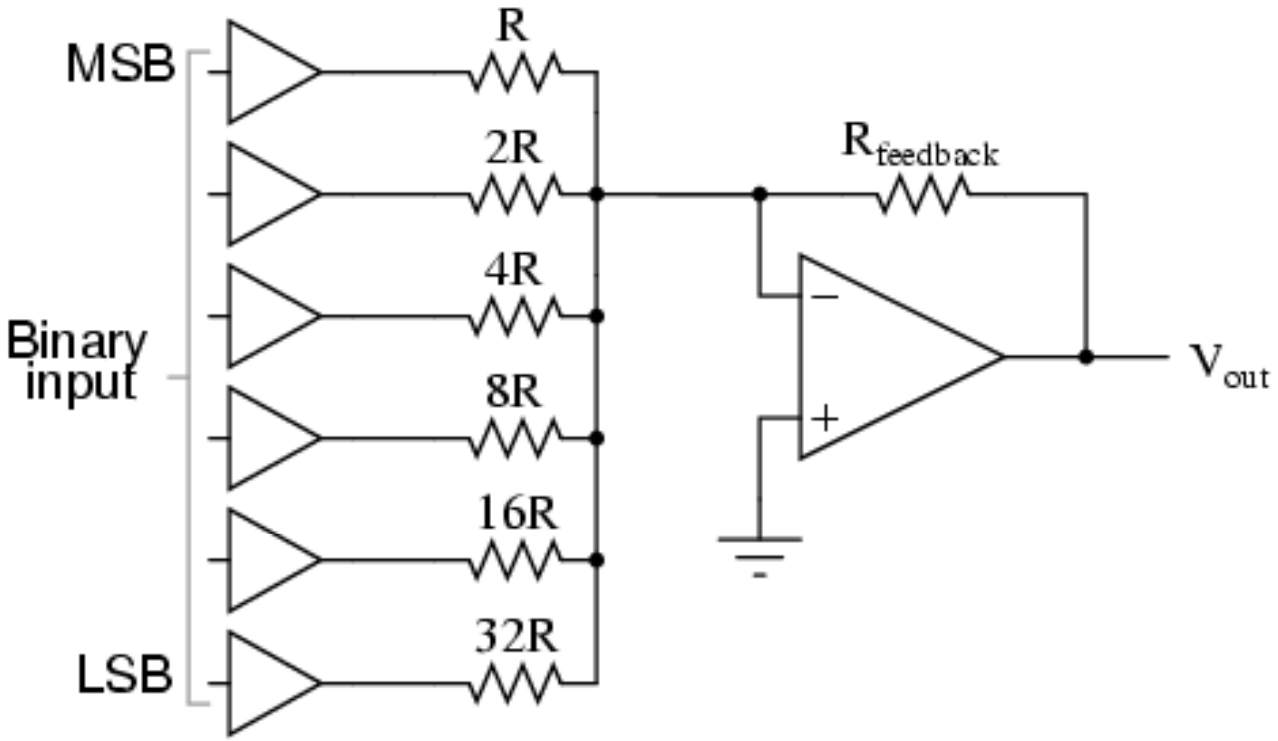
$$V_{out} = - (V_1 + V_2 + V_3)$$

DAC with Weighted Sum

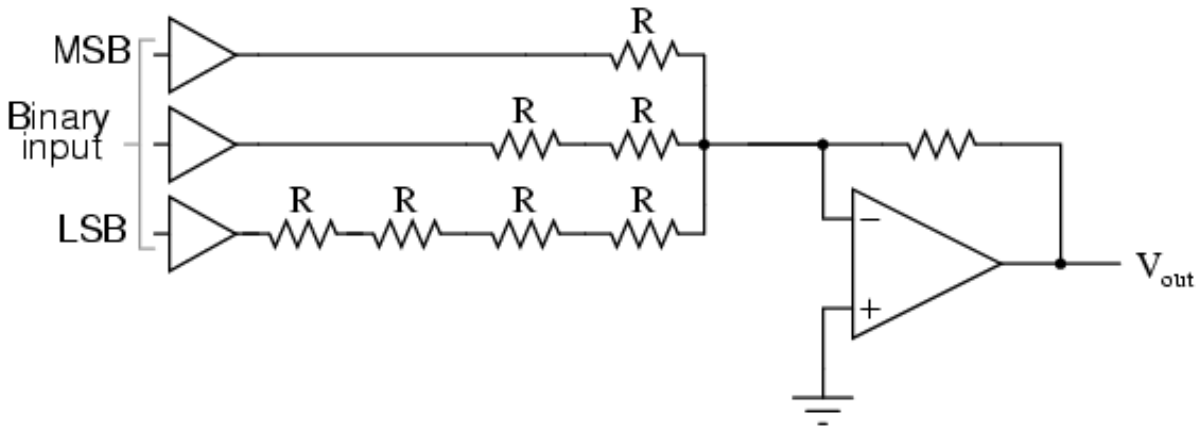


$$V_{out} = -\left(V_1 + \frac{V_2}{2} + \frac{V_3}{4}\right)$$

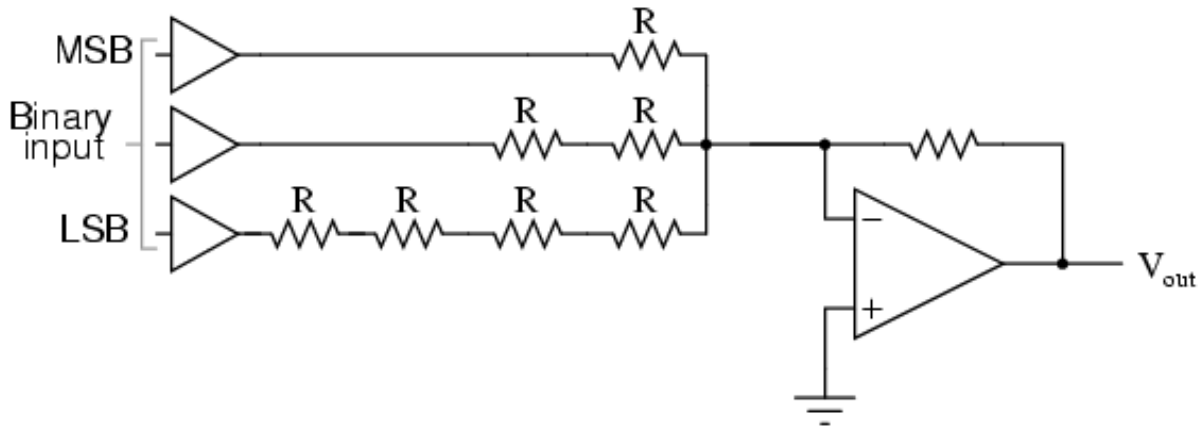
6-bit binary-weighted DAC



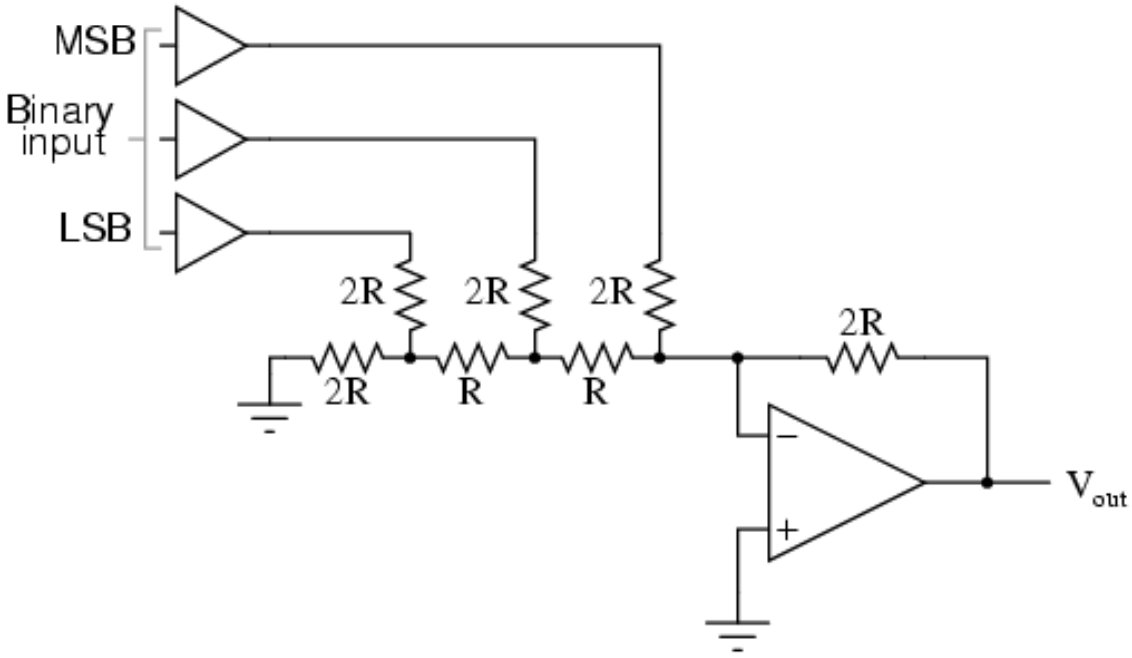
Binary Weighted DAC

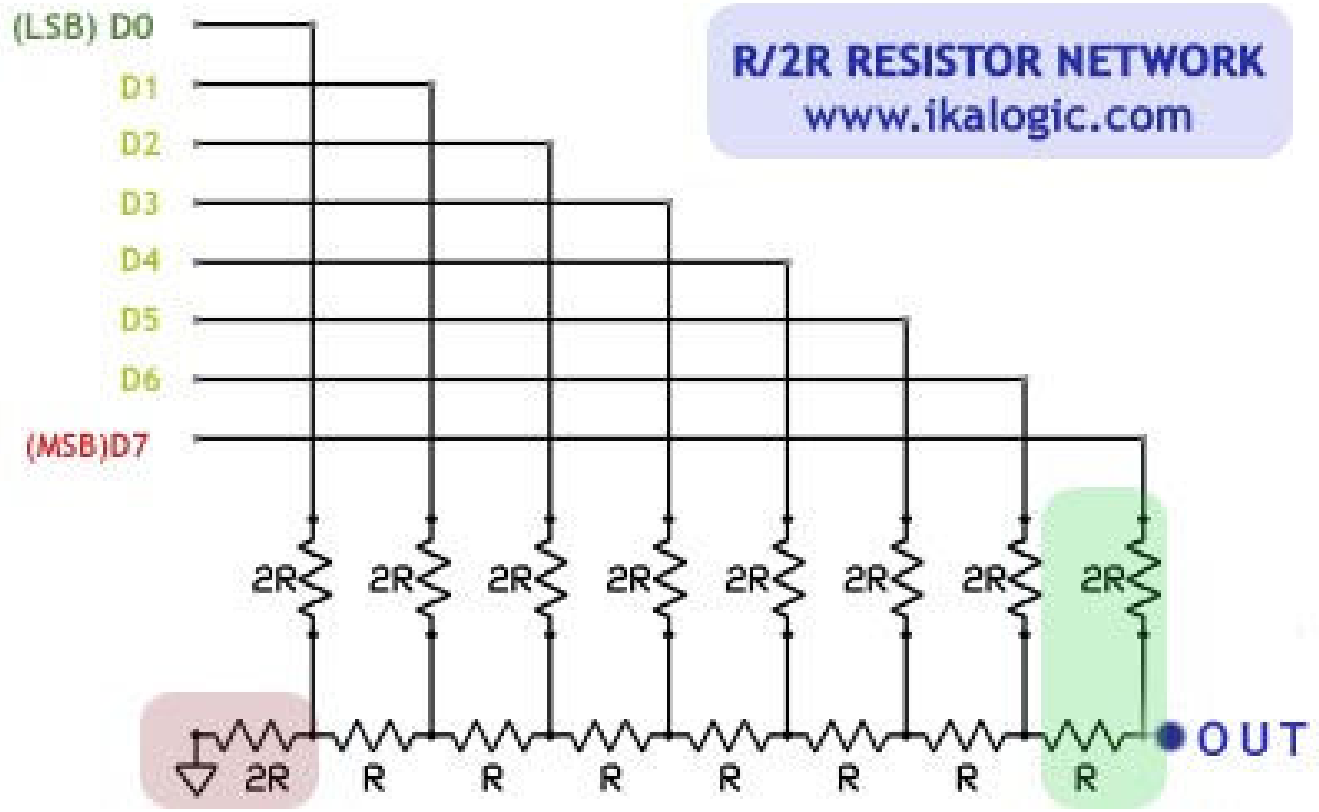


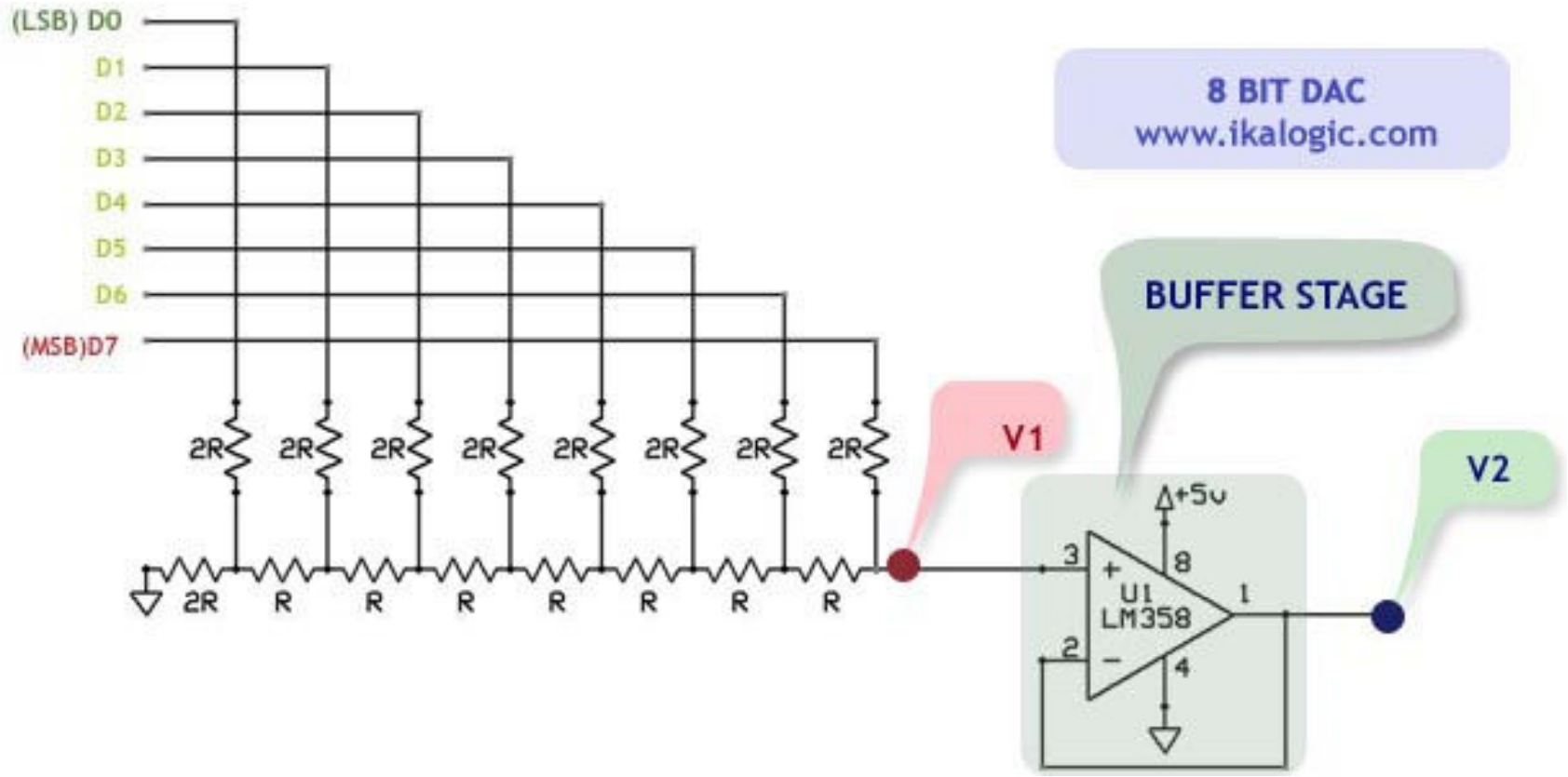
Binary Weighted DAC

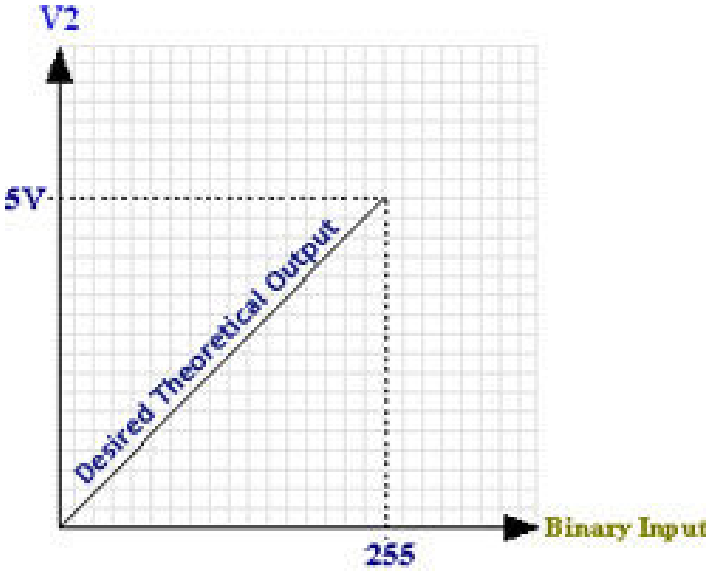


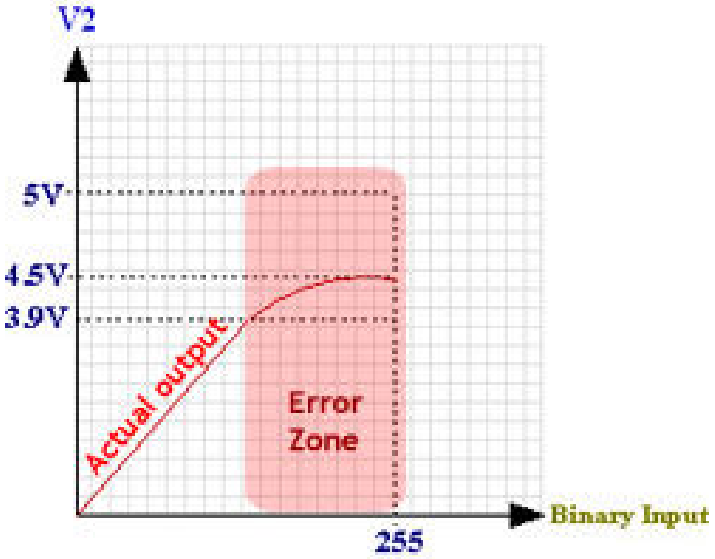
R/2R "ladder" DAC




R/2R RESISTOR NETWORK
www.ikalogic.com
(LSB) D0
D1
D2
D3
D4
D5
D6
(MSB)D7
2R
2R
2R
2R
2R
2R
2R
2R
2R
R
R
R
R
R
R
R
OUT


(LSB) D0
D1
D2
D3
D4
D5
D6
(MSB)D7
2R
R
8 BIT DAC
www.ikalogic.com
BUFFER STAGE
V1
V2
+5v
U1
LM358



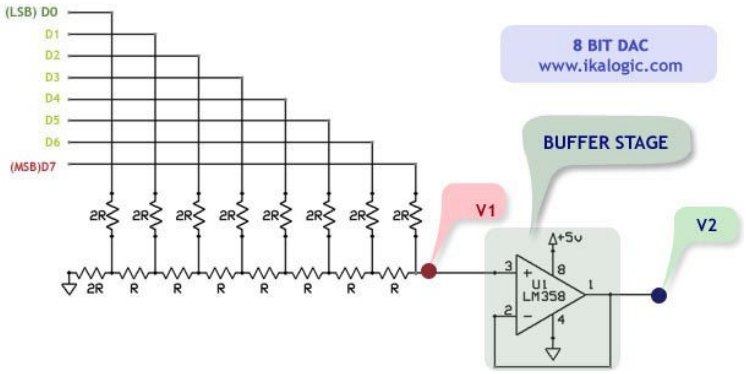


8 BIT R/2R DAC performance
www.ikalogic.com

DAC Implementation

Table 30.1 Summary of experimental results.

	8-bit	10-bit	12-bit
DNL (LSB)	0.150	0.450	2.000
INL (LSB)	0.200	1.000	3.000
Settling time	200 ns		
Power	3.88 mW (driving a 1k load)		
Area (mm^2)	0.045		
$f_{clk,\max}$	4 MHz		
Output swing	$0 < V_{out} < VDD\ (= 1.8\ V)$		



DAC Implementation

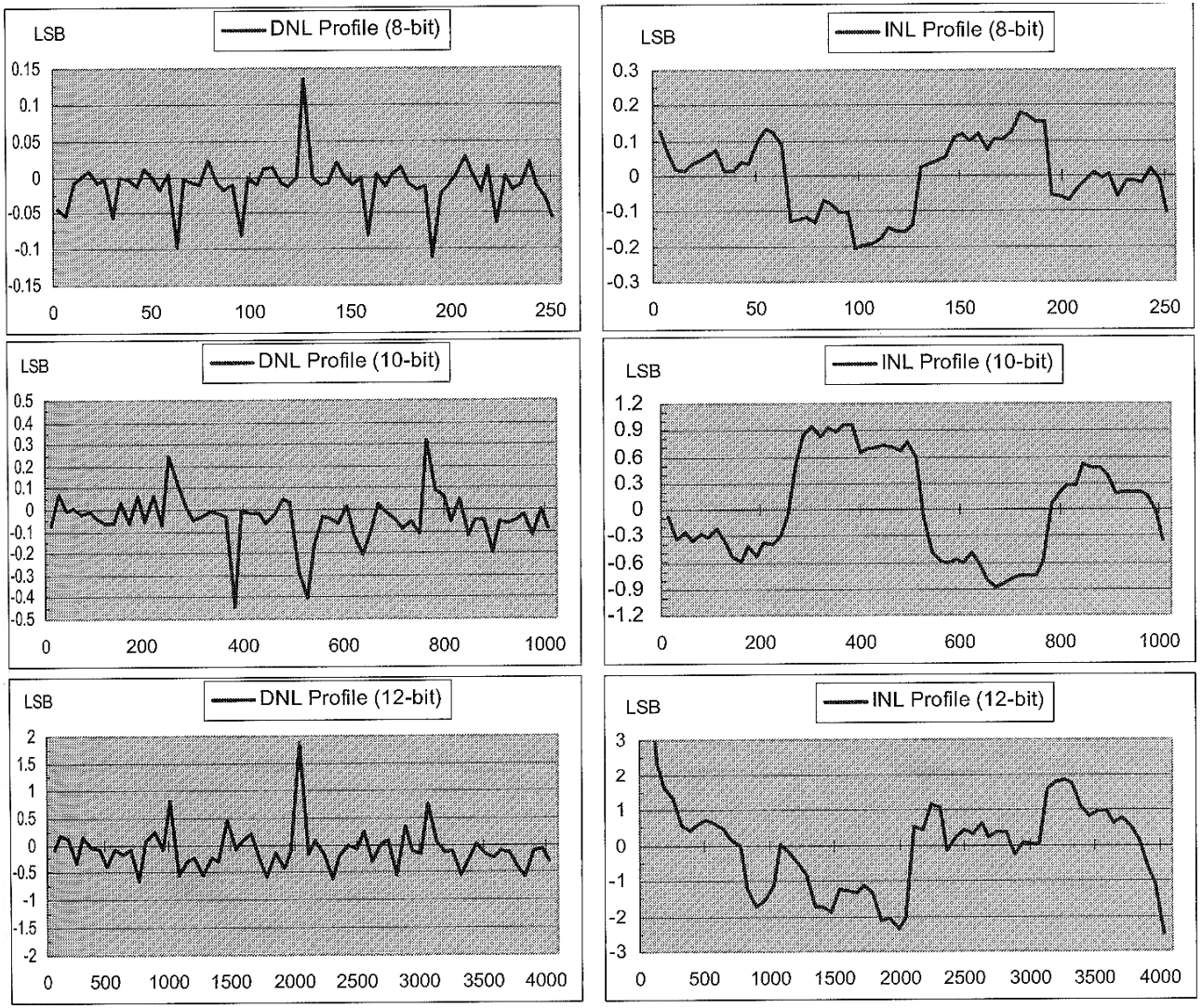


Figure 30.4 Experimental results for the wide-swing DAC of Fig. 30.3.

Pipeline DAC

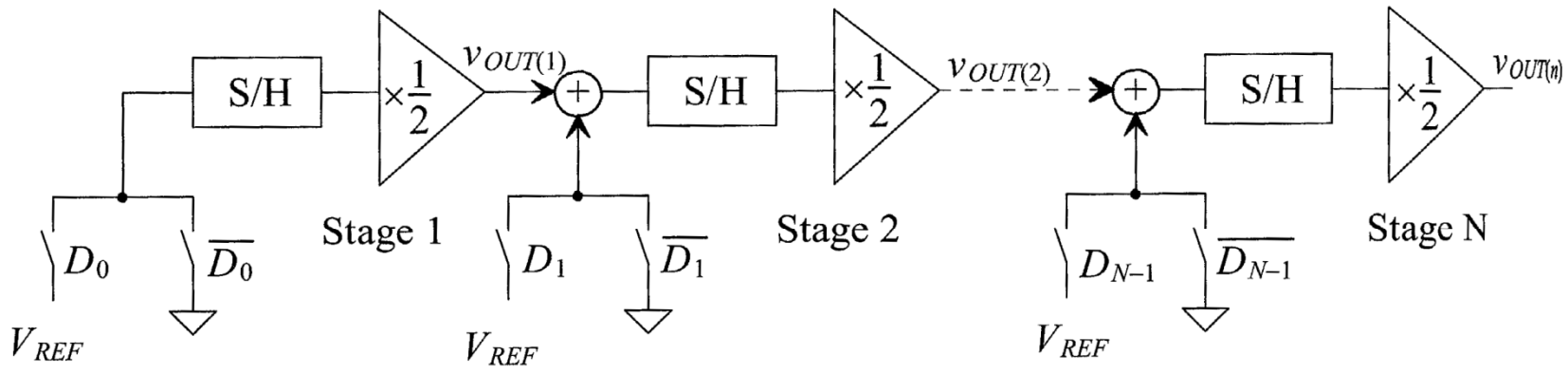


Figure 29.19 A pipeline digital-to-analog converter.

Digital to Analog Converter