CMPEN 411
VLSI Digital Circuits
Spring 2012

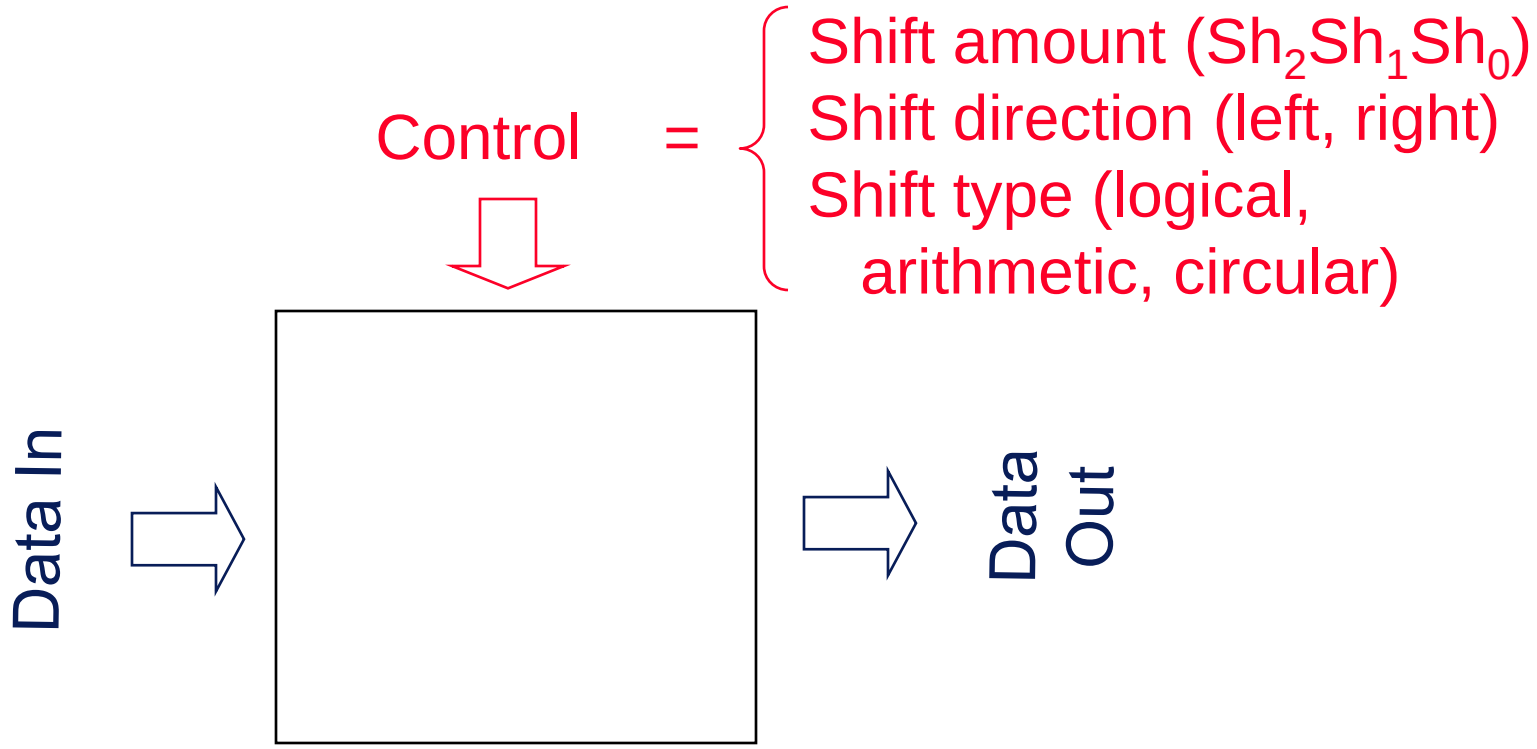
Lecture 21: Shifters, Decoders, Muxes

[Adapted from Rabaey's *Digital Integrated Circuits*, Second Edition, ©2003 J. Rabaey, A. Chandrakasan, B. Nikolic]

Review: Basic Building Blocks

- Datapath
  - Execution units
    - Adder, multiplier, divider, shifter, etc.
  - Register file and pipeline registers
  - Multiplexers, decoders
- Control
  - Finite state machines (PLA, ROM, random logic)
- Interconnect
  - Switches, arbiters, buses
- Memory
  - Caches (SRAMs), TLBs, DRAMs, buffers

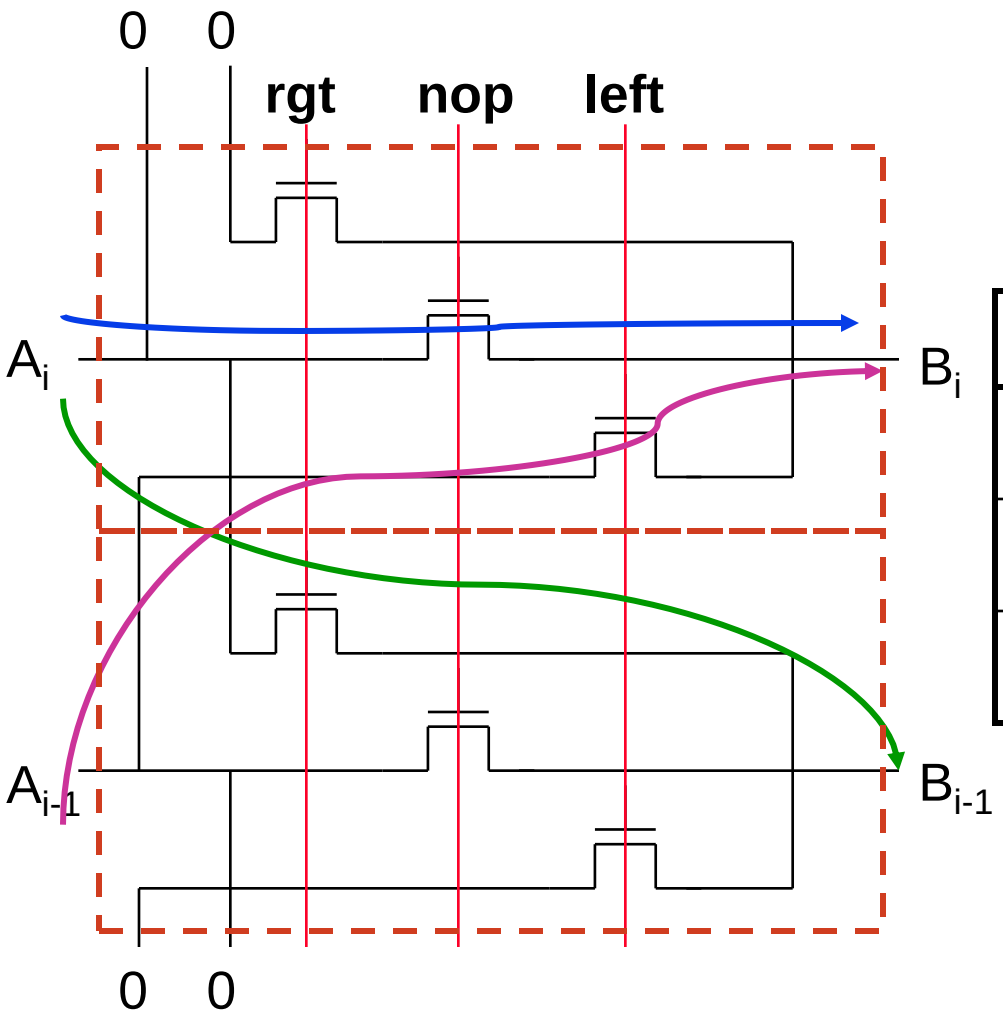
Parallel Programmable Shifters



Shifters used in multipliers, floating point units

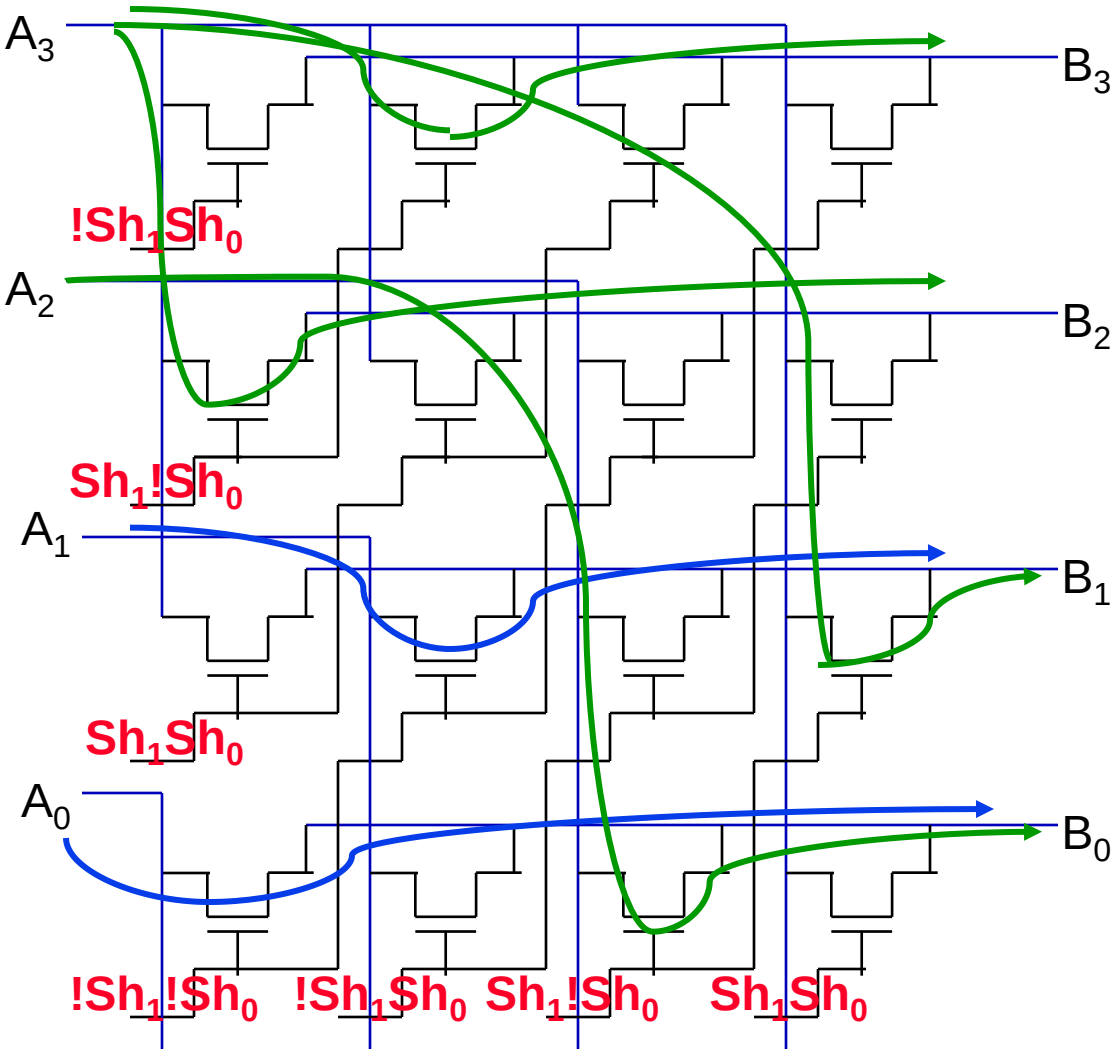
Consume lots of area if done in random logic gates

A Programmable Binary Shifter



A_i	A_{i-1}	rgt	nop	left	B_i	B_{i-1}
A_1	A_0	0	1	0	A_1	A_0
A_1	A_0	1	0	0	0	A_1
A_1	A_0	0	0	1	A_0	0

4-bit Barrel Shifter



Example:

$!Sh_1!Sh_0 = 1$

$B_3B_2B_1B_0 = A_3A_2A_1A_0$

$!Sh_1Sh_0 = 1$

$B_3B_2B_1B_0 = A_3A_3A_2A_1$

$Sh_1!Sh_0 = 1$

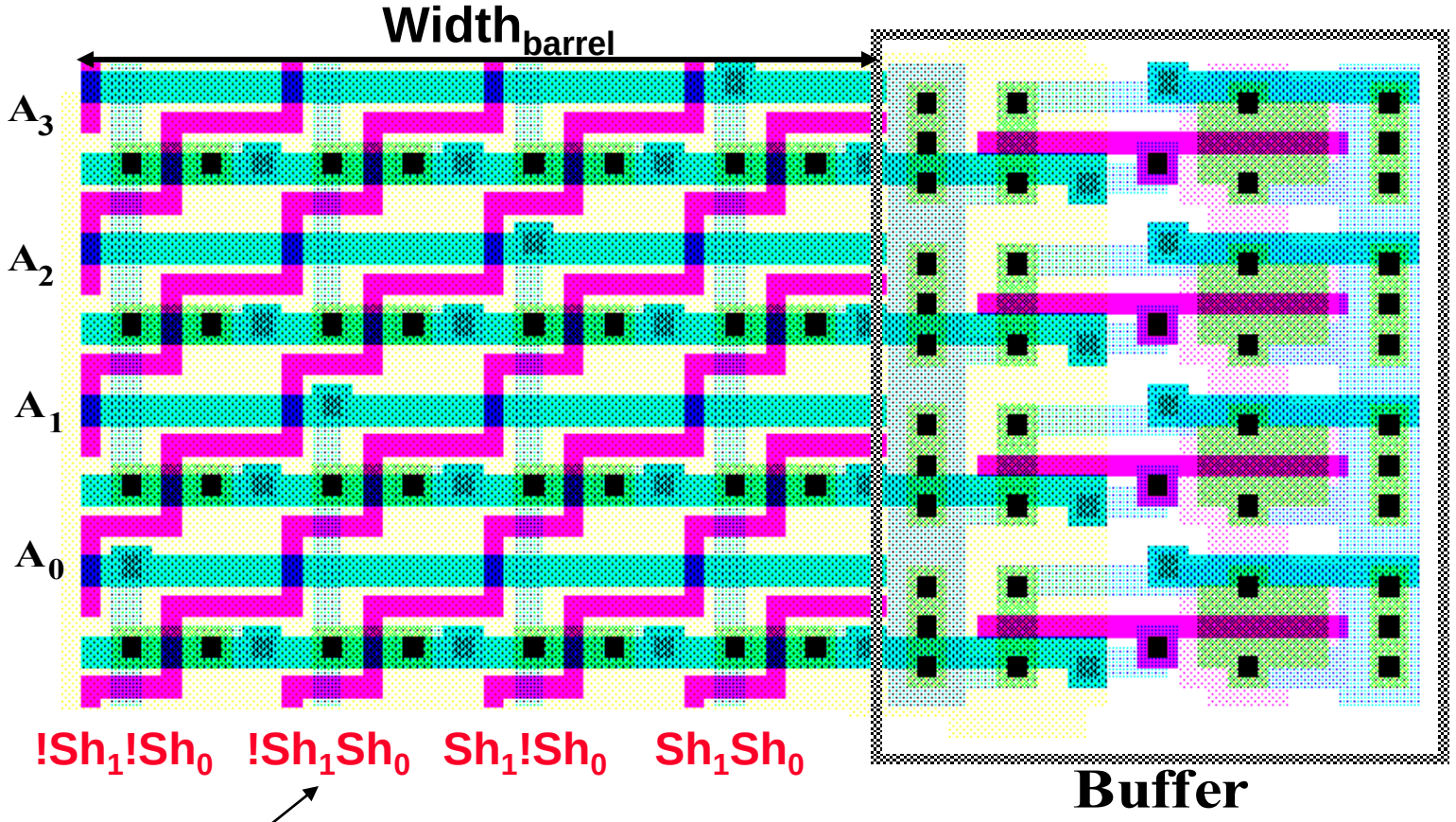
$B_3B_2B_1B_0 = A_3A_3A_3A_2$

$Sh_1Sh_0 = 1$

$B_3B_2B_1B_0 = A_3A_3A_3A_3$

Area dominated by wiring

4-bit Barrel Shifter Layout

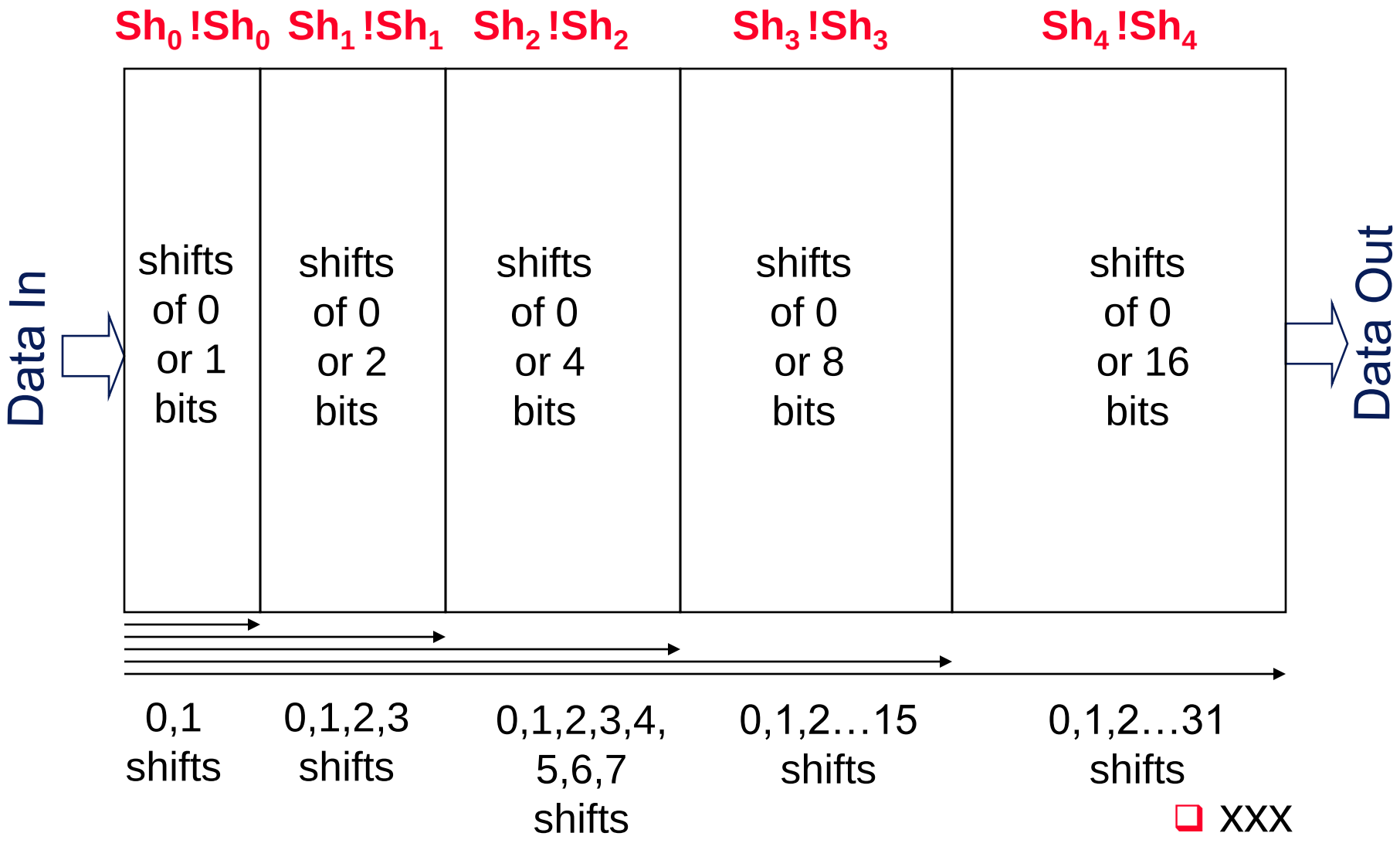


Only one Sh# active at a time

Width$_{barrel}$ ~ O(N)

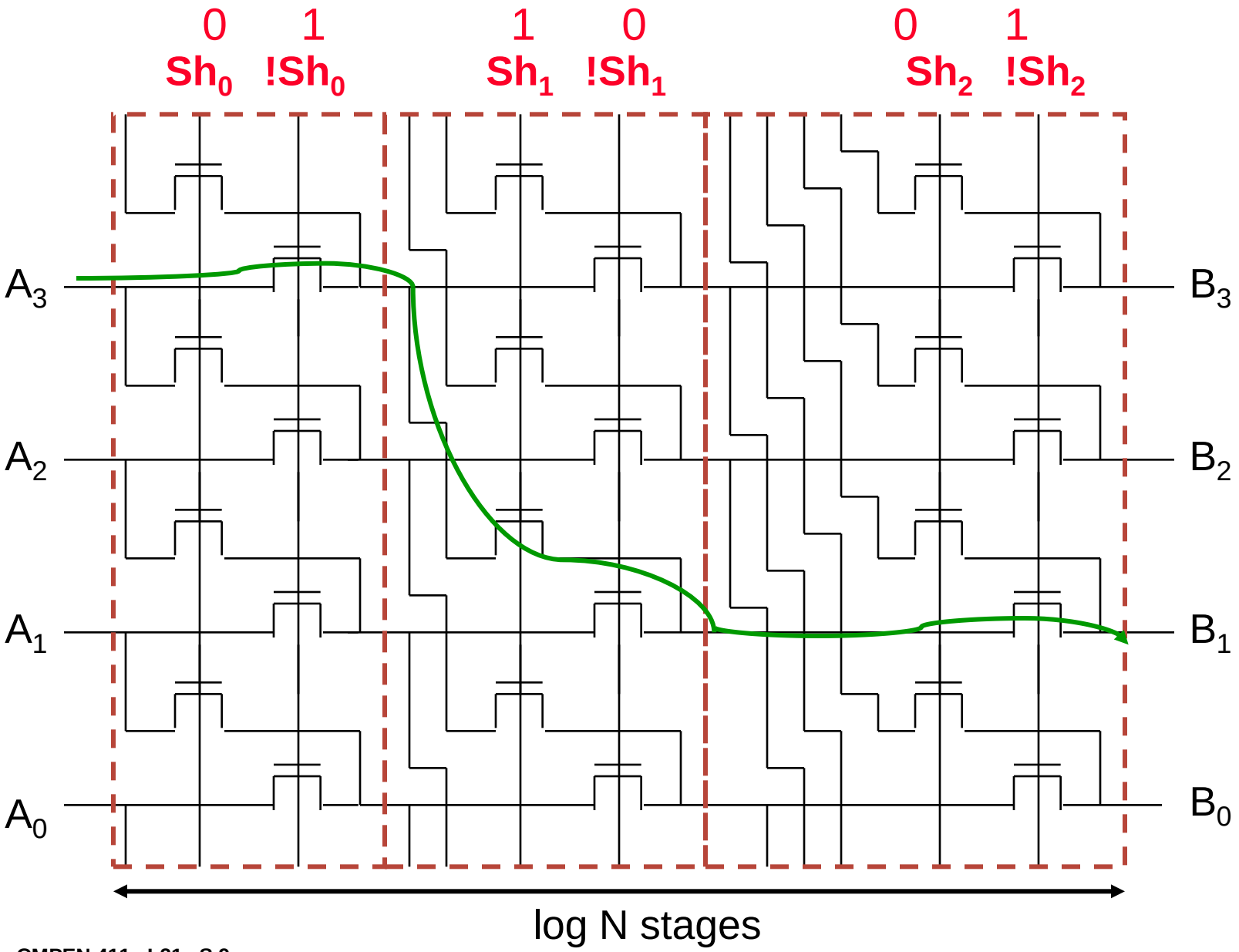
Delay ~ 1 fet + N diff caps

Logarithmic Shifter Structure

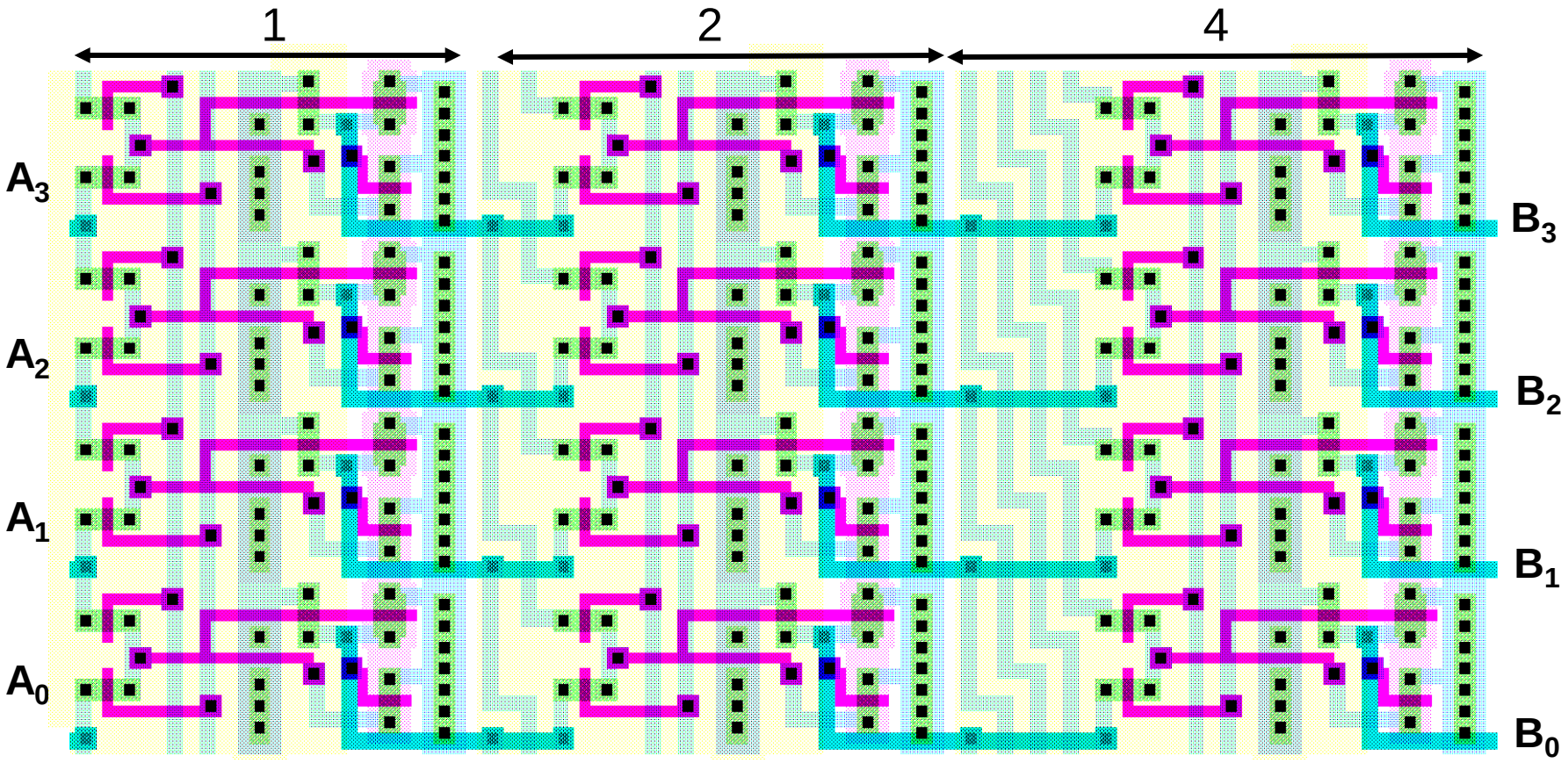


- XXX

8-bit Logarithmic Shifter



8-bit Logarithmic Shifter Layout Slice



$K = \log_2 N$

Delay ~ K fets + 2 diff caps

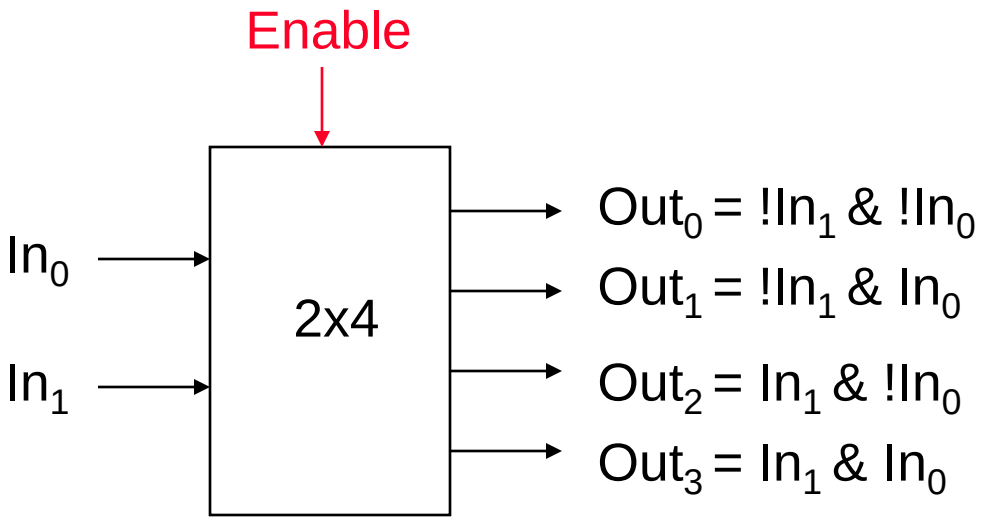
Shifter Implementation Comparisons

N	K	Barrel		Logarithmic	
		Width	Speed	Width	Speed
		2 N p_m	1 + N diffs	$p_m(2^K+2K-1)$	K + 2 diffs
8	3	16 p_m	1 + 8	13 p_m	3 + 2
16	4	32 p_m	1 + 16	23 p_m	4 + 2
32	5	64 p_m	1 + 32	41 p_m	5 + 2
64	6	128 p_m	1 + 64	75 p_m	6 + 2

Barrel shifter needs an K x 2^K shift amount decoder

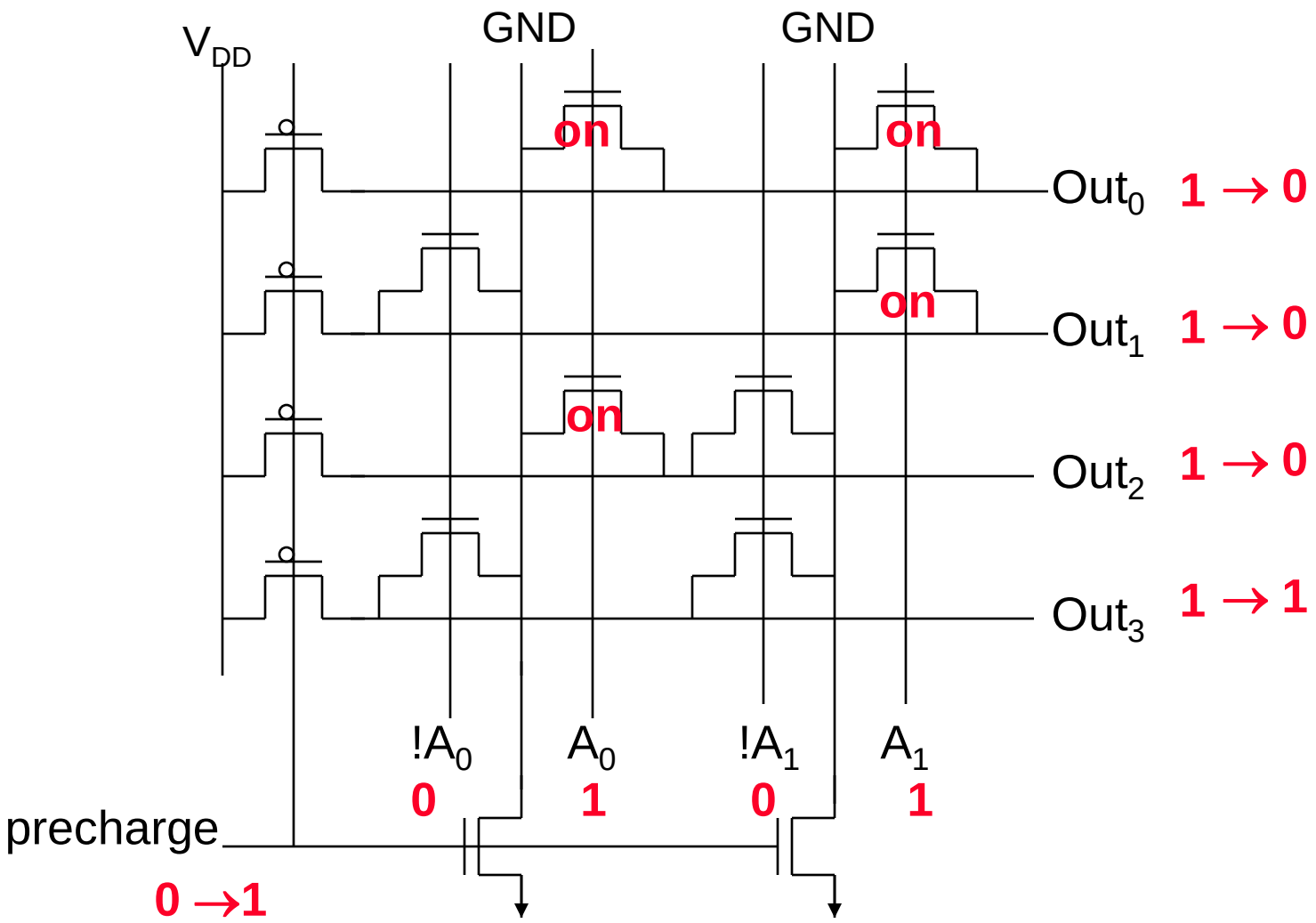
Decoders

- Decodes inputs to activate one of many outputs

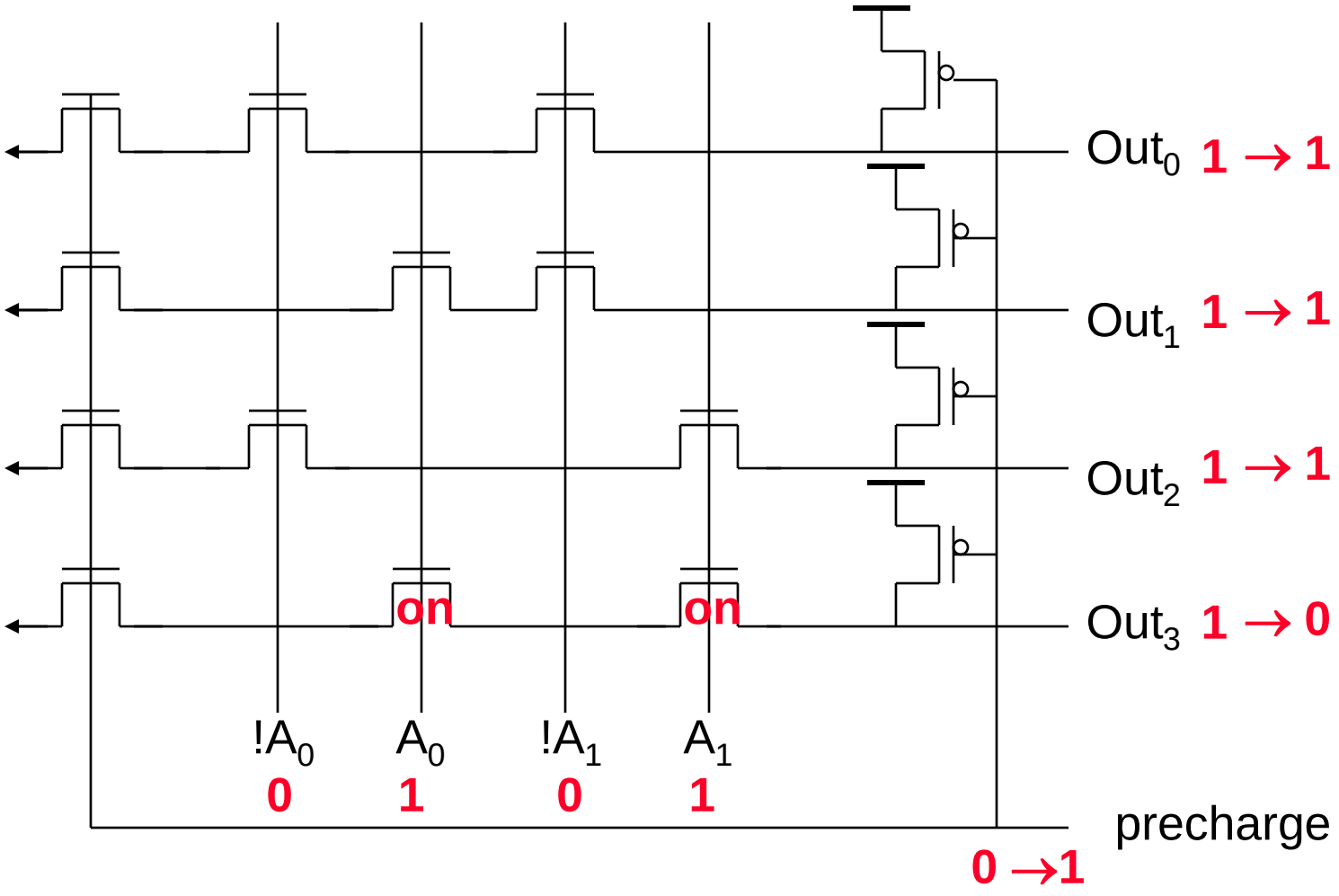


  - In random gate logic need two inverters, four 2-input nand gates, four inverters plus enable logic
  - how about for a 3-to-8, 4-to-16, etc. decoder?

Dynamic NOR Row Decoder

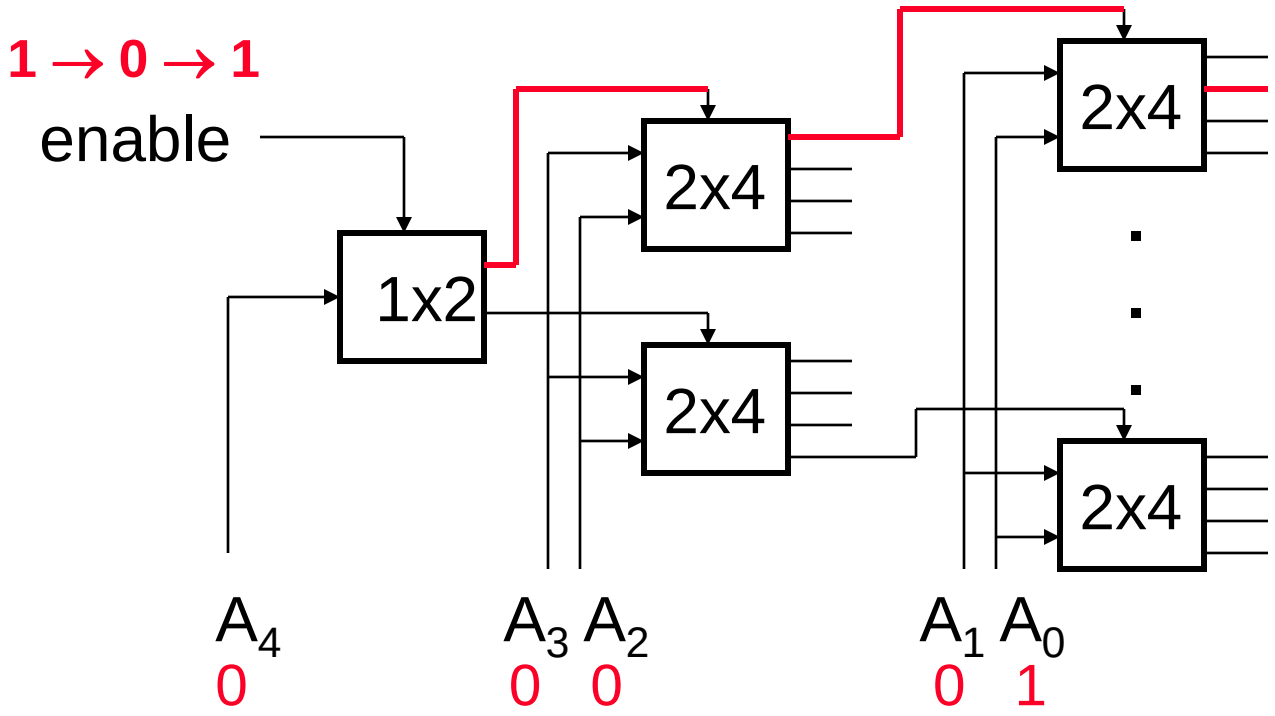


Dynamic NAND Row Decoder



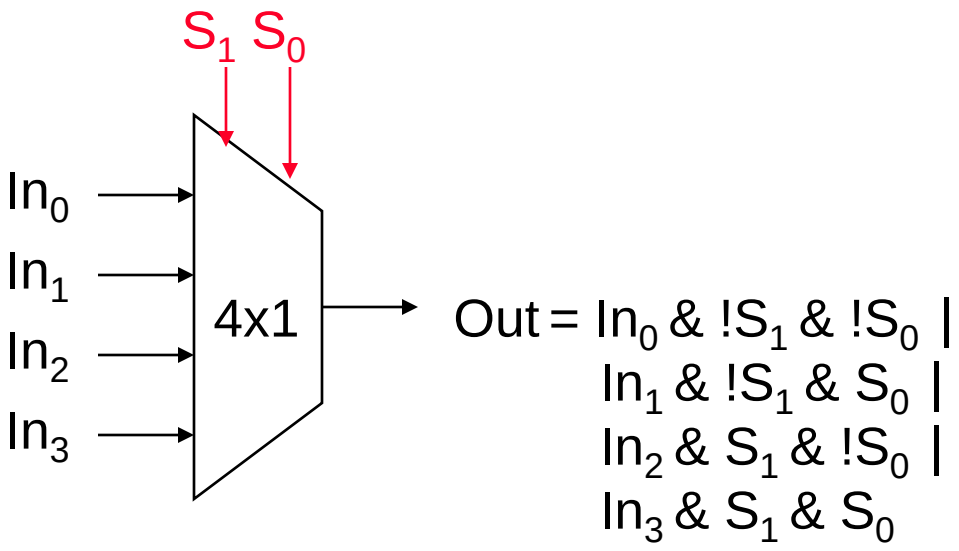
Building Big Decoders from Small

Active low enable
Active low output



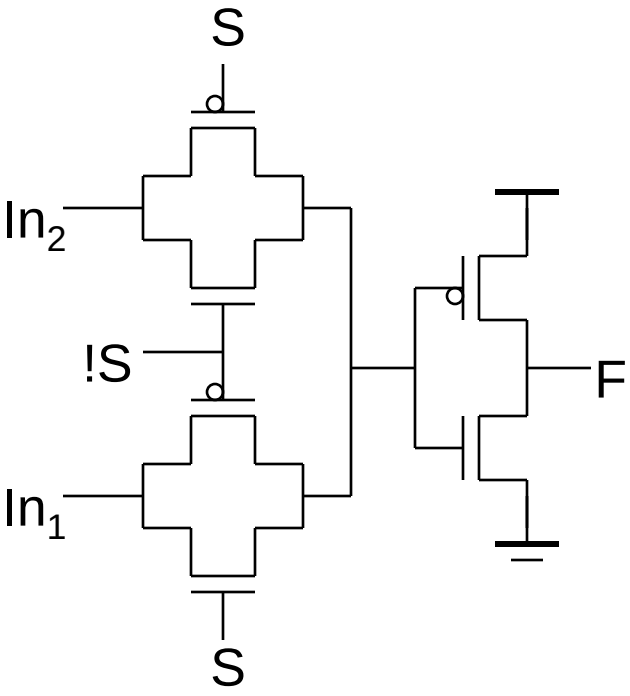
Multiplexers

- Selects one of several inputs to gate to the single output

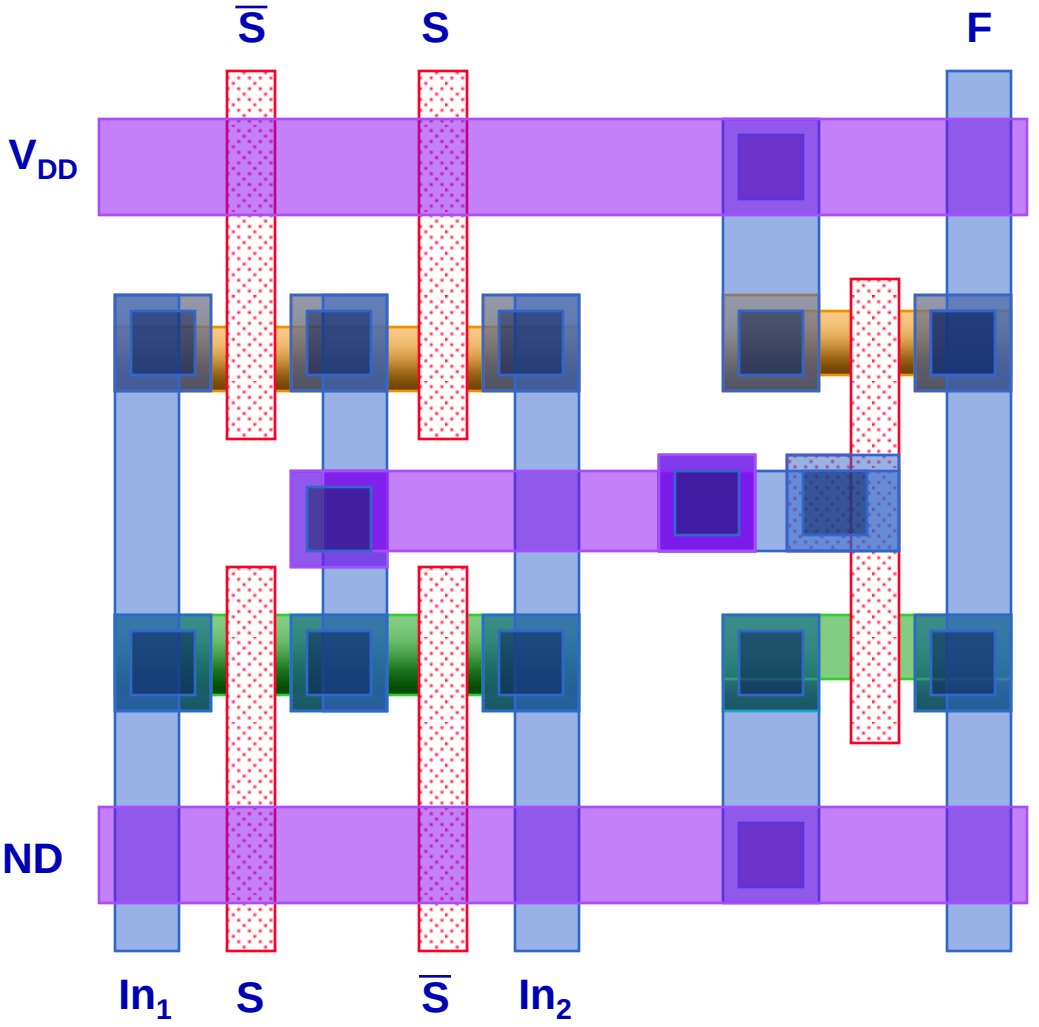


- In random gate logic need two inverters, four 3-input nands, one 4-input nand
- how about for an 8x1, 16x1, etc. mux?

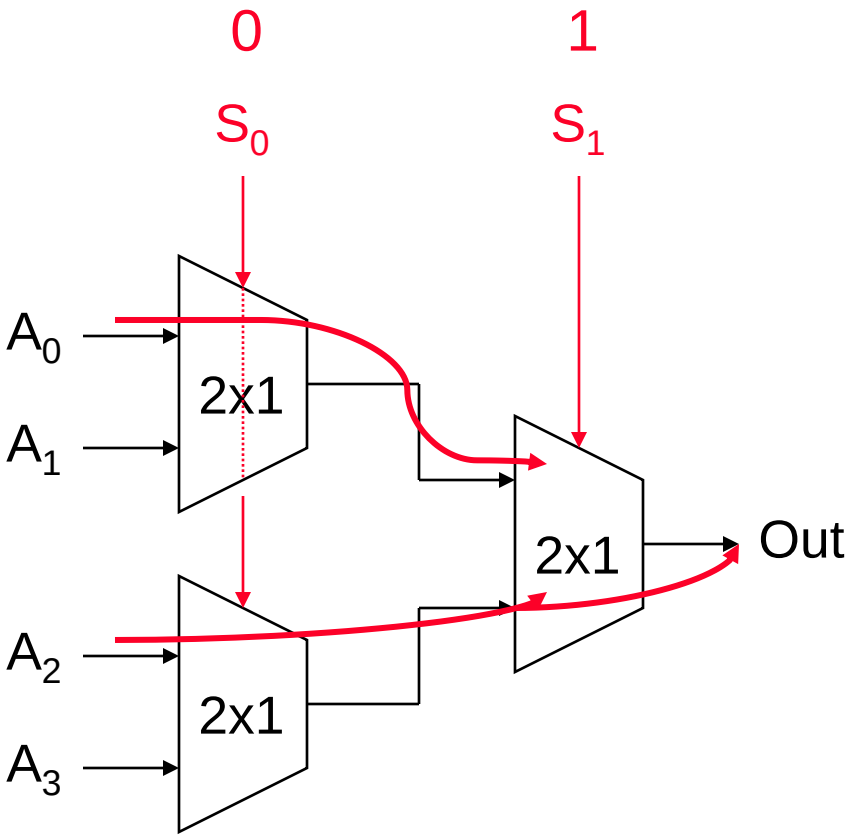
Review: TG 2x1 Multiplexer



$F = !((In_1 \& S) \mid (In_2 \& !S))$



Building Big Muxes from Small



Next Lecture and Reminders

- Next lecture
  - SRAM, DRAM, and CAM cores
    - Reading assignment – Rabaey, et al, 12.1-12.2.4