1st Workshop on SoC Architecture, Accelerators and Workloads (SAW-1)

Jan 10th 2010, Bangalore India

Held in conjunction with HPCA-16

Organizing Chairs:

Ravi Iyer	Intel Labs	ravishankar.iyer@intel.com
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Advance Program:

9:00	***9:15***	***Welcome to SAW 2010***		
9:15	9:50	Opening remarks - The future of SoCs	Raj Yavatkar	Intel Corporation
9:50	10:30	Smart Phones – Future Devices, Usages and Applications *(Invited talk)*	Roy Want	Intel Labs
10:30	11:00	Break		
11:00	11:25	A Bio-Inspired Framework for Secure System on Chip	Ayan Mandal, Suman K. Mandal, Aalap Tripathy and Rabi Mahapatra	Texas A&M University
11:25	11:50	Performance Characterization and Optimization of Optical Character Recognition on Handheld Platforms	Sadagopan Srinivasan, Li Zhao, Zhen Fang, Don Newell	Intel Labs, USA
11:50	12:15	A Software Power Characterization of Video Playback on Mobile Internet Devices	Padma Apparao, & Pramod Pesara	Intel Corporation
12:15	1:30	Lunch break		
1:30	2:10	Open Core Protocol: An Introduction to Interface Specification *(Invited talk)*	Prashant Karandikar	Texas Instruments
2:10	2:35	Ocin_sim - a DVFS aware simulator for NoC based platforms	Subodh Prabhu, Boris Grot, Paul V. Gratz and Jiang Hu	Texas A&M University
2:35	3:00	Stream and Memory Hierarchy Design for Multi-Purpose Accelerators	Sylvain Girbal, Sami Yehia, Hugues Berry, Olivier Temam	Thales Research and Technology; INRIA Saclay; France
3:00	3:30	Break		
3:30	4:10	Systems on Reconfigurable Platforms: Design Successes and Challenges *(Invited talk)*	Vijaykrishnan Narayanan	Penn State University
4:10	4:35	MoonRidge: An automated design framework for workload-optimized power-efficient reconfigurable accelerators	Sergey Yakoushkin, Alexandr Redkin, Anthony L. Chun	Intel Labs, Russia
4:35	5:00	Using Reconfigurable Logic to replace Fixed-Function Blocks in SoCs	Tao Wang, Peng Li, Yuan Liu, Zhiyuan Zhang, Angshuman Parashar, Azam Barkatullah, Dong Liu, Joel S. Emer	Intel Corporation