Sample & Hold Circuits

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Basic Sample and Hold Circuit Configuration

- **Concept**

- **MOSFET S&H Circuit**
Design Issues of CMOS S&H

- Sampling Moment Distortion
  - Finite Clock rising/falling time results in distortion

- Clock Feed-through
  - Overlap cap. of MOS Switch creates an sampling error during clock transition time

- MOS Switch Charge Injection
  - Some charge in the MOS channel flow to Source and Drain, then result in an error.
    - \( \Delta Q = C_{ox}(V_{GS} - V_{Th}) \), \( \Delta V_{hold} = \frac{\Delta Q}{C_H} \)
Solutions for Reducing Sampling Distortion

- **Differential S&H Circuit**

- **Sample Clock Bootstrapping**
  - Sampling distortion can be reduced by increasing clock amplitude
Sample Clock Bootstrap Circuits (I)

- Basic clock bootstrap circuit

Simulation Result
Sample Clock Bootstrap Circuits (II)

- Differential sampling clock bootstrap circuit

![Diagram of differential sampling clock bootstrap circuit]

Simulator Result

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Signal Dependent Clock Bootstrapping (I)

- The problem of clock bootstrap circuit
  - $V_{gs}$ of MOS switch can vary according to the input voltage level
  - $Ron$ of MOS Switch also vary
  - It can cause an error in holding voltage

- Signal Dependent clock bootstrap circuit
Signal Dependent Clock Bootstrapping (II)

- Modified Circuit
Low Signal Feed-through Switch

- Schematic

Simulation Result

Offset: 30 mV

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Charge injection Compensation Switch (I)

Simulation Result

Offset: 2.5 mV

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Charge injection Compensation Switch (II)

Offset: 0.72 mV

Simulation Result

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Actual Implementation S&H Circuits
Double Buffered S&H Configuration

Advantages:
- Obtain a low droop rate during holding mode
- Stability is determined by the stabilities of OP Amps

Disadvantages:
- OP Amps offset can constrain the accuracy of SHA
Double Buffered S&H Circuit with CMOS Switch

- Schematic

Clock Bootstrap Circuits
Double Buffered S&H Circuit with CMOS Switch

Simulation Result

Input
Output

VSS (-1.65V)

VDD (1.65V)
Feedback Improved S&H Circuit

Advantages:
- Offset free → More accurate than double buffered SHA

Disadvantages:
- Common Mode Rejection of the Input OP amp must be high
- Special Care must be taken to obtain stability of SHA
- Needs a special circuitry to stabilize the input amplifier during the holding mode

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Simple stabilization circuit for input amplifier
(cont’d) Feedback Improved S&H Circuit

Feedback improved S&H w/o input amp stabilization

Feedback improved S&H with input amp stabilization

Simulation Result

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Integrating S&H Circuit

Advantages:
- Switching moment and charge feed-through can be controlled very well

Disadvantages:
- Common Mode Rejection of the Input OP amp must be high
- Special Care must be taken to obtain stability of SHA
- Needs a special circuitry to stabilize the input amplifier during the holding mode
S&H Circuit using Miller Cap.
Switched Capacitor S&H Circuit

- Basic Configuration

- Common implementation for pipelined ADCs
References
