Current Source & Bias Circuits

Insoo Kim, Kyusun Choi
Mixed Signal CHIP Design Lab.
Department of Computer Science & Engineering
The Pennsylvania State University
Introduction

- Required Features of Current Source
  - High Rout
  - Wide Operation Range
  - Constant Current Source
  - Low PVT (Process, Voltage, Temperature) Sensitivity

- Required Features of Bias Circuit
  - Low Rout
  - Low PVT Sensitivity
Current Source

- Basic Current Source
- Wilson Current Mirror
- Cascode Current Mirror
**Ideal vs. Actual Current Source**

- **Ideal Current Source**

  ![Ideal Current Source Diagram]

  Output current should be independent of an output voltage.

- **Actual Current Source**

  ![Actual Current Source Diagram]

  ✓ Operating Range

  => Large Signal Analysis

  ✓ Output Resistance $R_{out}$

  => Small Signal Analysis

2/22/2011

Insoo Kim
Simple NMOS Current Source

- **Operating Range**

\[ I_{DS\text{(sat)}} = \frac{\beta}{2} (V_{GS} - V_{TH})^2 = \frac{\beta}{2} \Delta^2 \]

\[ V_{out} \geq \Delta = \sqrt{\frac{2 \cdot I_{DS\text{(sat)}}}{\beta}} \]

\[ V_{CC\text{(sat)}} = V_{GS} - V_{TH} = V_{B} - V_{TH} \]

- **Output Resistance**

\[ R_{out} = \frac{V_x}{I_x} = r_o = \frac{1}{g_o} \]

What’s the bad feature of this?
What's the bad feature of this?
Basic Current Mirror

- \( M_1 \): Current Input
- \( M_2 \): Current Output
- For Ideal Matching of \( M_1 \) & \( M_2 \), \( I_1 = I_2 \)
- Operating Range: Down to \( \Delta \)
- Output Resistance: \( R_{out} = r_{o2} \)

Mismatch Problem

\[
\frac{I_{out}}{I_{in}} = \frac{(1/2)\mu_n C_{ox} (W/L)_2 (V_{GS} - V_{TH2})^2 (1 + \lambda V_{DS2})}{(1/2)\mu_n C_{ox} (W/L)_1 (V_{GS} - V_{TH1})^2 (1 + \lambda V_{DS1})}
\]

- \( \checkmark \) transistor size \( W/L \)
- \( \checkmark \) threshold voltage
- \( \checkmark \) \( V_{DS} \)

What’s the bad feature of this?
**Wilson Current Mirror**

- **Output Resistance**: \( R_{\text{out}} = (g_m r_0) r_{02} \)
- **Operating Range**: Down to \( V_{\text{TH}} + 2\Delta \)
- **V_{\text{DS}} Mismatch?**
  \[
  V_{\text{DS1}} = V_{\text{GS3}} + V_{\text{GS2}} = V_{\text{GS3}} + V_{\text{DS2}} > V_{\text{DS2}}
  \]
- **I_{\text{out}}**:
  \[
  I_{\text{out}} = I_{\text{ref}} \cdot \frac{g_{m1}}{g_{m2}} = I_{\text{ref}} \cdot \frac{(W / L)_1}{(W / L)_2}
  \]
- **Improved Version**
- **Same Performance but**
  \[
  V_{\text{DS1}} = V_{\text{GS3}} + V_{\text{GS2}} - V_{\text{GS4}} = V_{\text{GS3}} + V_{\text{DS2}} - V_{\text{GS4}} \approx V_{\text{DS2}}
  \]

What’s the drawback of this circuit?

---

2/22/2011

Insoo Kim
Cascode Current Mirror

- Output Resistance: \( R_{\text{out}} = (g_{m3}r_{o3})r_{o2} \)
- Operating Range: Down to \( V_{\text{TH}}+2\Delta \)
- \( V_{\text{DS}} \) Mismatch Avoided
  \( V_{\text{DS1}} = V_{\text{GS4}} - V_{\text{GS3}} + V_{\text{DS2}} \approx V_{\text{DS2}} \)

But, it still has limited output swing problem.

- Output Resistance: \( R_{\text{out}} = (g_{m}r_{o})r_{o} \)
- Operating Range: \( 2\Delta \)
- \( V_{\text{DS}} \) Mismatch?
  \( V_{\text{TH}} + \Delta \neq \Delta \)
Wide Swing Cascode Current Mirror

\[ V_{G2} = 2\Delta + V_{TH} \]
\[ V_{G1} = \Delta + V_{TH} \]
\[ V_{GS5} = \Delta + V_{TH} \]
\[ V_{GS2} = \Delta + V_{TH} \]

\[ V_{DS3} = V_{G2} - V_{GS5} = \Delta \]
\[ V_{DS5} = V_{G1} - V_{DS3} = V_{TH} \]
\[ V_{DS1} = V_{G2} - V_{GS2} = \Delta \]

\[ I_{out} = I_{ref} \]

Current gain = 1
Bias Circuits

- Self Bias Circuits
- PTAT Bias Circuits
- Band gap Reference
Power Supply Dependency of Current Source

Consideration Factors
- VDD
- Channel Length Modulation
- Transistor Mismatch

\[ \Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1} \]

How do we generate Iref independent of the supply voltage?

2/22/2011
Insoo Kim
What’s the advantage of these circuits?

What’s the problem of these circuits?

What’s role of Rs?

\[ I_{out} = K I_{REF} \]

\[ V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox} (W/L)_N}} + V_{TH2} + I_{out} R_S \]

\[ I_{out} = \frac{2}{\mu_n C_{ox} (W/L)_N} \cdot \frac{1}{R_S} \left(1 - \frac{1}{\sqrt{K}}\right)^2 \]
Improved Self Biasing Circuit

Improved Circuit eliminating Body Effect

Improved Circuit with Start-up Circuit

* This Circuit is practical only if

1. $V_{TH1} + V_{TH5} + |V_{TH3}| < V_{DD}$
2. $V_{GS1} + V_{TH5} + |V_{GS3}| > V_{DD}$
A Simple Temperature Compensation Concept

1. R1 is a conductor which has positive TC
2. M1 has negative TC below ZTC point (Semiconductor)
3. If we control Vr0 below ZTC point, Vr0 become less sensitive to temperature due to opposite TC of M1 and R1
What’s the drawback of these circuits?
Why does this circuit need the voltage buffer?
Why are PMOS current mirrors stacked in the reference bias circuit?
VBE Referenced CMOS Self-bias Circuit

How do we fabricate BJT in CMOS Process Technology?

\[ V_R = V_{EB1} \]

\[ I_2 \cdot R = V_T \cdot \ln \left( \frac{I_1}{I_{S1}} \right) \]

\[ I_2 = \frac{1}{R} \cdot V_T \cdot \ln \left( \frac{I_1}{I_{S1}} \right) \]

\[ I_1 = I_2 = I_{out} = \frac{V_{EB1}}{R} \]

* Temperature Sensitivity ~ 4000 ppm/C
Realization of pnp BJT in CMOS Technology

2/22/2011

Insoo Kim
Vth Referenced CMOS Self-Bias Circuit

\[ I_2 = \frac{V_{GS1}}{R} = \frac{V_{TH} + \sqrt{\frac{2I_1}{\mu_n C_{ox}(W/L)_1}}}{R} \]

\[ I_1 = I_2 = I_{out} \approx \frac{V_{TH}}{R} \] for large \((W/L)1\)
Thermal Voltage Referenced CMOS Self-Bias Circuit

\[ \Delta V_{BE} = V_{BE1} - V_{BE2} \]
\[ = V_T \ln \left( \frac{nI_0}{I_{S1}} \right) - V_T \ln \left( \frac{I_0}{I_{S2}} \right) \]
\[ = V_T \ln n. \text{ PTAT voltage} \]
Thermal Voltage Referenced CMOS Self-Bias Circuit

\[ I_1 = I_2 \]

\[ V_{EB1} = V_{EB2} + I_2 \cdot R \]

\[ I_2 \cdot R + V_T \cdot \ln(I_2) = V_T \cdot \ln(n) + V_T \cdot \ln(I_1) \]

\[ I_2 \cdot \exp \left( \frac{I_2 \cdot R}{V_T} \right) = n \cdot I_1 \]

\[ I_2 \approx \frac{V_T \cdot \ln(n)}{R} \]

\[ I_{out} = I_1 = I_2 \approx \frac{V_T \cdot \ln(n)}{R} \]

\[ \frac{\Delta I_{out}}{I_{out}} = \frac{1}{T} - \frac{\partial R}{R} \text{ moderate TC} \]

* Temp. Sensitivity ~ +3300 ppm/C

2/22/2011

Insoo Kim
**Bandgap reference:** \( V_{\text{ref}} = V_{BE} + K \cdot V_T \)

\[
\frac{\partial V_{BE}}{\partial T} \approx -1.5 \text{ mV/°K} \\
\frac{\partial V_T}{\partial T} \approx +0.087 \text{ mV/°K} \\
V_{REF} \approx V_{BE} + 17.2V_T \approx 1.25 \text{ V}. 
\]

\[
V_{BE1} = RI + V_{BE2} \\
RI = V_{BE1} - V_{BE2} = V_T \ln n \\
V_{o2} = RI + V_{BE2} = V_T \cdot \ln n + V_{BE2} 
\]

What’s the problem?
(cont’d) CMOS Band gap Reference

Actual Implementation of CMOS Band Gap Reference

\[ V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3} (R_3 + R_2) \]

\[ = V_{BE2} + (V_T \ln n) \left( 1 + \frac{R_2}{R_3} \right) \]
Actual Implementation of CMOS Band gap Reference

\[ I_1 = I_2 \quad I_3 = I_2 = I_2 = I_1 \approx \frac{V_T \cdot \ln(n)}{R} \]

\[ V_o = I_3 \cdot xR + V_{EB3} = V_T \cdot x \cdot \ln(n) + V_{EB3} \]
Design Lab. – Self Bias Circuit with Temp. Compensation

- Schematics

(a) Basic Schematic
(b) actual implementation

* AMIS 0.5um Tech

2/22/2011

Insoo Kim
Simulation Results
Design Lab. – Self Bias Circuit with Temp. Compensation

- Simulation Results – Temp. Compensation

![Simulation Results](image)

Vr0 Current

2/22/2011

Insoo Kim
Design Lab. – Self Bias Circuit with Temp. Compensation

- Zero Temperature Coefficient Point

![Graph showing currents at different temperatures](image-url)

- 90°C
- 25°C
- 10°C
- 0.82V

2/22/2011
References