Digital Circuits with Feedback

SR latch
D Latch
D Flip-Flop
T Flip-Flop
Digital Circuits with Feedback

SR latch

\[
\begin{array}{c}
R \\
\downarrow \\
\text{NAND} \\
\uparrow \\
Q \\
\end{array}
\begin{array}{c}
S \\
\downarrow \\
\text{NAND} \\
\uparrow \\
\bar{Q} \\
\end{array}
\]
Digital Circuits with Feedback

SR latch

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>\bar{Q}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>latch</td>
<td>latch</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Digital Circuits with Feedback

SR latch

\[
\begin{array}{c|c|c|c}
S & R & Q & \overline{Q} \\
0 & 0 & \text{latch} & \text{latch} \\
0 & 1 & 0 & 1 \\
1 & 0 & 1 & 0 \\
1 & 1 & 0 & 0 \\
\end{array}
\]
Digital Circuits with Feedback

SR latch

How many feedback line?
Digital Circuits with Feedback

SR latch
Digital Circuits with Feedback

SR latch
Digital Circuits with Feedback

SR latch

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>( \overline{Q} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>latch</td>
<td>latch</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Digital Circuits with Feedback

Timing

Figure 9.3  Operation of flip-flop.
Digital Circuits with Feedback

(a) 

<table>
<thead>
<tr>
<th>$S^v$</th>
<th>$R^v$</th>
<th>$Q^v$</th>
<th>$Q^{v+1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>x</td>
</tr>
</tbody>
</table>

(b) 

Figure 9.4  R-S flip-flop.
Digital Circuits with Feedback

Figure 9.6  Clocked R-S flip-flop.
Digital Circuits with Feedback

![J-K flip-flop diagram]

<table>
<thead>
<tr>
<th>( J^v )</th>
<th>( K^v )</th>
<th>( C1^v )</th>
<th>( Q^{v+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>x</td>
<td>0</td>
<td>( Q^v )</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>( Q^v )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>( \bar{Q}^v )</td>
</tr>
</tbody>
</table>

**Figure 9.7**  
J-K flip-flop.
Figure 9.15  J-K latch.
Digital Circuits with Feedback

![Diagram of Master-Slave R-S Flip-Flop]

**Figure 9.17** Master-slave $R-S$ flip-flop.
Figure 9.18  Master-slave $J$-$K$ flip-flop.
Digital Circuits with Feedback

Figure 9.9  $T$ flip-flop.
Digital Circuits with Feedback

\[
\begin{array}{ccc}
D^v & C1^v & Q^{v+1} \\
\times & 0 & Q^v \\
0 & \uparrow & 0 \\
1 & \uparrow & 1 \\
\end{array}
\]

Figure 9.8  \( D \) flip-flop.
Figure 9.19  Positive edge-triggered $D$ flip-flop.
Figure 9.21 Positive edge-triggered $D$ flip-flop with reset and set.
Digital Circuits with Feedback
D latch

\(i_0\)
\(i_1\)
\(Z\)
\(S\)
\(0\)
Digital Circuits with Feedback

D latch

\[ i_0 \quad i_1 \]

\[ Z \]

\[ S \]

1
Digital Circuits with Feedback

D latch

D → W → Q

1
Digital Circuits with Feedback

D latch

D → Q
W → Q
0
Digital Circuits with Feedback

2 to 1 MUX switch implementation
Digital Circuits with Feedback

D latch

1 bit memory

Latch
Digital Circuits with Feedback

D Flip-Flop

D → FF → Q

CK → FF → Q
Digital Circuits with Feedback

D Flip-Flop

D → Q

CK

Q
Digital Circuits with Feedback

D Flip-Flop

D → Q

CK → Q

D Flip-Flop Circuit Diagram
Digital Circuits with Feedback

D Flip-Flop

Master Latch

Slave Latch

D → Q

CK
Digital Circuits with Feedback

D Flip-Flop

Master Latch

Slave Latch

CK

D

Positive Edge Trigger
Digital Circuits with Feedback

SR latch
D Latch
D Flip-Flop
T Flip-Flop
Digital Circuits with Feedback
Digital Circuits with Feedback

Figure 9.12  General model of sequential circuits.
Digital Circuits with Feedback