Switch Logic
Switch Logic
Switch Logic

Normally OPEN  Push to CLOSE
Switch Logic

N.O.

<table>
<thead>
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Switch Logic
Switch Logic
Switch Logic

Normally CLOSED  Push to OPEN
Switch Logic

N.C.
Switch Logic

![Switch Logic Diagram]
Switch Logic

5V

IN

OUT

9/2/2015

L05: CMOS Circuit Design
Switch Logic

IN
0V

5V

OUT
5V

9/2/2015
Switch Logic

IN
5V

OUT
0V
Switch Logic
Switch Logic
Switch Logic

5V

IN

OUT

IN

OUT
Switch Logic

5V

IN

OUT

IN

OUT

IN

OUT

9/2/2015

L05: CMOS Circuit Design
Switch Logic
Switch Logic
Switch Logic
Switch Logic

Diagram showing a circuit with switches labeled 'a' and 'b' connected to a light bulb and a battery.
Switch Logic

a AND b

9/2/2015

L05: CMOS Circuit Design
Switch Logic
Switch Logic

[Diagram of a simple switch circuit with a battery and a light bulb, labeled 'a' and 'b'.]
Switch Logic

\[ a \text{ OR } b \]
Switch Logic
Switch Logic
Switch Logic

\[ \text{a} \quad \text{b} \quad \text{OUT} \]

5V

\[ \text{OUT} \]

9/2/2015

L05: CMOS Circuit Design
Switch Logic

[Diagram of a CMOS circuit with inputs a and b and output OUT]
Switch Logic
Switch Logic
Switch Logic
Switch Logic
Switch Logic

```
5V

a
b

a
b

OUT

OUT

9/2/2015
L05: CMOS Circuit Design
36
Switch Logic
Switch Logic

\[ \text{Diagram of switch logic} \]
Switch Logic
Switch Logic
Switch Logic
Switch Logic
Switch Logic

\[ z = a \ ( b + c ) \]
Switch Logic

\[ z = a \ ( b + c ) \]
Switch Logic

\[ z = a \ ( b + c ) \]
Switch Logic

\[ z = a \left( b + c \right) \]
Switch Logic

\[ z = a \ ( b + c ) \]

10 transistors total
Switch Logic

\[ z = a \left( b + c \right) \]

PMOS FETs

NMOS FETs
Switch Logic

\[ z = a \ ( b + c ) \]
Switch Logic

\[ z = a \left( b + c \right) \]

8 transistors total!
Switch Logic

\[ y = a \ ( b + c \ d ) \]
Switch Logic

\[ y = a ( b + c d ) \]

**PMOS FETs:** AND – parallel connection
OR – series connection
Switch Logic

\[ y = a \cdot (b + c \cdot d) \]

**PMOS FETs:** AND – parallel connection
OR – series connection

**NMOS FETs:** AND – series connection
OR – parallel connection
Switch Logic

\[ y = a \left( b + c d \right) \]

**PMOS FETs:** AND – parallel connection
OR – series connection

**NMOS FETs:** AND – series connection
OR – parallel connection

5V to **PMOS FETs**
0V to **NMOS FETs**
Switch Logic

\[ y = a \ ( b + c \ d ) \]

**PMOS FETs:** AND – parallel connection
OR – series connection

**NMOS FETs:** AND – series connection
OR – parallel connection

5V to **PMOS FETs**
0V to **NMOS FETs**

Inverted OUTPUT in the middle,
So add an **Inverter**
Switch Logic

\[ y = a ( b + c d ) \]