Testing and Faults
Chip Technology

Willamette Core (0.18μm)  

Northwood Core (0.13μm)
Chip Technology
Chip Technology

2011 ITRS - Technology Trends

- 2009/10/11 ITRS MPU/ASIC Metal 1 (M1) \( \frac{1}{2} \) Pitch (nm) [historical trailing at 2-yr cycle; extended to 2013; then 3-yr cycle]
- 2009/10/11 ITRS MPU Printed Gate Length (GLpr) (nm) [3-yr cycle from 2011/35.3nm]
- 2009/10/11 ITRS MPU Physical Gate Length (nm) [begin 3.8-yr cycle from 2009/29.0nm]

Graph showing the trend of nanometers over the years from 1995 to 2030, with a projection to 2026.

2011 ITRS: 2011-2026

Long-Term '19-'26
Scaling Calculator +

Cycle Time:

0.7x \downarrow 0.7x \downarrow

250 \rightarrow 180 \rightarrow 130 \rightarrow 90 \rightarrow 65 \rightarrow 45 \rightarrow 32 \rightarrow 22 \rightarrow 16

0.5x \uparrow

N-1 \quad N \quad N+1

Cycle Time (T yrs):

*CARR(T) =

\[(0.5)^{(1/2T \text{ yrs})}] - 1\]

CARR(3 yrs) = -10.9%
CARR(2 yrs) = -15.9%

* CARR(T) = Compound Annual Reduction Rate (@ cycle time period, T)

(DRAM M1 Example)
### Chip Technology

**Table D**  
**Rounded versus Actual Trend Numbers (DRAM Product Trend Example)**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Calculated Trend Numbers (nm)</strong></td>
<td>360</td>
<td>255</td>
<td>180</td>
<td>127.3</td>
<td>103.4</td>
<td>90</td>
<td>68.2</td>
<td>63.6</td>
</tr>
<tr>
<td><strong>ITRS Rounded Numbers (nm)</strong></td>
<td>350</td>
<td>250</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>90</td>
<td>70</td>
<td>65</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
<th></th>
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<th></th>
<th></th>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Calculated Trend Numbers (nm)</strong></td>
<td>45</td>
<td>40.1</td>
<td>31.8</td>
<td>28.35</td>
<td>22.5</td>
<td>17.9</td>
<td>15.9</td>
<td>14.2</td>
<td>10.0</td>
<td>8.9</td>
<td>8.0</td>
<td>6.3</td>
</tr>
<tr>
<td><strong>ITRS Rounded Numbers (nm)</strong></td>
<td>45</td>
<td>40</td>
<td>32</td>
<td>28</td>
<td>22.5</td>
<td>17.9</td>
<td>15.9</td>
<td>14.2</td>
<td>10.0</td>
<td>8.9</td>
<td>8.0</td>
<td>6.3</td>
</tr>
</tbody>
</table>
Chip Technology

2011 ITRS - Functions/chip and Chip Size

- 2011 ITRS Cost-Performance MPU Functions per chip at production (Mtransistorst)
- 2011 ITRS High-Performance MPU Functions per chip at production (Mtransistors)
- 2011 Cost-Performance MPU Chip size at production (mm²)
- 2011 High-Performance MPU Chip size at production (mm²)

Average "Moore's Law" = 2x/2yrs

MPU = 2x/2yrs

MPU = 2x/3yrs

<260mm²
<140mm²

Year of Production

2011 ITRS: 2011-2026

Long-Term '19-'26
## Chip Technology

### Table C

#### 2011 Chip Frequency Model Trend vs. 2009/2010 ITRS Frequency

|--------------------|------|------|------|------|------|------|------|------|------|------|

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2019</th>
<th>2020</th>
<th>2021</th>
<th>2022</th>
<th>2023</th>
<th>2024</th>
<th>2025</th>
<th>2026</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Frequency (MHz)</td>
<td>11.475</td>
<td>12.361</td>
<td>13.315</td>
<td>14.343</td>
<td>15.451</td>
<td>16.640</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>On-chip local clock -- WAS</td>
<td>11.475</td>
<td>12.361</td>
<td>13.315</td>
<td>14.343</td>
<td>15.451</td>
<td>16.640</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Chip Frequency (MHz)</td>
<td>5.124</td>
<td>5.329</td>
<td>5.542</td>
<td>5.764</td>
<td>5.994</td>
<td>6.234</td>
<td>6.483</td>
<td>6.743</td>
</tr>
</tbody>
</table>

### GHz frequency
Testing and Faults
Testing and Faults
Testing and Faults
Testing and Faults

The Protruding Via

Location of the Protruding Via on the Wafer

4RCCAL 25.0kV 8.4nm x46.0k SE(U) 1.00um
Testing and Faults

Litho Induced Short and Open

12/6/2012 L12: Testing
Testing and Faults

12/6/2012
Testing and Faults
Testing and Faults

(a) Line-open failure.  (b) Open failure in contact plug.

Figure 8.30  Electromigration-related failure modes (Courtesy of N. Cheung and A. Tao, U.C. Berkeley).
Testing and Faults
Testing and Faults

Figure 8.30  Electromigration-related failure modes (Courtesy of N. Cheung and A. Tao, U.C. Berkeley).
Testing and Faults
Wafer Cost

Chip Yield
Testing and Faults

Random particles causing shorts or opens
Testing and Faults
Testing and Faults
Testing and Faults
Wafer Cost

Yield = 6/12 = 50%

Yield = 57/64 = 89%

Wafer Cost = $10,000
Wafer Cost

Die size: 40 mm x 40 mm
Yield: 35.7%
Good: 10
Bad: 18
Total: 28

Die size: 20 mm x 20 mm
Yield: 75.7%
Good: 103
Bad: 33
Total: 136

Die size: 10 mm x 10 mm
Yield: 94.2%
Good: 620
Bad: 38
Total: 658
Wafer Cost

![Wafer Price Trend](image)

Investment Needed For
ONE LEADING EDGE FAB

- 200mm: >$1B
- 300mm: >$5B
- 450mm: >$10B
## Wafer Cost

<table>
<thead>
<tr>
<th>Tested Wafer Cost</th>
<th>$1,890 (200mm epi wafer)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die Size</td>
<td>135,000 sq mils (90mm²)</td>
</tr>
<tr>
<td>Total Dice Available</td>
<td>292</td>
</tr>
<tr>
<td>Probe Yield</td>
<td>37% (at 1.2 defects/cm²)</td>
</tr>
<tr>
<td>Number Of Good Dice</td>
<td>108</td>
</tr>
<tr>
<td>Package Cost</td>
<td>$25.75 (296-pin CPGA)</td>
</tr>
<tr>
<td>Assembly Yield</td>
<td>99%</td>
</tr>
<tr>
<td>Final Test Cost</td>
<td>$35.00</td>
</tr>
<tr>
<td>Final Test Yield</td>
<td>70%</td>
</tr>
<tr>
<td>Factory Cost</td>
<td>$112.41</td>
</tr>
</tbody>
</table>

Source: ICE

### Figure 2-22. Pentium (166MHz P54CS) Cost Analysis (3Q96)
## Wafer Cost

<table>
<thead>
<tr>
<th></th>
<th>16M DRAM (0.35μ)</th>
<th>64M DRAM (0.35μ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tested Wafer Cost</td>
<td>$1,180 (200mm)</td>
<td>$1,485 (200mm)</td>
</tr>
<tr>
<td>Die Size</td>
<td>84,000 sq mils (54mm²)</td>
<td>232,500 sq mils (150mm²)</td>
</tr>
<tr>
<td>Total Dice Available</td>
<td>476</td>
<td>162</td>
</tr>
<tr>
<td>Probe Yield</td>
<td>80% (at 0.5 defects/cm²)</td>
<td>40% (at 0.7 defects/cm²)</td>
</tr>
<tr>
<td>Number Of Good Dice</td>
<td>380</td>
<td>65</td>
</tr>
<tr>
<td>Package Cost</td>
<td>$0.40</td>
<td>$0.50</td>
</tr>
<tr>
<td>Assembly Yield</td>
<td>99%</td>
<td>99%</td>
</tr>
<tr>
<td>Final Test Cost</td>
<td>$0.60</td>
<td>$1.20</td>
</tr>
<tr>
<td>Final Test Yield</td>
<td>95%</td>
<td>85%</td>
</tr>
<tr>
<td>Factory Cost</td>
<td><strong>$4.36</strong></td>
<td><strong>$29.15</strong></td>
</tr>
<tr>
<td>ASP</td>
<td>$7.75</td>
<td>$55.00</td>
</tr>
<tr>
<td>Approx. Revenue/Wafer Start</td>
<td>$2,770</td>
<td>$3,008</td>
</tr>
<tr>
<td>Revenue/Sq In. Started</td>
<td>$55</td>
<td>$60</td>
</tr>
<tr>
<td>Gross Margin</td>
<td>44%</td>
<td>47%</td>
</tr>
</tbody>
</table>

Source: ICE

**Figure 2-23. 16M and 64M DRAM Cost Analysis**
## Wafer Cost

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Defect /cm²</th>
<th>Area mm²</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
</tr>
<tr>
<td>PowerPC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>SuperSPARC</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>

## Wafer Cost

**Die Test Cost** = \( \frac{\text{Test Jig Cost} \times \text{Ave. Test Time}}{\text{Die Yield}} \)

### Packaging Cost:

- Depends on pins, heat dissipation, beauty, ...

<table>
<thead>
<tr>
<th>Chip</th>
<th>Die cost</th>
<th>pins</th>
<th>Package type</th>
<th>cost</th>
<th>Test &amp; Assembly</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>$4</td>
<td>132</td>
<td>QFP</td>
<td>$1</td>
<td>$4</td>
<td>$9</td>
</tr>
<tr>
<td>486DX2</td>
<td>$12</td>
<td>168</td>
<td>PGA</td>
<td>$11</td>
<td>$12</td>
<td>$35</td>
</tr>
<tr>
<td>PowerPC 601</td>
<td>$53</td>
<td>304</td>
<td>QFP</td>
<td>$3</td>
<td>$21</td>
<td>$77</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>$73</td>
<td>504</td>
<td>PGA</td>
<td>$35</td>
<td>$16</td>
<td>$124</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>$149</td>
<td>431</td>
<td>PGA</td>
<td>$30</td>
<td>$23</td>
<td>$202</td>
</tr>
<tr>
<td>SuperSPARC</td>
<td>$272</td>
<td>293</td>
<td>PGA</td>
<td>$20</td>
<td>$34</td>
<td>$326</td>
</tr>
<tr>
<td>Pentium</td>
<td>$417</td>
<td>273</td>
<td>PGA</td>
<td>$19</td>
<td>$37</td>
<td>$473</td>
</tr>
</tbody>
</table>
Testing and Faults

Fault Cost:

- Wafer: $0.01 - $0.1
- Packaged Chip: $0.1 - $1
- Board: $1 - $10
- System: $10 - 100
- Field: $100 - $1000
Testing and Faults

Pentium Bug:

\[ \frac{824\,633\,702\,441.0}{824\,633\,702\,441.0} = 0.999\,999\,996\,274\,709\,702 \]

Due to faulty floating point number divide look-up table
Testing and Faults

32bit Adder Test:
Testing and Faults

32bit Adder Test:

<table>
<thead>
<tr>
<th>Total test cases:</th>
<th>2</th>
<th>65</th>
<th>3.68935E+19</th>
<th>cases</th>
</tr>
</thead>
</table>

A[31:0]  

Adder  

Result[31:0]  

B[31:0]
Testing and Faults

32bit Adder Test:

<table>
<thead>
<tr>
<th>Total test cases:</th>
<th>2</th>
<th>65</th>
<th>3.68935E+19 cases</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 test per 1nsec</td>
<td></td>
<td></td>
<td>3.68935E+19 nsec</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 billion tests per second</td>
</tr>
</tbody>
</table>
Testing and Faults

32bit Adder Test:

<table>
<thead>
<tr>
<th>Total test cases:</th>
<th>2</th>
<th>65</th>
<th>3.68935E+19</th>
<th>cases</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 test per 1nsec</td>
<td></td>
<td></td>
<td>3.68935E+19</td>
<td>nsec</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>36893488147</td>
<td>sec</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 sec</td>
<td>1000000000 nsec</td>
</tr>
</tbody>
</table>
# Testing and Faults

## 32bit Adder Test:

![Adder Diagram](image)

<table>
<thead>
<tr>
<th>Total test cases:</th>
<th>2</th>
<th>65</th>
<th>3.68935E+19 cases</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 test per 1nsec</td>
<td>3.68935E+19 nsec</td>
<td>1 billion tests per second</td>
<td></td>
</tr>
<tr>
<td></td>
<td>36893488147 sec</td>
<td>1 sec</td>
<td></td>
</tr>
<tr>
<td></td>
<td>614891469.1 min</td>
<td>1min</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>60 sec</td>
<td></td>
</tr>
</tbody>
</table>
32bit Adder Test:

<table>
<thead>
<tr>
<th>Total test cases:</th>
<th>2</th>
<th>65</th>
<th>3.68935E+19</th>
<th>cases</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 test per 1nsec</td>
<td>3.68935E+19</td>
<td>nsec</td>
<td>1 billion tests per second</td>
<td></td>
</tr>
<tr>
<td></td>
<td>36893488147</td>
<td>sec</td>
<td>1sec</td>
<td>1000000000 nsec</td>
</tr>
<tr>
<td></td>
<td>614891469.1</td>
<td>min</td>
<td>1min</td>
<td>60 sec</td>
</tr>
<tr>
<td></td>
<td>10248191.15</td>
<td>hour</td>
<td>1hour</td>
<td>60 min</td>
</tr>
<tr>
<td></td>
<td>427007.9647</td>
<td>day</td>
<td>1day</td>
<td>24 hour</td>
</tr>
<tr>
<td></td>
<td>1169.884835</td>
<td>year</td>
<td>1year</td>
<td>365 day</td>
</tr>
</tbody>
</table>
Testing and Faults
Testing and Faults
Testing and Faults
Testing and Faults

Figure 10-1 Testing AND and OR Gates for Stuck-at Faults

(a) 1\rightarrow 0
    1 \ b
    1 \ c

(b) 0\rightarrow 1
    1 \ a
    1 \ c

(c) 0\rightarrow 1
    0 \ a
    0 \ b
    0 \ c

(d) 1\rightarrow 0
    0 \ a
    0 \ b
    0 \ c
Testing and Faults

**SA0**: Stuck at 0

**SA1**: Stuck at 1
Testing and Faults

Fig. 10-2  Testing an AND-OR Network

Table 10-1  Test Vectors for Fig. 10-2

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>c</th>
<th>d</th>
<th>e</th>
<th>f</th>
<th>g</th>
<th>h</th>
<th>i</th>
<th>Faults Tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>a0, b0, c0, p0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>d0, e0, f0, q0</td>
</tr>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>0</td>
<td>X</td>
<td>X</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>g0, h0, i0, r0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>a1, d1, g1, p1, q1, r1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>b1, e1, h1, p1, q1, r1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>c1, f1, i1, p1, q1, r1</td>
</tr>
</tbody>
</table>

(a) stuck-at-0 test

(b) stuck-at-1 test
Testing and Faults

Figure 10-3  Fault Detection Using Path Sensitization
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4  Example Network for Stuck-at Fault Testing

Input A stuck at 1 (SA1)?
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4  Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4  Example Network for Stuck-at Fault Testing
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing

Test Vector for A SA1: A = 0, B = 1, C = 0, D = 1, F = 0/1
Testing and Faults

Figure 10-4  Example Network for Stuck-at Fault Testing

Test Vector for A SA1: A = 0, B = 1, C = 0, D = 1, F = 0/1
Test Vector for A SA0: A = 1, B = 1, C = 0, D = 1, F = 1/0
Testing and Faults

Figure 10-4 Example Network for Stuck-at Fault Testing

Test Vector for A SA1: A = 0, B = 1, C = 0, D = 1, F = 0/1
Test Vector for A SA0: A = 1, B = 1, C = 0, D = 1, F = 1/0
Test Vector for A SA0: A = 1, B = 1, C = 0, D = 0, F = 0/1
Testing and Faults
# Testing and Faults

## Table 10-2  Tests for Stuck-at Faults in Figure 10-4

<table>
<thead>
<tr>
<th>Normal Gate Inputs</th>
<th>Faults Tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>A B C D</td>
<td>a b p c q r d s t u v w</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>0 1 0 0 0 1 1 0 1 1 0 1</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>1 1 1 0 0 1 1 1 0 1 1 1</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>1 0 0 1 1 0 1 0 1 0 1 1</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>1 1 1 0 0 1 0 1 0 0 1 0</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>1 1 1 1 1 0 1 1 0 0 1 0</td>
</tr>
</tbody>
</table>

Faults Tested:
- a1 p1 c1 v1 f1
- a0 b0 p0 q1 r0 d0 u0 v0 w0 f0
- b1 c0 s1 t0 v0 w0 f0
- a0 b0 d1 s0 t1 u1 w1 f1
- a0 b0 q0 r1 s0 t1 u1 w1 f1
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Boolean Difference

- Shannon expansion
  - A Boolean function $f(X_1, X_2, \ldots, X_n)$ can be expanded about any variable $X_i$
  - $f(X_1, X_2, \ldots, X_n) = X_i \cdot f(X_1, \ldots, X_i = 0, \ldots, X_n) + \overline{X_i} \cdot f(X_1, \ldots, X_i = 1, \ldots, X_n)$
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Boolean Difference

- Shannon expansion
  - A Boolean function \( f(X_1, X_2, \ldots, X_n) \) can be expanded about any variable \( X_i \)
    \[ f(X_1, X_2, \ldots, X_n) = X_i f(X_1, \ldots, X_i = 0, \ldots, X_n) + \neg X_i f(X_1, \ldots, X_i = 1, \ldots, X_n) \]
- Boolean Difference of \( f(X_1, X_2, \ldots, X_n) \) with respect to \( X_i \)
- Symbol is (partial derivation)
  \[
  \frac{d}{dX_i} f(X_1, X_i, \ldots, X_n)
  \]
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Boolean Difference

- Shannon expansion
  - A Boolean function \( f(X_1, X_2, \ldots, X_n) \) can be expanded about any variable \( X_i \)
  - \( f(X_1, X_2, \ldots, X_n) = X_i \cdot f(X_1, \ldots, X_i = 0, \ldots, X_n) + X_i f(X_1, \ldots, X_i = 1, \ldots, X_n) \)
- Boolean Difference of \( f(X_1, X_2, \ldots, X_n) \) with respect to \( X_i \)
- Symbol is (partial derivation)
  \[
  \frac{d}{dX_i} \frac{f(X_1, X_i, \ldots, X_n)}{dX_i}
  \]
- Definition is:
  \[
  \frac{d f}{dX_i} = f_{X_i} \oplus f_{X_i} = f(X_1, \ldots, X_i = 0, \ldots, X_n) \oplus f(X_1, \ldots, X_i = 1, \ldots, X_n)
  \]
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Boolean Difference

Example

\[ f = w + xy, \]
\[ f_y' = w \]
\[ f_y = w + x \]
\[ \frac{df}{dy} = (w) \oplus (w + x) = w'x \]
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Boolean Difference

\[
\frac{df(x,y,w)}{dy} = 1
\]
- for values of w and x for which \( f \) depends on y

\[
\frac{df(x,y,w)}{dy} = 0
\]
- for values of w and x for which \( f \) is independent of y

\[
\frac{df(w+xy)}{dy} = w'x
\]
- \( w'x = 1 \), for \( w=0, \ x=1 \)
  - When \( w = 0, x = 1, w + xy = y \)
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Boolean Difference

Example

\[ \frac{df}{dy} = fy' \oplus fy \]

\[ = (w + x) \oplus z \]

\[ = wz' + xz' + w'x'z \]
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Boolean Difference

- **Test pattern generation**
  - \( df/dx = d(xy+yz)/dx = yz \oplus (y + yz) = yz' \)

- **Test for a/0 is** \( xyz = (110) \)
  - Set \( x = 1 \) to *Provoke* Fault
  - Set \( y = 1, z = 0 \) to *Sensitize* Fault Site to Output
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Figure 10-4 Example Network for Stuck-at Fault Testing
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Figure 10-4 Example Network for Stuck-at Fault Testing

Boolean Difference Equation

\[
\frac{dF}{dA} = F(A=1) \oplus F(A=0)
\]
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