Digital Circuits with Feedback

SR latch
D Latch
D Flip-Flop
T Flip-Flop
Digital Circuits with Feedback

SR latch
D Latch
D Flip-Flop
T Flip-Flop
Digital Circuits with Feedback

SR latch

![SR latch diagram]
Digital Circuits with Feedback

SR latch

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>Q̅</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>latch</td>
<td>latch</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<td>1</td>
<td>1</td>
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<td>0</td>
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</tbody>
</table>
Digital Circuits with Feedback

SR latch

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>( \overline{Q} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>latch</td>
<td>latch</td>
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<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
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<td>1</td>
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<td>0</td>
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</table>
Digital Circuits with Feedback

SR latch

How many feedback line?
Digital Circuits with Feedback

SR latch
Digital Circuits with Feedback

SR latch

\[
\begin{align*}
\text{R} & \quad \longrightarrow \quad \text{Q} \\
\text{S} & \quad \longrightarrow \quad \overline{\text{Q}}
\end{align*}
\]
Digital Circuits with Feedback

SR latch

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Q</th>
<th>(\overline{Q})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>latch</td>
<td>latch</td>
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<tr>
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<td>0</td>
<td>1</td>
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</table>
Figure 9.3  Operation of flip-flop.
Digital Circuits with Feedback

Figure 9.4  R-S flip-flop.
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Clock

Figure 9.6 Clocked $R$-$S$ flip-flop.

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![Diagram of J-K flip-flop]

<table>
<thead>
<tr>
<th>( J^v )</th>
<th>( K^v )</th>
<th>( C1^v )</th>
<th>( Q^{v+1} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \times )</td>
<td>( \times )</td>
<td>0</td>
<td>( Q^v )</td>
</tr>
<tr>
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<td>0</td>
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<td>( Q^v )</td>
</tr>
<tr>
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<tr>
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<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>( \bar{Q}^v )</td>
</tr>
</tbody>
</table>

**Figure 9.7** J-K flip-flop.
Figure 9.15  *J-K* latch.
Figure 9.17 Master-slave $R-S$ flip-flop.
Digital Circuits with Feedback

Figure 9.18  Master-slave $J$-$K$ flip-flop.
Digital Circuits with Feedback

**Figure 9.9**  $T$ flip-flop.
Digital Circuits with Feedback

Figure 9.8  $D$ flip-flop.
Digital Circuits with Feedback

Figure 9.19  Positive edge-triggered $D$ flip-flop.
Digital Circuits with Feedback

(a)

(b) S \^ r | R \^ r | D \^ r | C1 \^ r | Q \^ r+1
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
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<td>x</td>
<td>x</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>x</td>
<td>0</td>
<td>Q ^ r</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>↑</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
</tbody>
</table>

Figure 9.21 Positive edge-triggered D flip-flop with reset and set.
Digital Circuits with Feedback
Digital Circuits with Feedback

D latch

\[ i_0 \rightarrow \circ \rightarrow S \rightarrow Z \rightarrow \circ \rightarrow i_1 \]
Digital Circuits with Feedback

D latch

i0  →  O
i1  →  O

S  →  1

Z
Digital Circuits with Feedback

D latch

D → Q

W → Q

1
Digital Circuits with Feedback

D latch

D → Q

W → 0

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2 to 1 MUX switch implementation
Digital Circuits with Feedback

D latch

1 bit memory

Latch
Digital Circuits with Feedback

D Flip-Flop

D → Q

CK → Q
Digital Circuits with Feedback

D Flip-Flop

D CK Q

0 1
D Flip-Flop
Digital Circuits with Feedback

D Flip-Flop

Master Latch

Slave Latch

D → Q

CK

Q
Digital Circuits with Feedback

D Flip-Flop

Master Latch

Slave Latch

Positive Edge Trigger

D

CK

Q
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Figure 9.12 General model of sequential circuits.