Learning Objective
Use the VLSI CAD tools to design and implement the SRAM consisting of 32 words, 16 bit per word, and analyze it. (This SRAM will be used as the program-storing ROM for the 8-bit RISC processor.)

Glossary
RAM: Random Access Memory, volatile memory, data contents lost when powered off, and data contents can be changed quickly in comparison to a magnetic tape or disk data storage which requires sequential data access.

SRAM: Static RAM, memory contents do not need periodic refreshing, SRAM cell is typically consisting of transistors forming a latch (with 1bit feedback), SRAM cells are larger in size in comparison to DRAM cells resulting in lower memory density than DRAM.

DRAM: Dynamic RAM, memory contents do need periodic refreshing, DRAM cell is typically consisting of a capacitor and a transistor switch, SRAM cells are smaller in size in comparison to SRAM resulting in higher memory density than SRAM.

ROM: Read Only Memory, non-volatile memory, permanent data storage - keeps data content even when powered off, fixed data content from the chip fabrication.

Flash memory: ROM implemented with floating gate transistors, a fixed data content by charge stored in a floating gate, with limited re-programming feature using the electron tunneling effect.

Instruction
This semester, we are building a simple microprocessor shown below. It is an 8-bit RISC processor, its full description and specification is posted at: http://www.cse.psu.edu/~kyusun/class/cmpen471/11f/hw/pj7/pj7.html
Design and implement 32 x 16 SRAM which will replace the program memory, the ROM for the 8 bit RISC microprocessor.

SRAM: 32 word, 16 bit per word, replacement for the program ROM

![SRAM Diagram](image)

The information stored in a ROM cannot be changed once the chip is fabricated. And ROM contains the program for the 8-bit RISC processor. This may present a problem if a program needs to be changed. So we replace it with an SRAM which allows its content to be changed.
The proposed SRAM will consist of separate writing and reading ports. Data width of the SRAM will be 16 bit, idat0+idat1+idat2 needs to be 16 bit for our case. In summary, the SRAM consisting of 32 words, 16 bit per word, 5 bit write-address port (addrW), 16 bit write-data port (dat0), 5 bit read-address port (addrR), and 16bit read-data port (dat1).

1. Design the SRAM, using bit-slice approach. This will allow easy expansion to larger size SRAM later, for example, 256x24 SRAM.

2. As in any memory design, the design goal is to layout the large size memory in a small area, and achieve very fast data access time. That is, your implementation of the SRAM should result in smallest AT^2 number. Most cases, the power consumption of the memory during its normal operation is also minimized but for this homework, we will only concern the optimization of area and speed. Worse designs in class will receive less than full points.

3. Bit-slice SRAM circuit is shown below.

**The 32x1 SRAM Circuit**
4. Non-bit-slice SRAM circuit is shown below.

The 32x16 SRAM Circuit
5. There are a number of ways to implement a SRAM cell. Four SRAM cell implementations are shown below. One may choose a SRAM cell to implement from the SRAM circuits shown below, or one may develop a new SRAM cell and implement.

**SRAM Cell Circuits**

![SRAM Cell Options](image)

6. Using the Cadence tool Virtuoso, design the 32x16 SRAM circuit schematic and layout. The design must be free from the DRC errors and pass the LVS checking.

7. Extract the circuit from the layout including the parasitic capacitances. Then hspice simulate the extracted circuit netlist. Any of the timing measurements required for the questions below must use the simulation of the extracted circuit from the layout including the parasitic capacitances.

8. To verify the functioning, design the Hspice simulation files: .hsp, .s, and .sp files. Your simulation output must show adrW, dat0, Wr, write address decoder output, a D latch input and output, adrR, read address decoder output, ad, and dat1 signals. Design your .hsp file to show that five writings and five readings to a random memory locations. Explain your writing and reading sequence with the signals adrW, Wr, dat0, adrR, dat1.
9. For your 32x16 SRAM, explain the data writing time. How do you measure the writing time from the simulation result? Please explain. What is the worst case data writing time of your 32x16 SRAM? Please explain the worst case data writing time.

1 bit slice, memory write time test:

10. Moreover, please explain data writing setup time and hold time. What are the worst case data writing setup time and hold time of your SRAM? How fast can you repeat the data writing of one location to another location in your 32x16 SRAM (write cycle time)?

11. Show the simulation results showing the write times: St, Ht, W0, W1, P0, P1, and Aw shown above. Show the measured times in a table.
12. For your 32x16 SRAM, explain the data reading time. How do you measure the data reading time from the simulation result, please explain. What is the worst case data reading time of your 32x16 SRAM? Please explain the worst case data reading time. How fast can you repeat the data reading of one location to another location in your 32x16 SRAM (read cycle time)?

13. Show the simulation results showing the read times: R1, R0, and ReadCyc shown above. Show the measured times in a table.

14. Which component is the slowest? Why does it take so long? How can we make it faster? Design the .hsp file to demonstrate the fastest writing and reading times of the 32x16 SRAM while maintaining the correct output result. What limits the maximum speed of operation? Show the simulation plot to substantiate your answer.

15. How many transistors are used in your 32x16 SRAM design?

16. Did you use static, dynamic, or pass transistor logic?

17. Which SRAM cell did you use for the 32x16 SRAM? Show your SRAM cell circuit.

18. Are there any errors in schematic?

19. Is there an error in layout? Does your layout pass the DRC checking without errors?

20. Is there a mismatch on the schematic versus layout? Does your design pass the LVS checking without errors?
21. Extract the circuit from the layout including the parasitic capacitances. Then hspice simulate the extracted circuit netlist. What is the worst case output signal rise time, fall time, and delay time? The worst case delay time is from which input to which output? Explain the signal path for the worst case delay time (this is called critical signal path)? Worst case delay time: T = _____ nSec.

22. What is the total layout height and width? What is the total layout area measured in um**2?
   Area: A = _____ um**2

23. What is the AT**2 measure of your design?
   AT**2 = ___________ um**2 nSec**2

24. Use hierarchical design method to manage design complexity. That is, design simple cells and design top cell which combines simple cells. The Cadence tool Virtuoso assumes all design is done this way, uses cellview to manage cells. Use meaningful names for the cells; for example, use ‘dpram8x8’ rather than ‘hw5’ for the dual port RAM register.

25. Homework 7 preparation: Create a directory hw7yourlastname under c411 directory (assuming you have c411 directory in your home for this class). Change the current directory to hw7yourlastname. Set up the directory for a new Cadence Virtuoso library. Then start the hw7 design project. For example, my hw7 directory will be hw7choi and I will be running the following unix commands right after I login to my account:

   % cd c411
   % mkdir hw7choi
   % cd hw7choi
   % runcds
   % virtuoso &

   You can follow the same except that you need to use your last name after 'hw7'. Collect all the components in this directory, it will be 'tar' and zipped, turn-in to the instructor for grading. This way, you can collect all the files within the hw7yourlastname directory and it will allow the grading. Otherwise, any missing files may cause your design verification for grade to fail. You may lose points if your turned-in hw7 design files cannot be verified by grader.

26. Create a hw7 report file hw7yourlastname.doc and include captured image of layout and the simulation results. Add your explanations and comments. On the Linux machines in room 218 IST, one can use 'openoffice.org' program for the document creating and editing, and use 'gimp' program for the image capture and processing from the screen.

27. The hw7 report file must also include the answers to the questions.

28. The hw7 report file can be in .doc or .pdf, must include a cover page for student information such as 'CMPEN 411', ‘Homework 7’, your name, etc. Please use the sample Homework 7 report format, the sample hw7 report file is posted: Sample hw7 Report

29. Create a tarred zip file of your hw7yourlastname directory in c411 directory. It will contain the schematics, symbols, layouts, .hsp, .sp files, and .doc report file. In your c411 directory, use the following unix commands

   % tar -czvf hw7yourlastname.tgz hw7yourlatname

to create a tarred zip file of hw7yourlastname library. For example,

   % tar -czvf hw7choi.tgz hw7choi

   will archive the directory hw7choi and create a zipped file hw7choi.tgz in my c411 project directory. For the grading, the command ‘tar –xzvf hw7choi.tgz’ will be used to restore project.
You may want to delete .tr0 files before zipping, for their sizes are usually large.

30. Turn-in your project zip file through Penn State ANGEL. Deposit your zip file into the Homework 7 DropBox under CLASS tab in CMPEN 411 Course.

31. Make sure that you include all the files necessary into your project folder, in order to verify for grading. Turn-in your project before 11:30pm on the due date.