

# Yuan Xie

Department of Computer Science and Engineering  
Pennsylvania State University  
354E IST Building, University Park, PA, 16802  
(814) 865-7496

yuanxie@cse.psu.edu  
<http://www.cse.psu.edu/~yuanxie/>

## Education

- 2002      **Princeton University**      Princeton, NJ  
Ph.D. in Electrical Engineering  
Thesis: *Code Compression and Decompression Architecture for Embedded VLIW Processors*  
Advisor: Wayne Wolf
- 1999      **Princeton University**      Princeton, NJ  
M.S. in Electrical Engineering
- 1997      **Tsinghua University**      Beijing, P.R.China  
B.S in Electronic Engineering

## Professional Experience

- 2003 - present      **Pennsylvania State University**      University Park, PA  
Assistant Professor in the Department of Computer Science Engineering
- 2002 - 2003      **IBM Microelectronic Division**      Essex Junction, Vermont  
Advisory Engineer in Worldwide Design Center
- 1997 -2002      **Princeton University**      Princeton, NJ  
Research Assistant in Electrical Engineering Department  
Advisor: Wayne Wolf
- 1998, 1999      **Mentor Graphics Inc.**      Willsonville, OR  
Research Summer Intern in the Behavioral Synthesis group

## Research Interests

VLSI Design, Electronic Design Automation (EDA), Computer Architecture, Embedded Systems.

## Awards and Honors

- 2007      ASP-DAC 2008 Best Paper Award Nomination (Paper [C1]).
- 2006      **National Science Foundation Faculty Early Career Development (CAREER) Award.**
- 2006      Chun-Hui Outstanding Overseas Scholar Award, Chinese Ministry of Education
- 2006      ICCAD 2006 Best Paper Award Nomination (Paper [C15]).
- 2002      SRC(Semiconductor Research Corporations) Inventor Recognition Award.
- 2001      International Conference on ASICs, Best Paper Award.

## Journal Publications

- [J1]. R. Rajaraman, V. Degalahal, J. S. Kim, N. Vijaykrishnan, Y. Xie, M. J. Irwin. "Modeling Soft Errors at Device and Logic Level for Combinational Circuits." To appear in *IEEE Transactions on Dependable and Secure Computing (TDCS)*.
- [J2]. Shengqi Yang, W. Wolf, Yuan Xie, N. Vijaykrishnan. "A New Methodology for Reliability-Aware Low-Power Design." To appear in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*.
- [J3]. S. Srinivasan, R. Krishnan, P. Mangalagiri, Yuan Xie, and N. Vijaykrishnan. "Towards Increasing FPGA Lifetime." To appear in *IEEE Transactions on Dependable and Secure Computing (TDCS)*.
- [J4]. Feng Wang, Mike Debole, Xiaoxia Wu, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin. "On-chip Bus Thermal Analysis and Optimization." To appear in *IET Computer and Digital Techniques*.

- [J5]. Yuh-fang Tsai, Feng Wang, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin. “Design Space Exploration for Three-Dimensional Cache.” To appear in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*.
- [J6]. Chang-hong Lin, Yuan Xie, and W.Wolf. “Code Compression for VLIW Embedded Systems Using a Self-Generating Table.” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 15. No. 10., Oct. 2007
- [J7]. Yuan Xie, W.Wolf, and H. Lekatsas. “Decompression Unit Design for VLIW Embedded Processors.” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 15. No. 8, pp.975-980, Aug. 2007.
- [J8]. Gabriel Loh, Yuan Xie, and Bryan Black. “Processor Design in Three-Dimensional Die-Stacking Technologies.” *IEEE Micro*, Vol. 27. No. 3, pp.31-48, May/June 2007.
- [J9]. Yuan Xie, Lin Li, M. Kandemir, N. Vijaykrishnan, and M. J. Irwin. “Reliability-Aware Co-synthesis for Embedded Systems.” *Journal of VLSI Signal Processing*, March 2007.
- [J10]. Yuan Xie, Wei-lun Hung. “Temperature-Aware Task Allocation and Scheduling for Embedded Multiprocessor Systems-on-Chip (MPSoC) Design.” *Journal of VLSI Signal Processing*, Vol. 45, No. 3, pp.177-189, December 2006.
- [J11]. Yuan Xie, Gabriel Loh, Bryan Black, and Kerry Bernstein. “Design Space Exploration for 3D Architecture.” *ACM Journal of Emerging Technologies for Computer Systems*, Vol. 2. No. 2, pp.65-103, April 2006.
- [J12]. N. Vijaykrishnan and Yuan Xie. “Reliability Concerns in Embedded System Designs.” *IEEE Computer*, Vol. 39, No. 1, pp.118-120, January 2006.
- [J13]. Yuan Xie, W.Wolf, and H. Lekatsas. “Code Compression Using Variable-to-fixed Coding.” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 14. No. 5, pp.525-536, January. 2006.
- [J14]. Yuan Xie, Jiang Xu, W.Wolf. “Augmenting Platform-based Design with Synthesis Tools.” *Journal of Circuits, Systems and Computers*, Vol. 14. No. 5, pp.525-536, April. 2003.

## Book Chapters

- [1]. Degalahal, V., R. Ramanarayanan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. “Effect of Power Optimizations on Soft Error Rate.” *IFIP Series on VLSI-SoC. pp. 1-20, 2006. Edited by R. Reis. Springer.*
- [2]. H. Luo, W. Wang, K. He, R. Luo, H. Yang, and Yuan Xie. “A Novel Gate-Level NBTI Delay Degradation Model with Stacking Effect.” *Integrated Circuits and System Design: Power and Timing Modeling, Optimization and Simulation.* pp. 160-170, 2007. Edited by N. Azemard and L. Svensson. Springer.

## Refereed Conference Publications

- [C1]. Feng Wang, Xiaoxia Wu, Yuan Xie. “Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning.” To appear in *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2008. **Best Paper Award Nomination (10 candidates out of 351 submissions, final decision will be made in Jan. 2008).** (29% acceptance rate for regular papers (100/351)).
- [C2]. Feng Wang, C. Nicopoulos, Xiaoxia Wu, Yuan Xie, N. Vijaykrishnan. “Variation-aware Task Allocation and Scheduling for MPSoC.” To appear in *Proceedings of International Conference on Computer Aided Design (ICCAD)*, Nov. 2007.
- [C3]. Xiaoxia Wu, Paul Falkenstern, and Yuan Xie. “Scan Chain Design for Three-dimensional(3D) ICs.” To appear in *Proceedings of International Conference on Computer Design (ICCD)*, Oct. 2007.
- [C4]. S. Srinivasan, P. Mangalagiri, Yuan Xie, N. Vijaykrishnan. “FPGA Routing Architecture Analysis Under Variations.” To appear in *Proceedings of International Conference on Computer Design (ICCD)*, Oct. 2007.
- [C5]. J. Kim, C. Nicopoulos, D. Park, R. Das, Yuan Xie, N. Vijaykrishnan, C. Das. “A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures.” *Proceedings of the Annual International Symposium on Computer Architecture (ISCA)*, pp. 138-149, June 2007. (46 papers accepted out of 204 submissions. 23% acceptance rate)
- [C6]. Alex K. Jones, Steven Levitan, Rob A. Rutenbar, and Yuan Xie. “Collaborative VLSI-CAD Instruction in the Digital Sandbox.” *Proceedings of IEEE International Conference on Microelectronic Systems Education*, pp. 141-142, June 2007.
- [C7]. Feng Wang, Yuan Xie, and Hai Ju. “A Novel Criticality Computation Method in Statistical Timing Analysis.” *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1611-1616, April 2007. (208 papers accepted out of 933 submissions. 22% acceptance rate)

- [C8]. Y. Wang, H. Luo, K. He, R. Luo, Yuan Xie, and H. Yang. "Temperature-aware NBTI Modeling and the Impact of Input Vector Control on Performance Degradation." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 546-551, April 2007. (208 papers accepted out of 933 submissions. 22% acceptance rate)
- [C9]. R. Krishnan, R. Ramanarayanan, S. Srinivasan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Variation Impact on SER of Combinatorial Circuits." *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 911-916, March 2007. (93 papers accepted out of 292 submissions. 31% acceptance rate)
- [C10]. A. Mupid, M. Mutyam, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Variation Analysis of CAM Cells." *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 333-338, March 2007. (93 papers accepted out of 292 submissions. 31% acceptance rate)
- [C11]. H. Luo, Y. Wang, K. He, R. Luo, H. Yang, Yuan Xie. "Modeling of PMOS NBTI Effect Considering Temperature Variation." *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 139-144, March 2007. (93 papers accepted out of 292 submissions. 31% acceptance rate)
- [C12]. Feng Wang and Yuan Xie. "Soft Error Rate Analysis for Combinational Logic Using An Accurate Electrical Masking Model." *Proceedings of IEEE International Conference on VLSI Design (VLSID)*, pp. 165-170, Jan. 2007. (141 papers accepted out of 432 submissions. 32% acceptance rate)
- [C13]. Balaji Vaidyanathan, W-L. Hung, Feng Wang, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Architecting Microprocessor Components in 3D Design Space." *Proceedings of IEEE International Conference on VLSI Design (VLSID)*, pp. 103-108, Jan. 2007. (141 papers accepted out of 432 submissions. 32% acceptance rate)
- [C14]. Balaji Vaidyanathan, Yuan Xie, N. Vijaykrishnan, R. Luo. "Leakage Optimized DECAP Design for FPGAs." *Proceedings of IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 560-563, Dec. 2006.
- [C15]. Wei-lun Hung, Xiaoxia Wu, Yuan Xie. "Guaranteeing Performance Yield in High-Level Synthesis." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp.303-309, Nov. 2006. **Best paper award nomination.** (130 papers accepted out of 537 submissions. 24% acceptance rate).
- [C16]. Qian Ding, R. Luo, H. Wang, H. Yang and Yuan Xie. "Modeling the Impact of Process Variation on Critical Charge Distribution." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 243-237, Sept. 2006. (58 regular papers accepted out of 177 submissions. 31% acceptance rate)
- [C17]. Balaji Vaidyanathan and Yuan Xie. "Crosstalk-Aware Energy Efficient Encoding for Instruction Bus through Code Compression." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 93-97, Sept. 2006. (58 papers accepted out of 177 submissions. 31% acceptance rate)
- [C18]. Xiaoxia Wu, Feng Wang, and Yuan Xie. "Analysis of Subthreshold Finfet Circuit for Ultra-low Power Design." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 91-93, Sept. 2006.
- [C19]. S. Srinivasan, M. Prasanth, S. Karthink, Yuan Xie, N. Vijaykrishnan. "FLAW: FPGA Lifetime Awareness." *Proceedings of the 43rd Design Automation Conference (DAC)*, pp. 630-635, July. 2006. (209 papers accepted out of 865 submissions. 24% acceptance rate)
- [C20]. F. Li, C. Nicopoulos, T. Richardson, Yuan Xie, N. Vijaykrishnan, M. Kandemir. "Design and Management of 3D Chip Multiprocessors using Network-in-memory." *Proceedings of the Annual International Symposium on Computer Architecture (ISCA)*, pp. 130-141, June. 2006. (31 papers accepted out of 234 submissions. 13% acceptance rate)
- [C21]. Feng Wang, Yuan Xie. "An Accurate and Efficient Model of Electrical Masking Effect for Soft Errors in Combinatorial Logic." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.
- [C22]. B. Vaidyanathan, Yuan Xie, N. Vijaykrishnan. "Soft Error Analysis and Optimizations of C-elements in Asynchronous Circuits." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.
- [C23]. R. Ramanarayanan, R. Krishnan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Temperature and Voltage Scaling Effects on Electrical Masking." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.
- [C24]. Wei-lun Hung, G. Link, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Interconnect and Thermal-aware Floorplanning for 3D Microprocessors." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 98-104, March. 2006. (93 papers accepted out of 256 submissions. 36% acceptance rate)
- [C25]. Feng Wang, Yuan Xie, N. Vijaykrishnan and M. J. Irwin. "On-chip Bus Thermal Analysis and Optimization." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 850-855, March 2006. (233 papers accepted out of 834 submissions. 28% acceptance rate)

- [C26]. Feng Wang, Yuan Xie, K. Bernstein and Y. Luo. "Dependability Analysis of Nano-scale FinFET Circuits." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 399-404, March 2006.
- [C27]. M. Mutyam, M. Eze, N. Vijaykrishnan, Yuan Xie. "Delay and Energy Efficient Data Transmission for On-Chip Buses." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 355-360, March 2006.
- [C28]. S. Yang, W. Wolf, N. Vijaykrishnan, Yuan Xie. "Reliability-Aware SOC Voltage Islands Partition and Floorplan." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 343-348, March 2006.
- [C29]. O. Ozturk, F. Wang, M. Kandemir, Yuan Xie. "Optimal Topology Exploration for Application-Specific 3D Architectures." *Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 390-395, Jan. 2006. (135 papers accepted out of 432 submissions. 31% acceptance rate)
- [C30]. Ramanarayanan, R., J. S. Kim, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "SEAT-LA: A Soft Error Analysis tool for Combinational Logic." *Proceedings of IEEE International Conference on VLSI Design*, pp. 499-502, Jan. 2006. (26.8% acceptance rate for regular papers (88 out of 328 submissions))
- [C31]. T. Richardson, C. Nicopoulos, D. Park, N. Vijaykrishnan, Yuan Xie, C. R. Das. "A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks." *Proceedings of IEEE International Conference on VLSI Design*, pp. 499-502, Jan. 2006. (26.8% acceptance rate for regular papers)
- [C32]. R. Luo, H. Luo, H. Yang, Yuan Xie. "An Instruction Level Analytical Power Model for Designing Low Power SOC." *Proceedings of IEEE International Conference on ASICs*, pp.1070-1073, Oct. 2005.
- [C33]. T. Richardson and Yuan Xie. "Evaluation of Thermal-Aware Design Techniques for Microprocessors." *Proceedings of IEEE International Conference on ASICs*, pp.62-65, Oct. 2005.
- [C34]. W-L. Hung, G. Link, Yuan Xie, N. Vijaykrishnan, N. Dhanwada, J. Conner. "Temperature-Aware Voltage Islands Architecting in System-on-Chip Design." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 689-696, Oct. 2005. (101 out of 313 submissions, 32% acceptance rate)
- [C35]. S. K. Narayanan, G. Chen, M. Kandemir, Yuan Xie. "Temperature-Sensitive Loop Parallelization for Chip Multiprocessors." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 677-682, Oct. 2005. (101 out of 313 submissions, 32% acceptance rate)
- [C36]. Y-F. Tsai, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Three-Dimensional Cache Design Exploration Using 3DCacti." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 519-524, Oct. 2005. (101 out of 313 submissions, 32% acceptance rate)
- [C37]. D. Hostetler and Yuan Xie. "Adaptive Power Management in Software Radios Using Resolution Adaptive Analog to Digital Converters." *Proceedings of IEEE International Symposium on VLSI (ISVLSI)*, pp. 186-191, May. 2005.
- [C38]. W-L. Hung, Yuan Xie, N. Vijaykrishnan, C. Addo-Quaye, T. Theocharides, M. J. Irwin "Thermal-Aware Floorplanning Using Genetic Algorithms." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 634-639, Mar. 2005. (83 out of 222 submissions, 37% acceptance rate)
- [C39]. S. Tosun, O. Ozturk, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "An ILP Formulation for Reliability-Oriented High-Level Synthesis." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 364-369, Mar. 2005. (83 out of 222 submissions, 37% acceptance rate)
- [C40]. S. Tosun, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "Reliability-Centric Hardware/Software Co-design." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 364-369, Mar. 2005. (83 out of 222 submissions, 37% acceptance rate)
- [C41]. S. Tosun, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "Reliability-centric High-level Synthesis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1258-1263, March 2005. ( 176 papers accepted out of 825 submissions. 21% acceptance rate)
- [C42]. S. Yang, W. Wolf, N. Vijaykrishnan, Yuan Xie. "Power Attack Resistant Crypto Design: A Dynamic Voltage and Frequency Switching Approach." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 64-69, March 2005. ( 21% acceptance rate)
- [C43]. Wei-lun Hung, Yuan Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. "Thermal-Aware Allocation and Scheduling for Systems-on-a-Chip Design." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 898-899, March 2005. ( 21% acceptance rate)

- [C44]. Y-F Tsai, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Leakage-Aware Interconnect for On-Chip Network." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 230-231, March 2005. (21% acceptance rate)
- [C45]. J.Conner, Yuan Xie, M. Kandemir, R. Dick, G. Link. "FD-HGAC: A Hybrid Heuristic/Genetic Algorithm Hardware/Software Co-synthesis Framework with Fault Detection." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*., pp. 709-712, Jan. 2005. (99 regular papers accepted out of 692 submissions (14.3%))
- [C46]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Yuan Xie. "Low-Leakage Robust SRAM Cell Design for Sub-100nm Technologies." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*., pp. 539-544, Jan. 2005. 14.3% acceptance rate for regular papers (99 regular papers accepted out of 692 submissions (14.3%))
- [C47]. Y-F. Tsai, N. Vijaykrishnan, M. J. Irwin, Yuan Xie. "Influence of Leakage Reduction Techniques on Delay/Leakage Uncertainty." *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 374-379, Jan. 2005. (97 regular papers accepted out of 352 submissions (28%)).
- [C48]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Yuan Xie. "Accurate Stacking Effect Macro-Modeling of Leakage Power in Sub-100nm Circuits." *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 165-170, Jan. 2005. (97 regular papers accepted out of 352 submissions (28%)).
- [C49]. S. Srinivasan, A. Gayasen, N. Vijaykrishnan, M. Kandemir, Yuan Xie, M. J. Irwin. "Improving Soft-error Tolerance of FPGA Configuration Bits." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, Nov. 2004. (24% acceptance rate).
- [C50]. W-L Hung, C. Addo-Quaye, T. Theocharides, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Thermal-Aware IP Virtualization and Placement for Networks-on-Chip Architecture." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 430-437, Oct. 2004. (84 out of 226 submissions, 37% acceptance rate.)
- [C51]. Yuan Xie, L. Li, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. "Reliability-aware Cosynthesis for Embedded Systems." *Proceedings of IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP)*, pp. 41-50, Sept. 2004.
- [C52]. W-L. Hung, Yuan Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. "Total Power Optimization Through Simultaneously Multiple-VDD Multiple-VTH Assignment and Device Sizing With Stack Forcing." *Proceedings of International Symposium on Low Power Electronics and Design (ISLPED 2004)*, pp. 144-149, Aug. 2004. 34% acceptance rate)
- [C53]. W. Xu, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Design of a Nanosensor Array Architecture." *Proceedings of Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 298-303, Apr. 2004. (23 full papers accepted out of 235 submissions, 10% rate)
- [C54]. V. Degalahal, R. Ramanarayanan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "The Effect of Threshold Voltages on the Soft Error Rate." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 503-508, Mar. 2004. (49 papers accepted out of 148 submissions, 33%)
- [C55]. C-H. Lin, W. Wolf, and Yuan Xie. "LZW-based Code Compression for VLIW Embedded Systems." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 76-81, Feb. 2004. (181 papers accepted out of 780 submissions (23%))
- [C56]. Yuan Xie. "Analysis of Two Code Compression Algorithms for Embedded Systems." *Proceedings of International Conference on ASIC (ASICON)*, pp. 773-776. Oct. 2003.
- [C57]. Yuan Xie, Wayne Wolf, H. Lekatsas. "Code Compression Using Arithmetic Coding Based Variable-to-fixed Coding." *Proceedings of Data Compression Conference (DCC 2003)*, pp. 382-391, Mar. 2003.
- [C58]. Yuan Xie, W. Wolf, and H. Lektasas. "Profile-driven Code Compression." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 76-81, Mar. 2003. (152 out of 590 submissions (25%))
- [C59]. Yuan Xie, W. Wolf, and H. Lektasas. "Code Compression for VLIW Using Variable-to-fixed Coding." *Proceedings of Fifteenth International Symposium on System Synthesis (ISSS 2002)*, pp. 138-143, Oct. 2002. (24 out of 71 submissions (33%))
- [C60]. Yuan Xie, W. Wolf, and H. Lektasas. "A Code Decompression Architecture for VLIW Processors." *Proceedings of the Thirty-Fourth International Symposium on Microarchitecture (MICRO-34)*. pp. 66-75. (29 out of 144 submissions, 20% acceptance rate)
- [C61]. Yuan Xie, W. Wolf, and H. Lektasas. "Compression Ratio and Decompression Overhead Tradeoffs in Code Compression for VLIW Architectures." *Proceedings of the Fourth International Conference on ASIC (ASICON)*. **Best Paper Award**.

[C62]. Yuan Xie, W. Wolf. "ASICosyn: Co-Synthesis of Conditional Task Graphs with Custom ASICs." *Proceedings of the Fourth International Conference on ASIC (ASICON)*.

[C63]. Yuan Xie, W. Wolf. "Allocation and Scheduling of Conditional Task Graphs in Co-synthesis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 620-625, Mar. 2001. (81 full papers out of 300 submissions (27%))

[C64]. Yuan Xie, Hua Lin, Zhao Wu, W. Wolf. "CAD Techniques for Multimedia System Design." *Proceedings of Synthesis and System Integration of Mixed Technologies (SASIMI)*, Mar. 2000.

[C65]. Yuan Xie and Wayne Wolf. "Co-synthesis with Custom ASICs." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 129-134, Jan. 2000.

## Patent

[1]. United States Patent. No.7,095,343. "Code Compression Algorithms and Architectures for Embedded Systems." Issued on August 22, 2006.

## Research Grants and Gifts

**Total Amount: \$2.62M , Personal share: \$1.51M**

08/2007-08/2009 **National Science Foundation (NSF): CNS 0720659: Hybrid Timing Analysis via Multi-mode Execution.**  
**PI**, \$120,000.

07/2007-07/2010 **National Science Foundation (NSF): CCF 0702617: HoDoo: Holistic Design of On-chip Interconnects.**  
**Co-PI** (with C. Das and N. Vijaykrishnan), \$630,894.

01/2007-01/2012 **National Science Foundation (NSF) CAREER: Process Variation Aware Embedded MPSoC Synthesis.**  
**PI**, \$400,000, plus \$270,000 PennState match.

09/2005-09/2008 **National Science Foundation (NSF): CNS 0454123: SEAT: Soft Error Analysis Toolset.**  
**Co-PI** (with N. Vijaykrishnan, M. J. Irwin, and K. Unlu) \$433,122.

09/2006-03/2008 **DARPA: Technology and Design Infrastructure for High Performance Three-Dimensional ICs.**  
**PI** (subcontract from IBM), \$150,000.

07/2007-04/2008 **Honda Research Institute: Three-Dimensional ICs Design.**  
**PI**, \$48,000.

09/2007-09/2008 **Toyota ITC: Fault-tolerant System Design.**  
**Co-PI** (with N. Vijaykrishnan), gift \$60,000.

07/2006-12/2006 **The Technology Collaborative (TTC): Digital Sandbox Course Collaboration Grant.**  
**PI**, \$27,330.

1/2005-12/2005 **The Technology Collaborative (TTC): Embedded Hardware Face Detection of Classification.**  
**Co-PI** (with N. Vijaykrishnan and H. Raju, R. Sharma), \$256,392.

09/2004-3/2006 **The Technology Collaborative (TTC): Transaction Level Power Modeling Methodology.**  
**Co-PI** (with N. Vijaykrishnan and M.Kandemir), \$149,903 plus \$80,000 match from IBM.

## Student Supervision

### Doctoral Dissertations Supervised

- 2007      **Yu Wang**, Ph.D. in Electronic Engineering, Tsinghua University (co-advised with Prof. Huazhong Yang)  
*Optimization for the Leakage Current and Reliability in Digital Integrated Circuits*  
First job: Postdoc in Tsinghua University.
- 2006      **Wei-lun Hung**, Ph.D. in Computer Science and Engineering  
*Designing Cool Chips: Low Power and Thermal-Aware Design Methodologies*  
First job: Lattice Inc.

### Master Thesis Supervised

- 2007      **Han-wei Chen**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)  
*Impact of Circuit Degradation on Design Security of Field Programmable Devices*  
Now graduate student at University of Texas at Austin.
- 2007      **Charles Addo-Quaye**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)  
*Thermal-Aware Placement and Virtualization for Three Dimensional Network-on-Chip Designs*  
Now Ph.D. student at PennState.
- 2007      **Melvin Eze**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)  
*Delay and Energy Efficient Data Transmission for On-Chip Buses*  
Now Ph.D. student at PennState.
- 2006      **Yinkun Xue**, M.S. in Computer Science and Engineering  
*Providing Energy-Aware Map Services to Mobile Devices*  
First job: Siemens Inc.
- 2005      **Thomas Richardson**, M.S. in Computer Science and Engineering  
*Analysis and Design of Scalable SoC Interconnects*  
First job: Availink Inc.

### Current Students

- Ph.D.      **Feng Wang**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2008.
- Ph.D.      **Balaji Vaidyanthan**, Ph.D. in Computer Science and Engineering, expected graduation date: 12/2008.
- Ph.D.      **Xiaoxia Wu**, Ph.D. in Computer Science and Engineering, expected graduation date: 12/2009
- Ph.D.      **Yibo Chen**, Ph.D. in Computer Science and Engineering
- Ph.D.      **Xiangyu Dong**, Ph.D. in Computer Science and Engineering
- Ph.D.      **Jin Ouyang**, Ph.D. in Computer Science and Engineering
- Ph.D.      **Guangyu Sun**, Ph.D. in Computer Science and Engineering (co-advise with A. Sivasubramaniam)
- Ph.D.      **Mike Debole**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
- Ph.D.      **Prasanth Mangalagiri**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
- Ph.D.      **Soumya Eachempati**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
- M.S.      **Paul Falkenstern**, M.S. in Computer Science and Engineering, expected graduation date: 06/2008.
- M.S.      **Yogitha Puttasiddaiah**, M.S. in Computer Science and Engineering, expected graduation date: 06/2008.
- M.S.      **Manu Parbhakar**, M.S. in Computer Science and Engineering, expected graduation date: 06/2008.
- M.S.      **Vishnu Nandakumar**, M.S. in Electrical Engineering, expected graduation date: 06/2008.

## Teaching

Semester	Course	Course Evaluation
Fall 2003	<b>CSE 597A</b> <i>Modern VLSI Design</i>	6.29 out of 7
Fall 2003	<b>CSE 598C</b> <i>Reliable and Low Power Design</i>	6.13 out of 7
Spring 2004	<b>CSE 477</b> <i>VLSI Digital Circuits</i>	5.50 out of 7
Fall 2004	<b>CSE 578</b> <i>CAD Tools</i>	5.91 out of 7
Spring 2005	<b>CSE 477</b> <i>VLSI Digital Circuits</i>	5.17 out of 7
Fall 2005	<b>CSE 578</b> <i>CAD Tools</i>	6.78 out of 7
Spring 2006	<b>CSE 331.1</b> <i>Computer Organization and Design</i>	5.54 out of 7
Spring 2006	<b>CSE 331.2</b> <i>Computer Organization and Design</i>	6.11 out of 7
Fall 2006	<b>CSE 578</b> <i>CAD Tools</i>	5.88 out of 7
Fall 2006	<b>CSE 431</b> <i>Introduction to Computer Architecture</i>	6.31 out of 7
Spring 2007	<b>CSE 477</b> <i>VLSI Digital Circuits</i>	6.53 out of 7

Department average: 5.17; College average:5.28

## Short Courses

05/2007	[1]. 3-week Summer Short Course, <b>Tsinghua University</b> . “Advanced VLSI Design”	<b>Beijing, China</b>
08/2006	[2]. 3-week Summer Short Course, <b>Tsinghua University</b> . “Advanced VLSI Design”	<b>Beijing, China</b>
05/2004	[3]. 2-day Industrial Short Course, <b>Pittsburgh Digital Greenhouse</b> . “Design of Reliable Power-Efficient Systems”	<b>Pittsburgh, PA</b>
01/2004	[4]. 2-day Industrial Short Course, <b>Pittsburgh Digital Greenhouse</b> . “Design of Reliable Power-Efficient Systems”	<b>Pittsburgh, PA</b>

## Tutorials

12/2006 MICRO-06	[1]. <b>Half-day Tutorial: “3D Integration for Microarchitectures”</b> <i>with K. Bernstein (IBM), B. Black (Intel), and G. Loh (Gatech)</i> <b>International Symposium on Microarchitecture (MICRO-39)</b>
8/2006 VLSI06	[2]. <b>Half-day Tutorial: “Thermal-Aware Design Techniques for Nanometer VLSI Chips”</b> <b>The 17th VLSI Design/CAD Symposium</b>
10/2005 ASICON05	[3]. <b>Half-day Tutorial: “Thermal-Aware Design Techniques for Nanometer VLSI Chips”</b> <b>The 6th International Conference on ASIC (ASICON)</b>
06/2005 ISCA05	[4]. <b>Half-day Tutorial: “Robust Systems Design from Unreliable Components”</b> <i>with S. Mitra (Intel), L. Spainhower (IBM), and N. Vijaykrishnan (PSU)</i> <b>International Symposium on Computer Architecture (ISCA)</b>
01/2005 ASPDAC05	[5]. <b>Half-day Tutorial: “Designing Reliable Circuit in the Presence of Soft Errors”</b> <b>Asia-South-Pasific Design Automation Conference (ASP-DAC)</b>
10/2004 ASPLOS04	[6]. <b>Full-day Tutorial: “Computing in the Presence of Soft Errors ”</b> <i>with N. Vijaykrishnan (PSU)</i> <b>Intl. Conf. on Architectural Support for Programming Languages and Operating Systems</b>

## Invited Talks

- 11/2007 [1]. Invited talk, **IBM Microelectronic Division, World-wide Design Center.** Essex Junction, VT  
“Process Variation Aware Synthesis for Nanometer VLSI”
- 10/2007 [2]. Invited tutorial, **Seagate Technology LLC.** Bloomington, MN  
“3D IC Design Tutorial”
- 10/2007 [3]. Invited talk, **SEMATECH 3D workshop .** Albany, New York  
“3D Architecture Design”
- 09/2007 [4]. Invited talk, **KAIST University.** Daejeon, Republic of Korea  
“Design Space Explorations for 3D ICs”
- 05/2007 [5]. Invited talk, **Honda Research Institute.** Tokyo, Japan  
“Design Automation for Three-dimensional ICs”
- 05/2007 [6]. Invited talk, **Peking University.** Beijing, China  
“New Dimension for High Performance”
- 04/2007 [7]. Invited talk, **IMEC (Interuniversity Microelectronics Centre).** Leuven, Belgium  
“The Challenges of Designing 3D Microarchitectures”
- 01/2007 [8]. Invited talk, **Dagstuhl Seminar on Power-Aware Computing Systems.** Dagstuhl, Germany  
“Thermal Challenges in 3D Microarchitecture Design”
- 10/2006 [9]. Invited talk, **University of Pittsburgh.** Pittsburgh, PA  
“The Challenges of Designing 3D Microarchitectures”
- 08/2006 [10]. Invited talk, **Hongkong University of Science and Technology.** Hong Kong, China  
“3D Microarchitecture Design”
- 08/2006 [11]. Invited talk, **Intel China Research Center.** Beijing, China  
“3D Microarchitecture Design”
- 03/2006 [12]. Invited talk, **IBM T.J.Watson Research Center.** Yorktown, NY  
“The Challenges of Designing 3D Microarchitectures”
- 10/2005 [13]. Invited talk, **IBM China Research Lab.** Shanghai, China  
“Thermal-Aware Design Techniques for Nanometer VLSI Chip”
- 10/2005 [14]. Invited talk, **Peking University.** Beijing, China  
“Thermal-Aware Design Techniques for Nanometer VLSI Chip”
- 10/2005 [15]. Invited talk, **Shanghai Jiaotong University.** Shanghai, China  
“Thermal-Aware Design Techniques for Nanometer VLSI Chip”
- 05/2005 [16]. Invited talk, **Syracuse University.** Syracuse, NY  
“Thermal-Aware Design Techniques for Nanometer VLSI Chip”
- 10/2005 [17]. Invited talk, **University of South Florida.** Tempa, FL  
“Thermal-Aware Design Techniques for Nanometer VLSI Chip”
- 10/2004 [18]. Invited talk, **IBM Circuit Education Seminar.**  
“Soft Errors: Interactions with Power Optimizations”

## Service and Activities

### Professional Community

2007- Chair of Student Technical Activities on the Technical Activities Board, IEEE Computer Society.

### Editorial

2007- Associate Editor, IEEE Transactions on VLSI Systems (TVLSI).

2007 Guest co-Editor, ACM Journal of Emerging Technologies for Computer Systems (JETC), Special Issues on 3D ICs.

### **Conferences/Workshops:**

- 2008 Program Committee Member, International Conference on VLSI Design (VLSID 2008)
- 2008 Program Committee Member, Asia and South Pacific Design Automation Conference (ASP-DAC 2008)
- 2008 Program Committee Member, IEEE International Symposium on Circuits and Systems (ISCAS 2008)
- 2007 Session Chair, International Conference on Computer Aided Design (ICCAD)
- 2007 Program Committee Member, International Workshop on Trustworthiness, Reliability and Services in Ubiquitous and Sensor Networks (TRUST 2007)
- 2006-2007 Program Committee Member, International Conference on Communications, Circuits, and Systems
- 2007 Program Committee Member, International Symposium on Low Power Electronics and Design (ISLPED 2007)
- 2007-2008 Program Committee Member, IEEE International Symposium on Circuits and Systems (ISCAS 2007)
- 2007 Program Committee Member, ACM International Conference on Computing Frontiers (CF 2007)
- 2007 Program Committee Member, EDAA/PhD Forum, in conjunction with DATE 2007
- 2006-2008 Program Committee Member, Finance Chair (2008), Greatlake Symposium on VLSI (GLSVLSI)
- 2006 Program Committee Member, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2006)
- 2006 Program Committee Member, International Conference on Nano-networks (Nano-Net 2006)
- 2006 Program Committee Member, IFIP International Conference on Embedded and Ubiquitous Computing
- 2005 Program Committee Member, International Conference on Embedded Software and System (ICESS'05)
- 2005 Tutorial Chair, ACM Conference on Embedded Software (EMSOFT 2005)
- 2004-2005 Session Chair, International Conference on Computer Design
- 2003 Session Chair, International Conference on ASICs

### **Services to the University**

- 2007- IEEE Computer Society Advisor, PennState
- 2007- Student Advisor, Engineering Advising Center, College of Engineering, PennState
- 2006-07 Ph.D. Candidacy Exam Chair, Computer Science Engineering Dept, PennState
- 2005-06 Department Colloquium Chair, Computer Science Engineering Dept, PennState
- 2003-05 Graduate Committee, Computer Science Engineering Dept, PennState