

Yuan Xie

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Education

2002	Princeton University Ph.D. in Electrical Engineering	Princeton, NJ
1999	Princeton University M.S. in Electrical Engineering	Princeton, NJ
1997	Tsinghua University B.S in Electronic Engineering	Beijing, P.R.China

Professional Experience

2008 - present	Pennsylvania State University Associate Professor in the Department of Computer Science Engineering	University Park, PA
2010	Peking University Adjunct Professor in the Center for Energy-Efficient Computing and Application	Beijing, China
2010	National Tsing Hua University Visiting Professor in the Department of Computer Science	HsinChu, Taiwan
05-06/2010	IMEC (Interuniversity Microelectronics Centre) Visiting Researcher	Leuven, Belgium
2003 - 2008	Pennsylvania State University Assistant Professor in the Department of Computer Science Engineering	University Park, PA
2002 - 2003	IBM Microelectronic Division Advisory Engineer in Worldwide Design Center	Essex Junction, Vermont

Research Summary

Yuan Xie has published 30+ journals and more than 100 refereed conference papers in the areas of VLSI design, EDA, computer architecture, and embedded systems, with a focus on design automation and novel architecture for Three-dimensional IC Design (3D ICs), emerging memory technologies, low power and thermal-aware design, system-level synthesis and high-level synthesis for embedded systems. He has graduated 10 Ph.D. students and is currently supervising 12 Ph.D. graduates. He has served as PI/Co-PI on 11 research grants administered by US Federal agencies (including National Science Foundation, DoE, and DARPA) and 13 research grants from industry, with total amount of \$8.65 million and personal share of \$3.62 million. These projects have resulted in the design of new CAD tools and optimizations, and novel architectures for emerging technologies such as 3D ICs and emerging memory technologies. He has received Best Paper Awards (ISLPED 2011, ASP-DAC 2008, ASICON 2001) with several Best Paper Nominations (ICCAD 2006, ASP-DAC 2009, ASP-DAC 2010). Through extensive collaboration with industry partners (IBM, HP, Qualcomm, Honda, Toyota, Seagate, IMEC etc.), he has helped transition research ideas to industry.

Service Summary

Yuan Xie has been active volunteer in the design automation, VLSI and computer architecture conferences. He served as program committee member, track chair and conference chair for leading conferences in these areas, including top EDA conferences such as DAC, ICCAD, ASP-DAC, and DATE (He will serve as the TPC Vice-chair for ASP-DAC 2012, TPC chair for ISLPED 2013, and TPC chair for ASP-DAC 2013), and top architecture conferences such as ISCA and HPCA. Currently he serves as a committee member in IEEE Design Automation Technical Committee (DATC), and serves as the Associate Editor for IEEE Transactions on CAD, IEEE Transactions on VLSI, ACM Journal of Emerging Technologies in Computing Systems, IEEE Design and Test of Computers, and IET Computers and Design Techniques. He has given 17 tutorials in prestigious conferences and 50+ invited talks in industry/academia to promote the awareness of 3D IC technology.

Awards and Honors

2011	ACM/IEEE International Symposium on Low Power Electronics Best Paper Award(Paper [C8])
2011	ACM Student Research Competition Grand Finals by advisee Xiangyu Dong
2010	Overseas and Hong Kong, Macau Scholars Collaborative Research Award by China NSF
2010-	Association for Computing Machinery(ACM) Distinguished Speaker
2010-13	IEEE Computer Society Distinguished Visitor
2010	ASP-DAC 2010 Best Paper Award Nomination (Paper [C37])
2009	Selected as one of the 7 overseas scholars in "Dragon Star" Program supported by China NSF.
2009	Penn State Engineering Society Outstanding Research Award Nomination, Penn State
2009	ASP-DAC 2009 Best Paper Award Nomination (Paper [C51])
2008	IBM Faculty Award
2008	ASP-DAC 2008 Best Paper Award (Paper [C65])
2008	Department Faculty Teaching Award, Computer Science and Engineering Department
2007	Outstanding Teaching Award Nomination, College of Engineering, Penn State
2006	National Science Foundation Faculty Early Career Development (CAREER) Award.
2006	Chun-Hui Outstanding Overseas Scholar Award, Chinese Ministry of Education
2006	ICCAD 2006 Best Paper Award Nomination (Paper [C80]).
2002	SRC(Semiconductor Research Corporations) Inventor Recognition Award.
2001	International Conference on ASICs, Best Paper Award (Paper [C126]).

Research Grants

Research Grants from Federal Agency

09/2011- 08/2012	National Science Foundation (NSF): EAGER: SHF: Harnessing Cross-Layer Heterogeneity for Future CMPs. <u>co-PI</u> , \$300,000.
01/2011- 12/2014	Department of Energy (DoE): Blackcomb: Hardware-Software Co-design for Non-Volatile Memory in Exascale Systems. <u>Co-PI</u> with ORNL, HP Labs, Univ. of Michigan , \$3,000,000 (\$457K to Penn State).
09/2010- 09/2013	National Science Foundation (NSF): CCF: Collaborative Research:Testing and Design-for-Testability Solutions for 3D Stacked Integrated Circuits. <u>PI</u> , \$200,000 (Total \$400K shared with Duke University).
09/2009- 09/2013	National Science Foundation (NSF): CCF 905365: Providing Predictable Timing for Task Migration in Embedded Multi-Core Environments (TiME-ME). <u>PI</u> , \$335,000 (Total \$1025K shared with NCSU and SIU).
09/2009- 09/2013	National Science Foundation (NSF): CCF 916887: TC:Small:Improving Lifetime Reliability for Reconfigurable Embedded Systems. <u>co-PI</u> , \$414,000
08/2009- 08/2012	National Science Foundation (NSF) and SRC: CCF 903432: ADAMS: Architecture and Design Automation for 3D Multi-core Systems. <u>PI</u> (with V. Narayanan), \$480,000.
08/2007- 08/2009	National Science Foundation (NSF): CNS 0720659: Hybrid Timing Analysis via Multi-mode Execution. <u>Sole PI</u> , \$136,000.
07/2007- 07/2010	National Science Foundation (NSF): CCF 0702617: HoDoo: Holistic Design of On-chip Interconnects. <u>Co-PI</u> (with C. Das and N. Vijaykrishnan), \$630,894.
01/2007- 01/2012	National Science Foundation (NSF) CAREER 0643902: Process Variation Aware Embedded MPSoC Synthesis. <u>Sole PI</u> , \$428,000, plus \$270,000 PennState match.
09/2005- 09/2008	National Science Foundation (NSF): CNS 0454123: SEAT: Soft Error Analysis Toolset. <u>Co-PI</u> (with N. Vijaykrishnan, M. J. Irwin, and K. Unlu) \$433,122.
09/2006- 03/2008	DARPA: Technology and Design Infrastructure for High Performance Three-Dimensional ICs. <u>Sole PI</u> , \$150,000.

Research Grants from Industry

01/2011- 12/2013	Semiconductor Research Corporations (SRC): Test and Design-for-Testability Solutions for 3D Stacked Integrated Circuits.<u>PI</u> , \$96,000.
01/2010- 12/2010	Industrial Technology Research Institute(ITRI, Taiwan): 3D Architecture for intelligent Signal Processing Architecture (iSPA).<u>PI</u> , NT\$50,000.
08/2009- 08/2012	Semiconductor Research Corporations (SRC) : ADAMS: Architecture and Design Automation for 3D Multi-core Systems. <u>PI</u> (with V. Narayanan), \$120,000.

04/2008- 03/2011	Semiconductor Research Corporations (SRC): <i>Statistical Behavioral Synthesis for Nanometer VLSI.</i> Sole PI , \$195,000.
12/2009- 12/2010	Industrial Technology Research Institute(ITRI, Taiwan): <i>Three-Dimensional Architecture Toolset.</i> Sole PI , \$50,000.
07/2008- 06/2009	IBM (Faculty Award): <i>Three-Dimensional Custom EDA Toolset.</i> Sole PI , gift \$20,000.
07/2008- 06/2009	Qualcomm: <i>Three-Dimensional Architecture.</i> Sole PI , \$50,000(gift).
01/2010- 06/2011	Qualcomm: <i>STT-RAM Memory Architecture for Mobile Computing.</i> Sole PI , \$75,000.
07/2007- 07/2009	Honda Research Institute: <i>Three-Dimensional ICs Design.</i> Sole PI , \$105,600.
09/2007- 09/2008	Toyota ITC: <i>Fault-tolerant System Design.</i> Co-PI (with N. Vijaykrishnan), gift \$60,000.
07/2006- 12/2006	The Technology Collaborative (TTC): <i>Digital Sandbox Course Collaboration Grant.</i> Sole PI , \$27,330.
1/2005- 12/2005	The Technology Collaborative (TTC): <i>Embedded Hardware Face Detection of Classification.</i> Co-PI (with N. Vijaykrishnan and H. Raju, R. Sharma), \$256,392.
09/2004- 3/2006	The Technology Collaborative (TTC): <i>Transaction Level Power Modeling Methodology.</i> Co-PI (with N. Vijaykrishnan and M.Kandemir), \$149,903 plus \$80,000 match from IBM.

Journal Publications

- [J1]. Vinay Saripalli, Guangyu Sun, Asit Mishra, Yuan Xie, Suman Datta, Vijaykrishnan Narayanan. "Exploiting Heterogeneity for Energy Efficiency in Chip Multiprocessors." To appear in *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, 2011
- [J2]. Yuan Xie. "Modeling, Architecture, and Applications for Emerging Non-volatile Memory Technologies." To appear in *IEEE Computer Design and Test*, January, 2011
- [J3]. Xiangyu Dong, Xiaoxia Wu, Yuan Xie, Yiran Chen, Hai Li. "Stacking MRAM atop Microprocessors: An Architecture-Level Evaluation." To appear in *IET Computers and Digital Techniques (IET CDT)*, June, 2011
- [J4]. Xiangyu Dong, Yuan Xie, Naveen Muralimanohar, Norm Jouppi. "Hybrid Checkpointing using Emerging Non-Volatile Memories for Future Exascale Systems." To appear in *ACM Transactions on Architecture and Code Optimization (TACO)*, 2011
- [J5]. Xiaoxia Wu, Wei Zhao, Chandra Nimmagadda, Durodami Lisk, Mark Nakamoto, Sam Gu, Riko Radojcic, Matt Nowak, and Yuan Xie. "Electrical Characterization for Inter-tier Connections and Timing Analysis for 3D ICs." To appear in *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*.
- [J6]. Shengqi Yang, Pallav Gupta, Marilyn Wolf, Dimitrios Serpanos, Yuan Xie, N. Vijaykrishnan. "Power Analysis Attack Resistance Engineering by Dynamic Voltage and Frequency Scaling." To appear in *ACM Transactions in Embedded Computing Systems (TECS)*
- [J7]. Yu Wang, Hong Luo, Ku He, Rong Luo, Huanzhong Yang, Yuan Xie. "Temperature-Aware NBTI Modeling and the Impact of Standby Leakage Reduction Techniques on Circuit Performance Degradation." To appear in *IEEE Transactions on Dependable and Secure Computing (TDCS)*.
- [J8]. Yu Wang, Xiaoming Chen, Wenping Wang, Yu Cao, Yuan Xie, Huazhong Yang. "Leakage Power and Circuit Aging Optimization by Gate Replacement Techniques." To appear in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*.
- [J9]. Xiaoxia Wu, Jian Li, Lixi Zhang, Evan Speight, Yuan Xie. "Hybrid Cache Architecture with Disparate Memory Technologies." To appear in *ACM Transactions on Architecture and Code Optimization (TACO)*.
- [J10]. Feng Wang, Yibo Chen, Xiaoxia Wu, C. Nicopoulos, Yuan Xie, N. Vijaykrishnan. "Variation-aware Task Allocation and Scheduling for MPSoC." *IEEE Transactions on CAD (TCAD)*, Vol 30, No.2, pp. 259-307, 2011
- [J11]. Feng Wang and Yuan Xie. "SER Analysis for Combinational Logic Using an Accurate Electrical Masking Model." *IEEE Transactions on Dependable and Secure Computing (TDCS)*. Vol. 8, No. 1, 2011, pp.137-146.

- [12]. Xiangyu Dong, Jishen Zhao, Yuan Xie. "Cost Analysis and Cost-driven Design for 3D ICs." *IEEE Transactions on CAD (TCAD)*, Vol 29, No. 12, pp. 1959-1972, Dec. 2010.
- [13]. Yiran Chen, Hai Li, Cheng-Kok Koh, Guangyu Sun, Jing Li, Yuan Xie, and Kaushik Roy. "Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance." *IEEE Transactions on VLSI (TVLSI)*, Vol 18, No. 11, pp. 1621-1624, Nov. 2010.
- [J14]. Xiaoxia Wu, Yibo Chen, Krishnendu Chakrabarty, Yuan Xie. "Test-access mechanism optimization for core-based three-dimensional SOCs." *Microelectronics Journal, Volume 41 Issue 10*, pp. 601-615, Oct. 2010
- [J15]. Gabe Loh, Yuan Xie. "3D Stacked Microprocessor: Are We There Yet?" *IEEE Micro, Volume 30 Issue 3*, pp. 60-64, May. 2010
- [J16]. Wei-lun Hung, Yuan Xie, Narayanan Vijaykrishnan, Mahmut Kandemir, and Mary Jane Irwin. "Total Power Optimization for Combinational Logics Using Genetic Algorithms." *Journal of VLSI Signal Processing. Vol. 58, No. 2*, pp.145-160, Feb. 2010.
- [J17]. Hong Luo, Yu Wang, Rong Luo, Huazhong Yang, Yuan Xie. "Temperature-aware NBTI Modeling Techniques in Digital Circuits." *IEICE Transactions on Electronics.*, No. 6, pp. 875-886, 2009
- [J18]. Yuan Xie and Yibo Chen. "Statistical High Level Synthesis Considering Process Variations." *IEEE Computer Design and Test, Special Issue on HLS*, Vol. 26, Issue 4, pp.78-87, July-August, 2009
- [J19]. Xiaoxia Wu, Paul Falkenstern, Krishnendu Chakrabarty, Yuan Xie. "Scan-chain design and optimization for three-dimensional integrated circuits." *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, Vol. 5, Issue 2, pp.1-26, July, 2009
- [J20]. M. DeBole, R. Krishnan, V. Balakrishnan, W. Wang, H. Luo, Y. Wang, Y. Xie, Y. Cao and N. Vijaykrishnan. "New-Age: A Negative Bias Temperature Instability-Estimation Framework for Microarchitectural Components." *International Journal of Parallel Programming.*, Vol. 37, No.4, pp.417-431, August, 2009.
- [J21]. M. Mutyam, A. Mupid, F. Wang, N. Vijaykrishnan, Yuan Xie, M. Kandemir. "Process Variation Aware Adaptive Cache Architecture and Management." *IEEE Transactions on Computers.*, Vol. 58, No.7, pp.865-877, July, 2009.
- [J22]. R. Rajaraman, V. Degalahal, J. S. Kim, N. Vijaykrishnan, Y. Xie, M. J. Irwin. "Modeling Soft Errors at Device and Logic Level for Combinational Circuits." *IEEE Transactions on Dependable and Secure Computing (TDCS).*, Vol. 6, No. 3, pp.202-216, June 2009.
- [J23]. C. Celik, K.Unlu, K. Ramakrishnan, R. Rajaraman, N. Vijaykrishnan, M. J. Irwin, Y. Xie. "Thermal Neutron Induced Soft Error Rate Measurement in Semiconductor Memories and Circuits." *Journal of Radioanalytical and Nuclear Chemistry.*, Vol. 278, No.2, pp.509-512, Nov 2008.
- [J24]. S. Srinivasan, R. Krishnan, P. Mangalagiri, Yuan Xie, and N. Vijaykrishnan. "Towards Increasing FPGA Lifetime." *IEEE Transactions on Dependable and Secure Computing (TDCS)*, Vol. 5, Issue 2, pp.115-127 Apr-Jun 2008.
- [J25]. Shengqi Yang, W. Wang, W. Wolf, Yuan Xie, N. Vijaykrishnan. "Case Study of Reliability-Aware and Low-Power Design." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 16, Issue 7, pp.861-873, July 2008.
- [J26]. Yuh-fang Tsai, Feng Wang, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin. "Design Space Exploration for Three-Dimensional Cache." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol.16, Issue 4, pp.444-455, Apr. 2008 .
- [J27]. Chang-hong Lin, Yuan Xie, and W.Wolf. "Code Compression for VLIW Embedded Systems Using a Self-Generating Table." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 15. No. 10.,pp.1160-1171, Oct. 2007
- [J28]. Feng Wang, Mike Debole, Xiaoxia Wu, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin. "On-chip Bus Thermal Analysis and Optimization." *IET Computer and Digital Techniques, Vol. 1, No. 5.*, pp.590-599, 2007.
- [J29]. Yuan Xie, W.Wolf, and H. Lekatsas. "Decompression Unit Design for VLIW Embedded Processors." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 15. No. 8, pp.975-980, Aug. 2007.
- [J30]. Gabriel Loh, Yuan Xie, and Bryan Black. "Processor Design in Three-Dimensional Die-Stacking Technologies." *IEEE Micro, Vol. 27. No. 3*, pp.31-48, May/June 2007.
- [J31]. Yuan Xie, Lin Li, M. Kandemir, N. Vijaykrishnan, and M. J. Irwin. "Reliability-Aware Co-synthesis for Embedded Systems." *Journal of VLSI Signal Processing, Vol. 49, No.10*, pp.87-99, March 2007.

- [J32]. Yuan Xie, Wei-lun Hung. “Temperature-Aware Task Allocation and Scheduling for Embedded Multiprocessor Systems-on-Chip (MPSoC) Design.” *Journal of VLSI Signal Processing*, Vol. 45, No. 3, pp.177-189, December 2006.
- [J33]. Yuan Xie, Gabriel Loh, Bryan Black, and Kerry Bernstein. “Design Space Exploration for 3D Architecture.” *ACM Journal of Emerging Technologies for Computer Systems*, Vol. 2. No. 2, pp.65-103, April 2006.
- [J34]. N. Vijaykrishnan and Yuan Xie. “Reliability Concerns in Embedded System Designs.” *IEEE Computer*, Vol. 39, No. 1, pp.118-120, January 2006.
- [J35]. Yuan Xie, W.Wolf, and H. Lekatsas. “Code Compression Using Variable-to-fixed Coding.” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 14. No. 5, pp.525-536, January. 2006.
- [J36]. Yuan Xie, Jiang Xu, W.Wolf. “Augmenting Platform-based Design with Synthesis Tools.” *Journal of Circuits, Systems and Computers*, Vol. 14. No. 5, pp.525-536, April. 2003.

Book

- [1]. Yuan Xie, Jason Cong, Sachin Sapatnekar. “Three-dimensional IC: Design, CAD, and Architecture.” *Springer*. 2009

Book Chapters

- [1]. Xiaoxia Wu, Yuan Xie, N. Vijaykrishnan. “Thermal-aware 3D IC Designs.” *3D Integration of Integrated Circuits*. Edited by C. S. Tan, K. N. Chen and S. J. Koester, Pan Stanford Publishing Ltd. 2011
- [2]. Yuan Xie, N. Vijaykrishnan, Chita Das. “3D Network-on-chip Architecture.” *Three-dimensional IC: Design, CAD, and Architecture*. Edited by Yuan Xie, Jason Cong, Sachin Sapatnekar. *Springer*. 2009.
- [3]. Yuan Xie, Xiangyu Dong. “System-level Cost Analysis and Design Exploration for 3D ICs.” *Three-dimensional IC: Design, CAD, and Architecture*. Edited by Yuan Xie, Jason Cong, Sachin Sapatnekar. *Springer*. 2009.
- [4]. Degalahal, V., R. Ramanarayanan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. “Effect of Power Optimizations on Soft Error Rate.” *IFIP Series on VLSI-SoC*. pp. 1-20, 2006. Edited by R. Reis. *Springer*.

Refereed Conference Publications

- [C1]. Dimin Niu, Yang Xiao, Yuan Xie “Low Power Memristor-Based ReRAM Design with Error Correcting Code”, *To appear in Proceedings of ACM/IEEE Asia and South-Pacific Design Automation Conference, 2012*, 99 accepted out of 288 submissions (34%)
- [C2]. Zuwei Li, Yuchun Ma, Qiang Zhou, Yici Cai, Yu Wang, Tingting Huang, Yuan Xie “Thermal-aware Power Network Design for IR Drop Reduction in 3D ICs”, *To appear in Proceedings of ACM/IEEE Asia and South-Pacific Design Automation Conference, 2012*, 99 accepted out of 288 submissions (34%)
- [C3]. Qiaosha Zou, Yibo Chen, Alan Su, Yuan Xie “System-level Design Space Exploration for 3D SoCs”, *To appear in Proceedings of ACM/IEEE CODES+ISSS, 2011*, (Invited Paper)
- [C4]. Jishen Zhao, Cong Xu, Yuan Xie “Bandwidth-Aware Reconfigurable Cache Design with Hybrid Memory Technologies”, *To appear in Proceedings of ACM/IEEE Intl. Conf. on Computer-aided Design (ICCAD), 2011*
- [C5]. Cong Xu, Dimin Niu, Xiaochun Zhu, Seung H. Kang, Matt Nowak and Yuan Xie “Device-Architecture Co-Optimization of STT-RAM Based Memory for Low Power Embedded System”, *To appear in Proceedings of ACM/IEEE Intl. Conf. on Computer-aided Design (ICCAD), 2011*
- [C6]. Guangyu Sun, Eren Kursun, Jude Rivers, Yuan Xie “Improving the Vulnerability of CMPs to Soft Errors with 3D Stacked Non-volatile Memory”, *To appear in Proceedings of ACM/IEEE Intl. Conf. on Computer Design (ICCD), 2011*
- [C7]. Jue Wang, Xiangyu Dong, Guanyu Sun, Dimin Niu and Yuan Xie. “Energy-Efficient Multi-Level Cell Phase-Change Memory System with Data Encoding”, *To appear in Proceedings of ACM/IEEE Intl. Conf. on Computer Design (ICCD), 2011*
- [C8]. Yibo Chen, Eren Kursun, Dave Motschman, Charles Johnson, Yuan Xie “Analysis and Mitigation of Lateral Thermal Blockage Effect of Through-Silicon-Via in 3D IC Designs”, *Proceedings of ACM/IEEE Intl. Symp. on Low Power Electronic Devices (ISLPED), 2011, Best Paper Award*
- [C9]. Jin Ouyang, Chuan Yang, Dimin Niu, Yuan Xie, Zhiwen Liu “F²BFLY: An On-Chip Free-Space Optical Network with Wavelength-Switching”, *Proceedings of ACM/IEEE 25th International Conference on Supercomputing (ICS), 2011*, (35 accepted out of 161 submissions, 21%)

- [C10]. A. Mishra, Xiangyu Dong, Guangyu Sun, Yuan Xie, N. Vijaykrishnan, C. Das “Architecting NoCs for Stacked 3D STT-RAM Caches in CMPs”, *Proceedings of ACM/IEEE International Conference on Computer Architecture (ISCA)*, 2011, (40 accepted out of 208 submissions, 19%)
- [C11]. Guangyu Sun, C. Hughes, C. Kim, Jishen Zhao, C. Xu, Yuan Xie, Yen-KuanChen “Moguls: a Model to Explore Memory Hierarchy for Throughput Computing”, *Proceedings of ACM/IEEE International Conference on Computer Architecture (ISCA)*, 2011,(40 accepted out of 208 submissions, 19%)
- [C12]. Yung-Chih Chen, Soumya Eachempati, Chun-Yao Wang, Vijaykrishnan Narayanan, Yuan Xie, Suman Dutta “Automated Mapping for Reconfigurable Single Electron Transistor Arrays”, *Proceedings of ACM/IEEE Design Automation Conference (DAC)*, 2011
- [C13]. Cong Xu, Xiangyu Dong, Norm Jouppi, and Yuan Xie “Design Implications of Memristor-Based RRAM Cross-Point Structures”, *In Proceedings of ACM/IEEE Design Automation and Test in Europe Conference (DATE)*, pp.734-739, 2011
- [C14]. Jishen Zhao, Xiangyu Dong, and Yuan Xie ‘An Energy-Efficient 3D CMP Design with Fine-Grained Voltage Scaling”, *In Proceedings of ACM/IEEE Design Automation and Test in Europe Conference (DATE)*, pp.539-542, 2011
- [C15]. Shekhar SriKantiah, Emre Kultursay, Tao Zhang, Mahmut Kandemir, Mary Jane Irwin, and Yuan Xie, “MorphCache: A Reconfigurable Adaptive Multi-level Cache Hierarchy for CMPs”, *Proceedings of IEEE International Symposium on High-Performance Computer Architecture Conference (HPCA)*, pp. 231-242, 2011
- [C16]. Jin Ouyang and Yuan Xie “Enabling Quality-of-Service in Nanophotonic Network-on-Chip”, *Proceedings of ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC 2011)*, 2011
- [C17]. Xiangyu Dong and Yuan Xie “AdaMS: Adaptive MLC/SLC Phase-Change Memory Design for File Storage”, *Proceedings of ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.31-36, 2011
- [C18]. Wulong Liu, Yu Wang, Wei Liu, Yuchun Ma, Yuan Xie, Huazhong Yang “On-Chip Hybrid Power Supply System for Wireless Sensor Nodes”, *Proceedings of ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.43-48, 2011
- [C19]. Guangyu Sun, Dimin Niu, Jin Ouyang, Yuan Xie “A Frequent-Value Based PRAM Memory Architecture”, *Proceedings of ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.211-216, 2011
- [C20]. Jin Ouyang and Yuan Xie “LOFT: A High Performance Network-on-Chip Providing Quality-of-Service Support”, *Proceedings of Intl. Symp. on Microarchitecture (MICRO 2010)*, pp.351-356, 2010
- [C21]. Tao Zhang, Kui Wang, Yi Feng, Yan Chen, Qun Li, Bing Shao, Xiaodi Song, Lian Duan, Yuan Xie, Xu Cheng, Yong-long Lin, “A 3D SoC Design for H.264 Application With On-Chip DRAM Stacking”, *Proceedings of IEEE International 3D System Integration Conference (3DIC)*, 2010
- [C22]. Jing Xie, Xiangyu Dong, Yuan Xie “3D Memory Stacking for Fast Checkpointing/Restore Applications”, *Proceedings of IEEE International 3D System Integration Conference (3DIC)*, 2010
- [C23]. Tao Zhang, Kui Wang, Yi Feng, Lian Duan, Xiaodi Song, Yuan Xie, Xu Cheng, Yong-long Lin, “A Customized Design of DRAM Controller for On-Chip 3D DRAM Stacking”, *Proceedings of Custom IC Conference (CICC 2010)*, 2010
- [C24]. Xiangyu Dong, Yuan Xie, Norm Jouppi, Naveen Muralimanohar “Simple but Effective Heterogeneous Main Memory with On-Chip Memory Controller Support” *Proceedings of Supercomputing (SC 2010)*, 2010.
- [C25]. Li Jiang, Yuxi Liu, Lian Duan, Yuan Xie, Qiang Xu “Modeling TSV Open Defects in 3D-Stacked DRAM”, *Proceedings of Int. Conf. on Testing (ITC 2010)*, Nov, 2010.
- [C26]. Matt Poremba, Yuan Xie, Marilyn Wolf. “Accelerating Adaptive Background Subtraction with GPU and CBEA Architecture”, *Proceedings of IEEE Workshop on Signal Processing Systems (SiPS)*, pp.305-310, Oct. 2010.
- [C27]. Jin Ouyang, Jing Xie, Matt Poremba, Yuan Xie “Design Methodology of 3D Network-on-Chip with Inductive/Capacitive-Coupling Vertical Interconnect” *Proceedings of Int. Conf. on CAD (ICCAD)*, Nov, 2010.
- [C28]. Yibo Chen, Dimin Niu, Yuan Xie, Krish Chakrabarty “Cost-Effective Integration of Three-Dimensional (3D) ICs Emphasizing Testing Cost Analysis” *Proceedings of Int. Conf. on CAD (ICCAD)*, Nov, 2010.
- [C29]. Yibo Chen, Jishen Zhao, Yuan Xie “3D-NonFAR: Three-Dimensional Non-Volatile FPGA ARchitecture Using Phase Change Memory.” *Proceedings of Intl. Symp. Low Power Electronic Devices (ISLPED)*. August, 2010. (25% acceptance rate).
- [C30]. Dimin Niu, Yiran Chen, Yuan Xie “Dual-element Memristor-Based Memory Design.” *Proceedings of Intl. Symp. Low Power Electronic Devices (ISLPED)*. August, 2010. (25% acceptance rate).

- [C31]. Jishen Zhao, Xiangyu Dong, Yuan Xie “Cost-Aware Three-Dimensional (3D) Many-Core Multiprocessor Design.” *Proceedings of Design Automation Conference (DAC)*. 2010. (24% acceptance rate).
- [C32]. Dimin Niu, Yiran Chen, Cong Xu, Yuan Xie “Impact of Process Variations on Emerging Memristor.” *Proceedings of Design Automation Conference (DAC)*. 2010. (24% acceptance rate).
- [C33]. Xiaoxia Wu, Guangyu Sun, Reetuparna Das, Yuan Xie, Jian Li, Chita R. Das “Cost-driven 3D Integration with Interconnect Layers.” *Proceedings of Design Automation Conference (DAC)*. 2010. (24% acceptance rate).
- [C34]. Yongsoo Joo, Dimin Niu, Guangyu Sun, Xiangyu Dong, Yuan Xie “Energy- and Endurance-Aware Design of Phase Change Memory Caches.” *Proceedings of Design Automation and Test in Europe (DATE)*. 2010. (25% acceptance rate).
- [C35]. Guangyu Sun, Yongsoo Joo, Yibo Chen, Yuan Xie, Yiran Chen, Helen Li “A Hybrid Solid-State Storage Architecture for Performance, Energy Consumption and Lifetime Improvement.” *Proceedings of High Performance Computer Architecture (HPCA)*. 2010. (18% acceptance rate).
- [C36]. Yuan Xie “Processor Architecture Design Using 3D Integration Technology.(Invited Paper)” *Proceedings of VLSI Design*. 2010.
- [C37]. Yibo Chen, Yu Wang, Yuan Xie, Andres Takach “Parametric Yield Driven Resource Binding in Behavioral Synthesis with Multi-Vth/Vdd Library.” *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC)*. 2010. (33% acceptance rate(115/340)) (**Best Paper Nomination**).
- [C38]. Yibo Chen, Yu Wang, Yuan Xie, Andres Takach “Minimizing Leakage Power in Aging-Bounded High-level Synthesis with Design Time Multi-Vth Assignment.” *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC)*. 2010. (33% acceptance rate(115/340)).
- [C39]. Dimin Niu, Yibo Chen, Xiangyu Dong, Yuan Xie “Energy and Performance Driven Circuit Design for Emerging Phase-Change Memory.” *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC)*. 2010. (33% acceptance rate(115/340)).
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- [C52]. Mike Debole, Guangyu Sun, Yuan Xie, Vijaykrishnan Narayanan "A Criticality-Driven Microarchitectural Three Dimensional (3D) Floorplanner." *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. (32% acceptance rate(116/355)).
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- [C63]. Xiangyu Dong, Xiaoxia Wu, Yuan Xie "Cost Analysis and Cost-driven EDA flow for 3D ICs" in *Proceedings of 3D-SIC Conference*, May. 2008.
- [C64]. Feng Wang, Guangyu Sun, Yuan Xie. "A Variation Aware High Level Synthesis Framework." *Proceedings of Design Automation and Test in Europe (DATE)*, pp.1063-1068, Mar. 2008. (198 out of 839 submissions, 23% acceptance rate)
- [C65]. Feng Wang, Xiaoxia Wu, Yuan Xie. "Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning." To appear in *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2008. **Best Paper Award.** (29% acceptance rate for regular papers (100/351)).
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- [C72]. Feng Wang, Yuan Xie, and Hai Ju. "A Novel Criticality Computation Method in Statistical Timing Analysis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1611-1616, April 2007. (208 papers accepted out of 933 submissions. 22% acceptance rate)
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- [C75]. A. Mupid, M. Mutyam, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Variation Analysis of CAM Cells." *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 333-338, March 2007. (93 papers accepted out of 292 submissions. 31% acceptance rate)
- [C76]. H. Luo, Y. Wang, K. He, R. Luo, H. Yang, Yuan Xie. "Modeling of PMOS NBTI Effect Considering Temperature Variation." *Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 139-144, March 2007. (93 papers accepted out of 292 submissions. 31% acceptance rate)
- [C77]. Feng Wang and Yuan Xie. "Soft Error Rate Analysis for Combinational Logic Using An Accurate Electrical Masking Model." *Proceedings of IEEE International Conference on VLSI Design (VLSID)*, pp. 165-170, Jan. 2007. (141 papers accepted out of 432 submissions. 32% acceptance rate)
- [C78]. Balaji Vaidyanathan, W-L. Hung, Feng Wang, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Architecting Microprocessor Components in 3D Design Space." *Proceedings of IEEE International Conference on VLSI Design (VLSID)*, pp. 103-108, Jan. 2007. (141 papers accepted out of 432 submissions. 32% acceptance rate)
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- [C81]. Qian Ding, R. Luo, H. Wang, H. Yang and Yuan Xie. "Modeling the Impact of Process Variation on Critical Charge Distribution." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 243-237, Sept. 2006. (58 regular papers accepted out of 177 submissions. 31% acceptance rate)
- [C82]. Balaji Vaidyanathan and Yuan Xie. "Crosstalk-Aware Energy Efficient Encoding for Instruction Bus through Code Compression." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 93-97, Sept. 2006. (58 papers accepted out of 177 submissions. 31% acceptance rate)
- [C83]. Xiaoxia Wu, Feng Wang, and Yuan Xie. "Analysis of Subthreshold Finfet Circuit for Ultra-low Power Design." *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 91-93, Sept. 2006.
- [C84]. S. Srinivasan, M. Prasanth, S. Karthik, Yuan Xie, N. Vijaykrishnan. "FLAW: FPGA Lifetime Awareness." *Proceedings of the 43rd Design Automation Conference (DAC)*, pp. 630-635, July. 2006. (209 papers accepted out of 865 submissions. 24% acceptance rate)
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- [C91]. Feng Wang, Yuan Xie, K. Bernstein and Y. Luo. "Dependability Analysis of Nano-scale FinFET Circuits." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 399-404, March 2006.
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- [C93]. S. Yang, W. Wolf, N. Vijaykrishnan, Yuan Xie. "Reliability-Aware SOC Voltage Islands Partition and Floorplan." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 343-348, March 2006.
- [C94]. O. Ozturk, F. Wang, M. Kandemir, Yuan Xie. "Optimal Topology Exploration for Application-Specific 3D Architectures." *Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 390-395, Jan. 2006. (135 papers accepted out of 432 submissions. 31% acceptance rate)
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- [C97]. R. Luo, H. Luo, H. Yang, Yuan Xie. "An Instruction Level Analytical Power Model for Designing Low Power SOC." *Proceedings of IEEE International Conference on ASICs*, pp.1070-1073, Oct. 2005.
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- [C102]. D. Hostetler and Yuan Xie. "Adaptive Power Management in Software Radios Using Resolution Adaptive Analog to Digital Converters." *Proceedings of IEEE International Symposium on VLSI (ISVLSI)*, pp. 186-191, May. 2005.
- [C103]. W-L. Hung, Yuan Xie, N. Vijaykrishnan, C. Addo-Quaye, T. Theocharides, M. J. Irwin "Thermal-Aware Floorplanning Using Genetic Algorithms." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 634-639, Mar. 2005. (83 out of 222 submissions, 37% acceptance rate)
- [C104]. S. Tosun, O. Ozturk, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "An ILP Formulation for Reliability-Oriented High-Level Synthesis." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 364-369, Mar. 2005. (83 out of 222 submissions, 37% acceptance rate)
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- [C106]. S. Tosun, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "Reliability-centric High-level Synthesis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1258-1263, March 2005. (176 papers accepted out of 825 submissions. 21% acceptance rate)
- [C107]. S. Yang, W. Wolf, N. Vijaykrishnan, Yuan Xie. "Power Attack Resistant Crypto Design: A Dynamic Voltage and Frequency Switching Approach." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 64-69, March 2005. (21% acceptance rate)
- [C108]. Wei-lun Hung, Yuan Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. "Thermal-Aware Allocation and Scheduling for Systems-on-a-Chip Design." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 898-899, March 2005. (21% acceptance rate)
- [C109]. Y-F Tsai, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Leakage-Aware Interconnect for On-Chip Network." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 230-231, March 2005. (21% acceptance rate)
- [C110]. J.Conner, Yuan Xie, M. Kandemir, R. Dick, G. Link. "FD-HGAC: A Hybrid Heuristic/Genetic Algorithm Hardware/Software Co-synthesis Framework with Fault Detection." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*., pp. 709-712, Jan. 2005. (99 regular papers accepted out of 692 submissions (14.3%))
- [C111]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Yuan Xie. "Low-Leakage Robust SRAM Cell Design for Sub-100nm Technologies." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*., pp. 539-544, Jan. 2005. 14.3% acceptance rate for regular papers (99 regular papers accepted out of 692 submissions (14.3%))
- [C112]. Y-F. Tsai, N. Vijaykrishnan, M. J. Irwin, Yuan Xie. "Influence of Leakage Reduction Techniques on Delay/Leakage Uncertainty." *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 374-379, Jan. 2005. (97 regular papers accepted out of 352 submissions (28%)).
- [C113]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Yuan Xie. "Accurate Stacking Effect Macro-Modeling of Leakage Power in Sub-100nm Circuits." *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 165-170, Jan. 2005. (97 regular papers accepted out of 352 submissions (28%)).
- [C114]. S. Srinivasan, A. Gayasen, N. Vijaykrishnan, M. Kandemir, Yuan Xie, M. J. Irwin. "Improving Soft-error Tolerance of FPGA Configuration Bits." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, Nov. 2004. (24% acceptance rate).
- [C115]. W-L Hung, C. Addo-Quaye, T. Theocharides, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Thermal-Aware IP Virtualization and Placement for Networks-on-Chip Architecture." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 430-437, Oct. 2004. (84 out of 226 submissions, 37% acceptance rate.)
- [C116]. Yuan Xie, L. Li, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. "Reliability-aware Cosynthesis for Embedded Systems." *Proceedings of IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP)*, pp. 41-50, Sept. 2004.
- [C117]. W-L. Hung, Yuan Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. "Total Power Optimization Through Simultaneously Multiple-VDD Multiple-VTH Assignment and Device Sizing With Stack Forcing." *Proceedings of International Symposium on Low Power Electronics and Design (ISLPED 2004)*, pp. 144-149, Aug. 2004. 34% acceptance rate)
- [C118]. W. Xu, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Design of a Nanosensor Array Architecture." *Proceedings of Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 298-303, Apr. 2004. (23 full papers accepted out of 235 submissions, 10% rate)
- [C119]. V. Degalahal, R. Ramanarayanan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "The Effect of Threshold Voltages on the Soft Error Rate." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 503-508, Mar. 2004. (49 papers accepted out of 148 submissions, 33%)
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- [C121]. Yuan Xie. "Analysis of Two Code Compression Algorithms for Embedded Systems." *Proceedings of International Conference on ASIC (ASICON)*, pp. 773-776. Oct. 2003.
- [C122]. Yuan Xie, Wayne Wolf, H. Lekatsas. "Code Compression Using Arithmetic Coding Based Variable-to-fixed Coding." *Proceedings of Data Compression Conference (DCC 2003)*, pp. 382-391, Mar. 2003.
- [C123]. Yuan Xie, W. Wolf, and H. Lektasas. "Profile-driven Code Compression." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 76-81, Mar. 2003. (152 out of 590 submissions (25%))

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- [C125]. Yuan Xie, W. Wolf, and H. Lektasas. "A Code Decompression Architecture for VLIW Processors." *Proceedings of the Thirty-Fourth International Symposium on Microarchitecture (MICRO-34)*. pp. 66-75. (29 out of 144 submissions, 20% acceptance rate)
- [C126]. Yuan Xie, W. Wolf, and H. Lektasas. "Compression Ratio and Decompression Overhead Tradeoffs in Code Compression for VLIW Architectures." *Proceedings of the Fourth International Conference on ASIC (ASICON)*. **Best Paper Award**.
- [C127]. Yuan Xie, W. Wolf. "ASICosyn: Co-Synthesis of Conditional Task Graphs with Custom ASICs." *Proceedings of the Fourth International Conference on ASIC (ASICON)*.
- [C128]. Yuan Xie, W. Wolf. "Allocation and Scheduling of Conditional Task Graphs in Co-synthesis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 620-625, Mar. 2001. (81 full papers out of 300 submissions (27%))
- [C129]. Yuan Xie, Hua Lin, Zhao Wu, W. Wolf. "CAD Techniques for Multimedia System Design." *Proceedings of Synthesis and System Integration of Mixed Technologies (SASIMI)*, Mar. 2000.
- [C130]. Yuan Xie and Wayne Wolf. "Co-synthesis with Custom ASICs." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 129-134, Jan. 2000.

Patent

- [1]. United States Patent. No.7,095,343. "Code Compression Algorithms and Architectures for Embedded Systems." Issued on August 22, 2006.

Student Supervision

Doctoral Dissertations Supervised

- 2011 **Guangyu Sun**, Ph.D. in Computer Science and Engineering
Memory Hierarchy Design using Emerging Non-volatile Memories
 First Employer: Assistant Professor at Peking University, China.
- 2011 **Xiangyu Dong**, Ph.D. in Computer Science and Engineering
Modeling and Leveraging Emerging Non-Volatile Memories for Future Computer Designs
 First Employer: Researcher at Qualcomm.
- 2011 **Yibo Chen**, Ph.D. in Computer Science and Engineering
Variation-aware Behavioral Synthesis for Nanometer VLSI circuits
 First Employer: Researcher at Synopsys Inc.
- 2011 **Mike Debole**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
Configurable Accelerators for Video Analytics
 First Employer: Post-doc at Penn State.
- 2010 **Soumya Echempati**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
Influence of Emerging Technologies on Interconnect Architectures
 First Employer: Intel.
- 2010 **Prasanth Mangalagiri**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)
A Reliability and Process Variation Aware Design flow for Platform FPGAS
 First Employer: Intel.
- 2010 **Xiaoxia Wu**, Ph.D. in Computer Science and Engineering
Design Space Exploration for 3D ICs
 First Employer: Qualcomm.
- 2009 **Balaji Vaidyanthan**, Ph.D. in Computer Science and Engineering
Reliability Analysis and Optimization for Nanoscale System-on-Chip Design
 First Employer: TSMC, Taiwan.
- 2008 **Feng Wang**, Ph.D. in Computer Science and Engineering
Design Automation Techniques to Mitigate Process Variations
 First Employer: Qualcomm.

- 2007 **Yu Wang**, Ph.D. in Electronic Engineering, Tsinghua University (co-advised with Prof. Huazhong Yang)
Optimization for the Leakage Current and Reliability in Digital Integrated Circuits
Current Job: Assistant Professor in Tsinghua University.
- 2006 **Wei-lun Hung**, Ph.D. in Computer Science and Engineering
Designing Cool Chips: Low Power and Thermal-Aware Design Methodologies
Current Employer: Sun Microsystems.

Postdoctor Supervised

- Post-Doc **Yongsoo Joo**, Now Assistant Professor at Ewha University, Korea.
- Post-Doc **Lian Duan**, Ph.D. from Peking University, China.

Master Thesis Supervised

- 2008 **Paul Falkenstern**, M.S. in Computer Science and Engineering
Design Automation Tools for 3D ICs
First job: Lockheed Martin Inc.
- 2007 **Han-wei Chen**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)
Impact of Circuit Degradation on Design Security of Field Programmable Devices
Now graduate student at University of Texas at Austin.
- 2007 **Charles Addo-Quaye**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)
Thermal-Aware Placement and Virtualization for Three Dimensional Network-on-Chip Designs
Now Ph.D. student at PennState.
- 2007 **Melvin Eze**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)
Delay and Energy Efficient Data Transmission for On-Chip Buses
Now Ph.D. student at PennState.
- 2006 **Yinkun Xue**, M.S. in Computer Science and Engineering
Providing Energy-Aware Map Services to Mobile Devices
First job: Siemens Inc.
- 2005 **Thomas Richardson**, M.S. in Computer Science and Engineering
Analysis and Design of Scalable SoC Interconnects
First job: Avallink Inc.

Current Students

- Ph.D. **Jin Ouyang**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2012
- Ph.D. **Dimin Niu**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2013
- Ph.D. **Tao Zhang**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2013
- Ph.D. **Jing Xie**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2014
- Ph.D. **Jishen Zhao**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2014
- Ph.D. **Cong Xu**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2014
- Ph.D. **Qiaosha Zou**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2015
- Ph.D. **Matthew Poremba**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2015
- Ph.D. **Hsiang-Yun Cheng**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2015
- Ph.D. **Jue Wang**, Ph.D. in Computer Science and Engineering, expected graduation date: 1/2016
- Ph.D. **Jia Zhan**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2016
- Ph.D. **Ping Chi**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2016

Teaching

Semester	Course	Course Evaluation
Fall 2003	CSE 597A <i>Modern VLSI Design</i>	6.29 out of 7
Fall 2003	CSE 598C <i>Reliable and Low Power Design</i>	6.13 out of 7

Spring 2004	CSE 477 <i>VLSI Digital Circuits</i>	5.50 out of 7
Fall 2004	CSE 578 <i>CAD Tools</i>	5.91 out of 7
Spring 2005	CSE 477 <i>VLSI Digital Circuits</i>	5.17 out of 7
Fall 2005	CSE 578 <i>CAD Tools</i>	6.78 out of 7
Spring 2006	CSE 331.1 <i>Computer Organization and Design</i>	5.54 out of 7
Spring 2006	CSE 331.2 <i>Computer Organization and Design</i>	6.11 out of 7
Fall 2006	CSE 578 <i>CAD Tools</i>	5.88 out of 7
Fall 2006	CSE 431 <i>Introduction to Computer Architecture</i>	6.31 out of 7
Spring 2007	CSE 477 <i>VLSI Digital Circuits</i>	6.53 out of 7
Fall 2008	CSE 578 <i>CAD Tools</i>	6.53 out of 7
Spring 2008	CSE 411 <i>VLSI Digital Circuits</i>	6.29 out of 7
Fall 2009	CSE 578 <i>CAD Tools</i>	6.50 out of 7
Spring 2009	CSE 331 <i>Computer Organization and Design</i>	5.15 out of 7
Spring 2010	CSE 411 <i>VLSI Circuits Design</i>	6.19 out of 7
Spring 2010	CSE 598K <i>Advanced Topics in Computer Hardware Design</i>	6.83 out of 7

Department average: 5.17; College average:5.28

Short Courses

06/2009	[1]. One-week Course in China DragonStar Program, Chinese Academy of Science. “Advanced Modern Architecture and VLSI Design”	Beijing, China
05/2007	[2]. 3-week Summer Short Course, Tsinghua University. “Advanced VLSI Design”	Beijing, China
08/2006	[3]. 3-week Summer Short Course, Tsinghua University. “Advanced VLSI Design”	Beijing, China
05/2004	[4]. 2-day Industrial Short Course, Pittsburgh Digital Greenhouse. “Design of Reliable Power-Efficient Systems”	Pittsburgh, PA
01/2004	[5]. 2-day Industrial Short Course, Pittsburgh Digital Greenhouse. “Design of Reliable Power-Efficient Systems”	Pittsburgh, PA

Tutorials

03/2011 DATE-11	[1]. Full-day Tutorial: “Manufacturing, CAD and Thermal-Aware Design for 3-D MPSoCs” <i>with David Atienza (EPFL), Ruchir Puri (IBM), Tanay Karnik (Intel), Patrick Leduc (CEA-LETI)</i> IEEE/ACM Design Automation and Test in Europe, 2011
11/2010 ICCAD-10	[2]. Half-day Tutorial: “Manufacturing, CAD and Thermal-Aware Design for 3-D MPSoCs” <i>with David Atienza (EPFL), Sani Nassif (IBM), Ayse K. Coskun (Boston University)</i> IEEE/ACM Intl. Conf. on CAD
6/2010 DAC-10	[3]. Full-day Tutorial: “3D IC: New Dimensions in IC Design” <i>with Ruchir Puri (IBM), Tanay Karnik (Intel), David Atienza (EPFL), Paul Marchal (IMEC)</i> IEEE/ACM Design Automation Conference
3/2010 SC-09	[4]. Half-day Tutorial: “The Impact of Emerging Technology on Computer System Design” <i>Norm Jouppi (HP Labs) and Yuan Xie</i> Architecture Support for Programming Language and Operating Systems (ASPLOS) 2010
1/2010 ASPDAC-10	[5]. Full-day Tutorial: “3D Integrated Circuit Design” <i>with Ruchir Puri (IBM), Paul Franzon (NCSU) and Sachin Sapatnekar (UMN)</i> ACM Asia and South-Pacific Design Automation Conference
1/2010 VLSI Design-10	[6]. Embedded Tutorial: “Processor Design using 3D Integrations” IEEE Symposium on VLSI Design Conference

- 12/2009
MICRO-2009 [7]. **Half-day Tutorial: “Integrated Multi-core Modeling”**
with Pradip Bose (IBM) and Eren Kursun (IBM)
42nd International Symposium on Microarchitecture
- 11/2009
SCA-09 [8]. **Half-day Tutorial: “The Impact of Emerging Technology on Computer System Design”**
Norm Jouppi (HP Labs) and Yuan Xie
Supercomputing 2009
- 04/2009
VLSI/DAT-09 [9]. **Half-day Tutorial: “3D Integration”**
Yuan Xie
International Symposium on VLSI/DAT
- 06/2008
ISCA-08 [10]. **Half-day Tutorial: “3D Integration for Microarchitectures”**
organized with G. Loh (Gatech)
International Symposium on Computer Architecture
- 5/2006
GLSVLSI-08 [11]. **Half-day Tutorial: “Technology, EDA, and Architecture for Emerging 3D Integration”**
with Syed Alam (Freescale), Mike Ignatowski (IBM)
Greatlake Symposium on VLSI (GLSVLSI), 2008
- 12/2006
MICRO-06 [12]. **Half-day Tutorial: “3D Integration for Microarchitectures”**
with K. Bernstein (IBM), B. Black (Intel), and G. Loh (Gatech)
International Symposium on Microarchitecture (MICRO-39)
- 8/2006
VLSI06 [13]. **Half-day Tutorial: “Thermal-Aware Design Techniques for Nanometer VLSI Chips”**
The 17th VLSI Design/CAD Symposium
- 10/2005
ASIC05 [14]. **Half-day Tutorial: “Thermal-Aware Design Techniques for Nanometer VLSI Chips”**
The 6th International Conference on ASIC (ASIC05)
- 06/2005
ISCA05 [15]. **Half-day Tutorial: “Robust Systems Design from Unreliable Components”**
with S. Mitra (Intel), L. Spainhower (IBM), and N. Vijaykrishnan (PSU)
International Symposium on Computer Architecture (ISCA)
- 01/2005
ASP05 [16]. **Half-day Tutorial: “Designing Reliable Circuit in the Presence of Soft Errors”**
Asia-South-Pasific Design Automation Conference (ASP-DAC)
- 10/2004
ASP04 [17]. **Full-day Tutorial: “Computing in the Presence of Soft Errors ”**
with N. Vijaykrishnan (PSU)
Intl. Conf. on Architectural Support for Programming Languages and Operating Systems

Invited Talks

- 6/2011 [1]. Invited talk, **IMAPS Northern California Chapter** **San Jose, CA**
“3D IC Design and Cost Implication”
- 5/2011 [2]. Invited talk, **Chinese Academy of Science** **Beijing, China**
“Emerging NVM technologies for Exascale Computing”
- 3/2011 [3]. Invited talk, **AMD Research Labs** **Seattle, WA**
“3D Architecture and Application”
- 3/2011 [4]. Invited talk, **Global Semiconductor Alliances (GSA)** **San Jose, CA**
“Cost, Architecture, and Applications for 3D Integration”
- 12/2010 [5]. Invited talk, **National Tsing Hua University** **Hsinchu, Taiwan**
“3D IC EDA and Architecture and Application”
- 11/2010 [6]. Invited talk, **Yuan Ze University** **Taipei, Taiwan**
“3D IC EDA and Architecture”
- 11/2010 [7]. Invited talk, **National Chiao-Tung University** **Hsinchu, Taiwan**
“Emerging Memory Technologies and the Impact on Computer System Design”
- 10/2010 [8]. Invited talk, **National Cheng Kung University** **Tainan, Taiwan**
“Emerging Memory Technologies and the Impact on Computer System Design”
- 10/2010 [9]. Invited talk, **National Cheng Kung University** **Tainan, Taiwan**
“Design Challenges for 3D ICs”
- 09/2010 [10]. Invited talk, **Global Semiconductor Alliance (GSA)** **San Jose, CA**
“ System Level Cost Analysis and Design Exploration for 3D ICs”

9/2010	[11]. Invited talk, Industrial Technology Research Institute(ITRI) "Design Challenges for 3D ICs"	Hsinchu, Taiwan
9/2010	[12]. Invited talk, Korea Advanced Institute of Science and Technology (KAIST) University Korea "Design Challenges for 3D ICs"	Daejeon,
7/2010	[13]. Invited talk, China Computer Federation "Emerging Technologies and the Impact on Computer System Design"	Beijing, China
6/2010	[14]. Invited talk, Qualcomm "Emerging Memory Technologies and the Impact on Computer System Design"	San Diego, CA
5/2010	[15]. Invited talk, IMEC (Interuniversity Microelectronic Centre) "Emerging Memory Technologies and the Impact on Computer System Design"	Leuven, Belgium
5/2010	[16]. Invited talk, ETH Zurich "3D IC Design, EDA, and Architecture"	Zurich, Switzerland
4/2010	[17]. Invited talk, Carnegie Mellon University "Emerging Memory Technologies and the Impact on Computer System Design"	Pittsburgh, PA
4/2010	[18]. Invited talk, Princeton University "Emerging 3D and NVM Technologies and the Impact on Computer System Design"	Princeton, NJ
1/2010	[19]. Invited talk, Intel "Modeling, Architecture, and Application for Emerging Memory Technologies"	Hiilsboro, Oregon
1/2010	[20]. Invited talk, Tsinghua University "Modeling, Architecture, and Application for Emerging Memory Technologies"	Beijing, China
1/2010	[21]. Invited talk, Intel "Modeling, Architecture, and Application for Emerging Memory Technologies"	Bengalore, India
11/2009	[22]. Invited talk, Intel "Design Methodologies and Architecture for 3D ICs"	Hiilsboro, Oregon
10/2009	[23]. Invited talk, IBM T.J. Watson Research Lab "Design Methodologies and Architecture for 3D ICs"	Yorktown, NY
8/2009	[24]. Invited talk, 9th International Forum on Embedded MPSoC and Multicore "Enabling Many-Core Design via 3D Stacking"	Savannah, GA
6/2009	[25]. Invited talk, National Chiao-Tung University (NCTU) "Design Methodologies and Architecture for 3D ICs"	HsinChu, Taiwan
04/2009	[26]. Invited talk, COOLCHIPS XII "3D Microarchitecture"	Yokohama, Japan
04/2009	[27]. Invited talk, Industrial Technology Research Institute(ITRI) "3D IC Design"	Hsinchu, Taiwan
02/2009	[28]. Invited talk, Semiconductor Research Corporation "3D IC Design and Architecture"	Raleigh, NC
02/2009	[29]. Invited talk, ECE Department, Duke University "New Dimensions in 3D IC Design"	Durham, NC
09/2008	[30]. Invited talk, ECE Department, Univ. of Texas in Austin "Potential and Challenges in 3D IC Design"	Austin, TX
09/2008	[31]. Invited talk, IBM Austin Research Lab "Potential and Challenges in 3D IC Design"	Austin, TX
09/2008	[32]. Invited talk, Freescale "Potential and Challenges in 3D IC Design"	Austin, TX
09/2008	[33]. Invited talk, National Tsinghua University "Reliable Circuits Design on Top of Unreliable Hardware"	Taiwan
07/2008	[34]. Invited talk, National Taiwan University "Design Challenges in Three-dimensional IC Design"	Taiwan
07/2008	[35]. Invited talk, National Tsinghua University "Design Challenges in Three-dimensional IC Design"	Taiwan

06/2008	[36]. Invited talk, Beijing BeiHang University “Potential and Challenges in 3D IC Design”	Beijing, China
06/2008	[37]. Invited talk, Harbin Institute of Technology. “Design Challenges in Three-dimensional IC Design”	China
11/2007	[38]. Invited talk, Qualcomm Inc. “Three-dimensional IC Design”	San Diego, CA
11/2007	[39]. Invited talk, MetaRAM Inc. “Three-dimensional IC Design”	San Jose, CA
10/2007	[40]. Invited talk, Georgia Institute of Technology. “Variation-aware Multi-Processor System-on-Chip (MPSOC) Design”	Atlanta, GA
10/2007	[41]. Invited tutorial, Seagate Technology LLC. “3D IC Design Tutorial”	Bloomington, MN
10/2007	[42]. Invited talk, SEMATECH 3D workshop . “3D Architecture Design”	Albany, New York
09/2007	[43]. Invited talk, KAIST University. “Design Space Explorations for 3D ICs”	Daejeon, Republic of Korea
05/2007	[44]. Invited talk, Honda Research Institute. “Design Automation for Three-dimensional ICs”	Tokyo, Japan
05/2007	[45]. Invited talk, Peking University. “New Dimension for High Performance”	Beijing, China
04/2007	[46]. Invited talk, IMEC (Interuniversity Microelectronics Centre). “The Challenges of Designing 3D Microarchitectures”	Leuven, Belgium
01/2007	[47]. Invited talk, Dagstuhl Seminar on Power-Aware Computing Systems. “Thermal Challenges in 3D Microarchitecture Design”	Dagstuhl, Germany
11/2006	[48]. Invited talk, The 3rd Annual 3-D Architectures Conference. “Design Space Exploration for 3D IC Design”	San Francisco, CA
10/2006	[49]. Invited talk, University of Pittsburgh. “The Challenges of Designing 3D Microarchitectures”	Pittsburgh, PA
08/2006	[50]. Invited talk, Hongkong University of Science and Technology. “3D Microarchitecture Design”	Hong Kong, China
08/2006	[51]. Invited talk, Intel China Research Center. “3D Microarchitecture Design”	Beijing, China
03/2006	[52]. Invited talk, IBM T.J.Watson Research Center. “The Challenges of Designing 3D Microarchitectures”	Yorktown, NY
10/2005	[53]. Invited talk, IBM China Research Lab. “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	Shanghai, China
10/2005	[54]. Invited talk, Peking University. “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	Beijing, China
10/2005	[55]. Invited talk, Shanghai Jiaotong University. “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	Shanghai, China
05/2005	[56]. Invited talk, Syracuse University. “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	Syracuse, NY
10/2005	[57]. Invited talk, University of South Florida. “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	Tempa, FL
10/2004	[58]. Invited talk, IBM Circuit Education Seminar. “Soft Errors: Interactions with Power Optimizations”	

Service and Activities

Professional Community

2009- Committee Member, IEEE Design Automation Technical Committee (DATC).
 2007- Chair of Student Technical Activities on the Technical Activities Board, IEEE Computer Society.
 2010- ACM Distinguished Speaker.
 2011-2013 IEEE Computer Society Distinguished Visitor.

Editorial

2010- Associate Editor, ACM Journal of Emerging Technologies in Computer Systems (JETC)
 2010- Associate Editor, IEEE Transactions on CAD (TCAD).
 2010- Associate Editor, IEEE Design and Test of Computers.
 2008- Associate Editor, IET Computers and Digital Techniques (IET CDT).
 2007- Associate Editor, IEEE Transactions on VLSI Systems (TVLSI).
 2009 Guest Co-Editor, IEEE Design and Test of Computers, Special Issues on 3D ICs.
 2009 Guest co-Editor, IET Computers and Digital Techniques (IET CDT), Special Issues on 3D ICs.
 2007 Guest co-Editor, ACM Journal of Emerging Technologies for Computer Systems (JETC), Special Issues on 3D ICs.

TPC Chair/Co-Chair in Conferences/Workshops:

2013 Technical Program Chair for International Symposium on Low Power Electronic Devices (ISLPED)
 2013 Technical Program Chair for Asia and South Pacific Design Automation Conference
 2012 Technical Program Vice Chair for Asia and South Pacific Design Automation Conference
 2011 General Co-Chair for Greatlake Symposium on VLSI (GSVLSI), Laussane, Switzerland
 2011 Technical Program Co-Chair for MPSOC Forum, Grenoble, France
 2010 General Co-Chair for Workshop on Design for 3D Integration, Laussane, Switzerland
 2009 Program Co-Chair for International Symposium on VLSI (ISVLSI), Orlando, Florida
 2009 Program Co-chair, First workshop for Three-dimensional Architectures, in conjunction with High Performance Computer Architectures(HPCA)
 2008 Program Chair for 3D IC and Architecture Workshop, Hsin Chu, Taiwan.
 2009 Program Subcommittee Chair for Emerging Technology Track, and TPC member, Design Automation and Test in Europe(DATE)

TPC member in Conferences/Workshops:

2012 Program Committee Member, The 39th International Symposium on Computer Architecture (ISCA)
 2012 Program Committee Member, IEEE International Symposium on High Performance Computer Architecture (HPCA)
 2011, 2008 Program Committee Member, IEEE/ACM Design Automation Conference (DAC)
 2009-2010 Program Committee Member, International Conference on Computer-Aided Design(ICCAD)
 2008-2012 Sub-Committee Chair on Emerging Technology, Design Automation and Test in Europe(DATE)
 2008-2011 Program Committee Member, Asia and South Pacific Design Automation Conference (ASP-DAC)
 2010 Program Committee Member, IFIP/ACM VLSI-SOC Conference
 2010 Student Award Committee Co-Chair, High Performance Computer Architecture (HPCA)
 2009,2006 Program Committee Member, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
 2009-2010 Program Committee Member, IEEE/ACM International Conference on Computer Design (ICCD)
 2008-2011 Program Committee Member, IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)
 2008 Program Committee Member, ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES 2008)

2008 Program Committee Member, Workshop on Interaction Between Compilers and Computer Architectures (INTERACT-12)

2008 Program Committee Member, International Conference on VLSI Design (VLSID 2008)

2007 Session Chair, International Conference on Computer Aided Design (ICCAD)

2007 Program Committee Member, International Workshop on Trustworthiness, Reliability and Services in Ubiquitous and Sensor Networks (TRUST 2007)

2006-2007 Program Committee Member, International Conference on Communications, Circuits, and Systems

2007-2008 Program Committee Member, Financial Chair (2008), International Symposium on Low Power Electronics and Design

2007-2008 Program Committee Member, IEEE International Symposium on Circuits and Systems (ISCAS 2007, 2008)

2007 Program Committee Member, ACM International Conference on Computing Frontiers (CF 2007)

2007-2008 Program Committee Member, EDAA/PhD Forum, in conjunction with DATE 2007/2008

2006-2009 Program Committee Member, Finance Chair (2008,2009), Greatlake Symposium on VLSI (GLSVLSI)

2006 Program Committee Member, International Conference on Nano-networks (Nano-Net 2006)

2006 Program Committee Member, IFIP International Conference on Embedded and Ubiquitous Computing

2005 Program Committee Member, International Conference on Embedded Software and System (ICCESS'05)

2005 Tutorial Chair, ACM Conference on Embedded Software (EMSOFT 2005)

2004-2005 Session Chair, International Conference on Computer Design

2003 Session Chair, International Conference on ASICs

Services to the University

2007- IEEE Computer Society Advisor, PennState

2007- Student Advisor, Engineering Advising Center, College of Engineering, PennState

2006-07 Ph.D. Candidacy Exam Chair, Computer Science Engineering Dept, PennState

2005-06 Department Colloquium Chair, Computer Science Engineering Dept, PennState

2003-05 Graduate Committee, Computer Science Engineering Dept, PennState