

ANALYSIS OF SUBTHRESHOLD FINFET CIRCUITS FOR ULTRA-LOW POWER DESIGN

Xiaoxia Wu Feng Wang Yuan Xie
 CSE Department, The Pennsylvania State University
 University Park, PA 16802, USA
 {xwu, fenwang, yuanxie}@cse.psu.edu

Abstract—In this paper, we first explore sub-threshold FinFET circuits design space, finding their optimal power supply point for minimum energy consumption. We then study soft error vulnerability in sub-threshold region. Our experiments indicate that the energy consumption in sub-threshold region can achieve 4 orders of magnitude energy saving. Compared to bulk CMOS technology, FinFET circuits have lower functional power supply and lower optimal energy consumption in sub-threshold region. In addition, FinFET has better soft error immunity in sub-threshold region.

I. INTRODUCTION

For some applications, such as portable wireless devices, medical devices, and sensor network nodes, using lower supply voltage can achieve lower energy consumption while still maintain acceptable operation speed. The minimum energy consumption is realized in sub-threshold region, in which the supply voltage (V_{dd}) is lower than the threshold voltage (V_{th}) of transistor. [1][2][3] In this region, off-state leakage can be utilized as the operating current to realize ultra-low power purpose.

In the past, sub-threshold bulk CMOS circuits have been extensively studied for ultra-low power design. Recently, Kim et al. have shown that a device with ideal sub-threshold slope is the optimal device for sub-threshold operation due to its smaller gate capacitance and larger operating current for a given off-current. [4] Double-gate FinFET is considered one of the most promising structures. [5]

In this paper, we first study ultra-low power design for FinFET circuits. Our experiments show that FinFET circuits have lower functional supply and lower energy consumption than CMOS circuits in sub-threshold region. We also study soft error vulnerability in sub-threshold region. Our analysis indicates that FinFET has better soft error immunity in sub-threshold region compared to its CMOS counterparts.

II. OPTIMAL OPERATING POINT ANALYSIS

A. FinFET Structure

Figure 1 shows the structure of multi-fin double-gate FinFET device. [6] Current flow is parallel to the wafer plane. The thickness (T_{si}) of a single fin equals to silicon channel thickness. Each fin provides of device width, where H is the height of the each fin. We use HSPICE to study FinFET and bulk CMOS circuit behavior, using Predictive Technology Model for 32 nm FinFET and 32 nm bulk CMOS technology. (<http://www.eas.asu.edu/~ptm/>)

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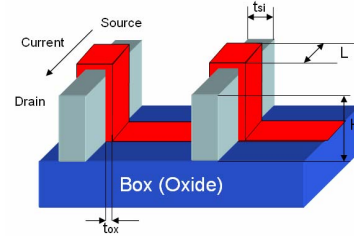


Fig. 1. FinFET structure

B. Sub-threshold Circuit

In sub-threshold region, a model of active energy dissipated in a circuit is

$$E_{active} = \alpha C V_{dd}^2$$

Where α is the activity factor, C is the total switching capacitance of the circuit, and V_{dd} is the power supply. The standard expression for sub-threshold current is

$$I_{sub} = K e^{\frac{V_{gs}-V_{th}}{nV_T}} (1 - e^{-\frac{V_{ds}}{V_T}})$$

Where K is a technology related factor, V_T is the thermal voltage which is temperature dependent and V_{th} is the threshold voltage. Hence, the total energy E_{total} is the sum of dynamic and leakage energy

$$E_{total} = E_{active} + E_{leakage} = \alpha C V_{dd}^2 + V_{dd} I_{leakage} T_{delay}$$

Where T_{delay} is delay of a circuit, $I_{leakage}$ is leakage current. In sub-threshold region, dynamic energy decreases because of the reduction of supply voltage. The sub-threshold current becomes the operating current, causing the delay to increase exponentially with voltage scaling. Since leakage energy is linear with the circuit delay, it will increase with supply-voltage reduction. While supply voltage is reduced to sub-threshold region, when the reduction of dynamic energy cannot compensate the increase of the leakage energy, a minimum energy point is reached.

C. Analysis Methodology and Result

We use a 30-stage inverter chain and a 8-bit ripple carry adder to simulate the energy dependence on supply voltage. In 8-bit ripple carry adder, the delay is measured using worst case delay from the least bit carryin to maximum bit sum.

The energy for FinFET and CMOS at different voltages is showed in Figure 2 and Figure 3. In both figures, the dynamic energy reduces while the leakage energy increases

with voltage reduction in the sub-threshold region. Hence, the summation of leakage energy and dynamic energy will be minimal at the optimal power supply point. In Figure 2, the optimal supply voltage and the minimum energy are 120mV and 1.32e-16J for 32nm FinFET inverter chain, 230mV and 5.33e-16J for 32nm bulk CMOS inverter chain. In Figure 3, the optimal supply voltage and the minimum energy are 170mV and 8.92e-16J for 32nm FinFET 8-bit adder, 300mV and 3.46e-15J for 32nm bulk CMOS 8-bit adder. For FinFET circuits, the energy in sub-threshold is 4 orders lower than normal region. CMOS inverter chain (8-bit adder) will not functional when the supply voltage is lower than 150mV (200mV), while FinFET inverter chain (8-bit adder) still works under 50mV (100mV) power supply.

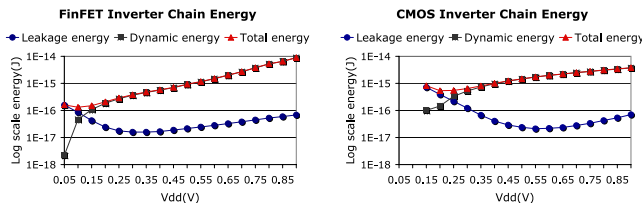


Fig. 2. FinFET and CMOS inverter chain Energy

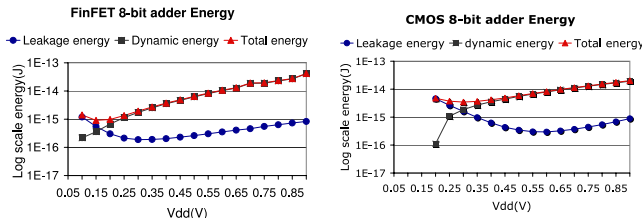


Fig. 3. FinFET and CMOS 8-bit adder Energy

The delays for FinFET and CMOS circuits at different voltages are shown in Figure 4. Under the same power supply voltage, the delays of FinFET circuits are much smaller than those of CMOS circuits, which means FinFET circuits can work faster than CMOS circuits. This is because FinFET has smaller gate capacitance and larger operating current. This trend is more obvious in sub-threshold region, and indicates FinFET is more suitable for sub-threshold region. In conclusion, FinFET circuits can achieve lower functional power supply, lower optimal energy consumption, and higher speed in sub-threshold region compared to its CMOS counterparts.

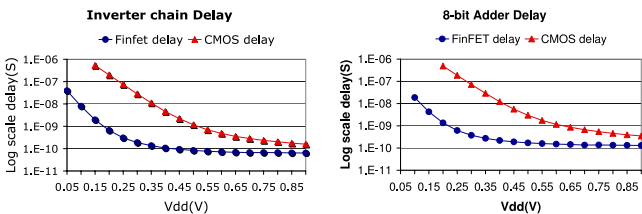


Fig. 4. Delay Comparison at different Vdd for FinFET and CMOS circuits

III. SOFT ERROR VULNERABILITY ANALYSIS

When supply voltage decreases, soft error vulnerability increases.[7] The soft error analysis is performed on the

inverter chain using 32nm FinFET and 32nm bulk CMOS technology. The current pulse is injected at the output node of the first stage. We assume a soft error occurs when the transient voltage pulse at the output of the second stage reaches a value of $V_{dd}/2$.

We study the soft error vulnerability under nominal supply voltage 0.9V and sub-threshold supply voltage 0.2V and 0.3V. Figure 5 shows the critical charge dependence on power supply voltage. Critical charge decreases with the reduction of power supply in both technologies, showing that the circuit is more vulnerable to soft error in sub-threshold region. Additionally, it shows that under the same voltage supply the critical charge in FinFET is larger than in CMOS. In sub-threshold region, the critical charge in FinFET is almost two times larger than in CMOS, indicating that FinFET has higher immunity to soft error.

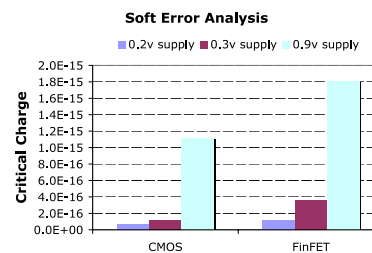


Fig. 5. Critical charge in FinFET and Bulk CMOS technology

IV. CONCLUSION

Double-gate FinFET has been proposed as a promising alternative for bulk CMOS technology to continue the technology scaling. This paper studies sub-threshold FinFET design and performs soft error analysis for sub-threshold FinFET circuits. The result shows that FinFET circuits can achieve lower functional voltage supply and lower optimal energy consumption compared to CMOS circuits. In addition, FinFET has better immunity to soft error in sub-threshold region. Hence, FinFET is more suitable and reliable for ultra-low power circuit design.

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