Dependability Analysis of Nano-scale FinFET circuits

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Abstract

FinFET technology has been proposed as a promising alternative for deep sub-micro bulk CMOS technology, because of its better scalability. Previous work have studied the performance or power advantages of FinFET circuits over bulk CMOS circuits. This paper provides the dependability analysis of FinFET circuits, studying the soft error vulnerability of FinFET circuits and the impact of process variation. Our experiments compare FinFET circuits against bulk CMOS circuits in both 32nm and 45nm technologies, showing that FinFET circuits have better dependability and scalability, which is indicated by better soft error immunity and less impact of process variation. It is concluded that FinFET-based circuit design is more robust than the bulk CMOS based circuit design.

1. Introduction

Conventional bulk CMOS scaling beyond 45nm is severely constrained by short channel effects and vertical gate insulator tunneling [9]. Double-gate FinFET technology [3][7][12[15] has been proposed as a very promising candidate to circumvent the conventional bulk CMOS scaling constraint, by changing the device structure in such a way that MOSFET gate length can be scaled further even with thicker oxide, so that we can continue scaling beyond the limit of conventional bulk CMOS. Figure 1 shows a multi-fin FinFET structure, which will be explained in Section 3.

One of the grand challenges for nano-scale VLSI designers is guaranteeing dependability. Shrinking geometries, lower supply voltage, and higher frequencies, all have a negative impact on circuit dependability: the occurrences of soft errors increases due to these factors, and higher levels of device parameter variations change the design problem from deterministic to probabilistic. Consequently, reducing soft error rate and mitigating the impact of process variation are becoming increasingly critical.

Both logic and SRAM FinFET technologies have been previously demonstrated [3][7]. Previous work have shown the performance and power advantage of FinFET circuits over bulk CMOS [2][3][7][12][15]. However, we haven't seen a comprehensive analysis for dependability of FinFET circuits. In this paper, we provide the reliability and scalability analysis for FinFET circuits, showing that FinFET circuits have better soft error immunity, as well as less impact of process variation on the performance, comparing against the bulk CMOS counterparts.

The paper is organized as follows: Section 2 provides a survey of related work. Section 3 describes the FinFET structure and the device model parameters. Section 4 describes the methodology to compare the soft error vulnerability of FinFET circuits against bulk CMOS circuits. Section 5 discusses the impact of process variation on both FinFET circuits and bulk CMOS circuits. Experimental result for 32-nm and 45-nm FinFET and bulk CMOS circuits are presented in both Section 4 and Section 5. Finally, Section 6 concludes the paper.

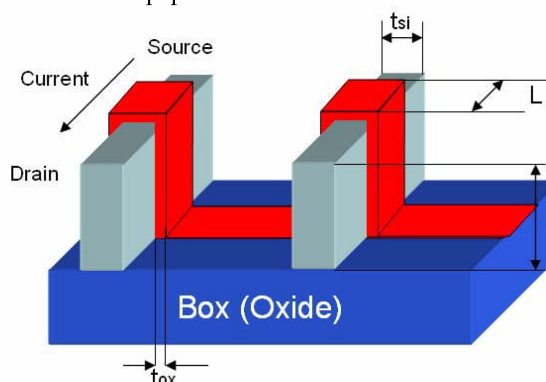

Fig. 1. Multiple-fin FinFET structure [15]

2. Related Work

FinFET device [5] was proposed as an elegant implementation of double-gate FET [9] , which enables continuous technology scaling. Rainey *et al.* [7] have demonstrated the feasibility of FinFET logic implementation in 180nm, by showing inverter-chain

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operation for the first time. FinFET SRAM behavior was investigated by Joshi *et al.* [3] and it has been shown to exhibit higher performance and lower power compared against conventional planar PD-SOI. IBM was the first to convert an existing microprocessor design in a 100 nm FinFET technology and ensure its functionality [6].

Even though FinFET device and circuits design consideration have been studied recently [1] [2][3][6][7][12][15], most of the work focused on the performance or power advantage that FinFET circuits can provide. Soft error vulnerability and process variation analysis for FinFET circuits are necessary since reliability is also an important design goal for nano-scale VLSI design. In [15], the design space exploration for performance power and reliability is performed for a 65nm FinFET SRAM. Guo et.al [12] showed that FinFET-based SRAM design has a 30% improvement of noise margin over that of the bulk CMOS SRAM. In this paper, we study the soft error vulnerability as well as the impact of process variation for FinFET circuits.

3. FinFET Structure and Device Model Parameter

Fig. 1 shows the structure of multi-fin double-gate FinFET devices [15]. Double gate FinFET consists of two SOI gates connected together. The thickness (Tsi) of a single fin equals to silicon channel thickness. The current flows from the source to drain along the wafer plan. Each fin provides 2H of device width, where H is the height of the each fin. For the FinFET devices, widths are quantized into units of the fins. Large width of device is obtained by using multiple fins.

We use Synopsys circuit simulator HSPICE to study FinFET circuits behavior. The FinFET devices in 32nm and 45nm, and the corresponding bulk CMOS counterparts, are modeled using Predictive Technology Model [8]. Table 1 shows the nominal 45nm and 32 nm device parameters that is used in our simulation.

Table 1. Nominal 32nm and 42nm FinFET device parameters

Parameter	32 nm FinFET	45nm FinFET
Supply Voltage (Vdd)	0.9 V	1.0 V
Physical Gate Length(L)	32nm	45nm
Physical Oxide Thickness(Tox)	1.4nm	1.5nm
Body thickness(Tsi)	8.6nm	8.4nm
Fin-Height(H)	65nm	65nm

4. Soft Error Vulnerability Analysis for FinFET circuit

In this section, we describe the methodology to conduct soft error vulnerability analysis for FinFET circuits. Section 4.1 gives a brief introduction on soft error and the simulation method; Section 4.2 shows the soft error vulnerability analysis method for bulk CMOS and FinFET logic and SRAM. Section 4.3 presents the experimental results.

4.1 Soft Error Background and the Simulation Methodology

Alpha particles from the packaging materials, high energy neutrons from cosmic radiations and the interaction of cosmic ray thermal neutron are three major sources of the radiations that induce soft error, which is also called Single Event Upset (SEU) [10]. A soft error occurs, when a particle strike at a specific node in a circuit, which results in a transient voltage pulse can cause a bit flip in the SRAM cell or be captured by the latch. The critical charge is defined as the minimum charge collected for a specific voltage transient occurs at the gate output, which can cause a bit flip in the SRAM cell or propagate through logic chains to the primary output and be latched by storage elements or. This concept of critical charge is generally used to estimate the sensitivity of SEU for both the SRAM circuits and combinational circuits [10][11]. A smaller critical charge value indicates higher soft error rate (SER).

Similar to previous work [10][11], a double exponential current source model is used to model a SEU at a node:

$$I(t) = I_{peak} \times (e^{-t/\tau_a} - e^{-t/\tau_b}) \quad (1)$$

where $I_{peak} = \frac{Q}{\tau_a - \tau_b}$, in which Q is the charge collected as a result of particle strike, τ_a is the collection time-constant, and τ_b is the ion-track

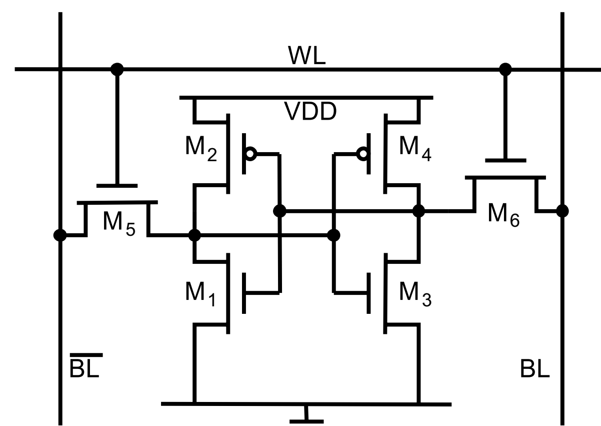

Fig. 2. 6-T SRAM Cell

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establishment time-constant [10]. τ_a and τ_b are the constants which depend only on process-related factors.

4.2 Soft Error Vulnerability Analysis

The analysis is performed on the SRAM cells design using FinFET and bulk CMOS. Conventional 6T-SRAM cell is shown in Fig.2. It consists of two NMOS pass gate transistors, two pull up PMOS transistors and two pull down NMOS transistors. To ensure robust read stability, the transfer ratio equals to 2 for both bulk CMOS based SRAM cell and FinFET-Based SRAM cell [16]. In other words, the pull down FinFET, M1 and M3, consists of two fins while the pass gate transistors, M5 and M6, consists of a single fin channel. For the bulk CMOS based SRAM cell, the W/L of pull down NMOS is twice of the W/L of pass gates [16]. To measure the critical charge, the current source shown in Equation (1) is injected at the storage node and the I_{peak} is swept until the bit flip occurs, the critical charge is then measured to be the soft error vulnerability metric. Note that here we assume that the charge collection for bulk CMOS device and FinFET device are the same.

FO4 (Fanout-of-4) logic gate is commonly used to characterize the specific technology. The analysis of the susceptibility of combination logic to soft errors is performed using FO4 inverter, which is an inverter with fan out of 4 inverters. The current pulse is injected at the output node of the inverter and the resultant transient voltage pulse is observed. We assume a soft error occurs when the transient voltage reaches a value of Vdd/2.

The analysis of soft error propagation in logic chain is performed using an inverter chain. 8 stage FO4 inverter chain is used in our experiments as shown in Fig.3. Current pulse is injected at the output of the first inverter and we measure the transient voltage propagated to the output of the logic chain. *Electrical masking* happens when the voltage transient resulting from a particle strike is attenuated by subsequent logic gates, because of the electrical property of the logic gate [4]. We assume soft error occurs, when the transient voltage pulse at the output of inverter 8 has a value of Vdd/2.

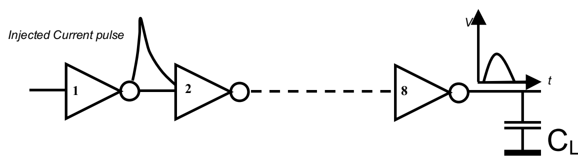

Fig. 3. 8 stage FO4 logic chain

4.3 Analysis Results

The soft error analysis for SRAM and combinational logic is performed for 32 nm and 45 nm technology using Predictive Technology Model [8].

Fig. 4 shows the critical charge reduces with the adoption of the FinFET devices to build the same designs, from the SRAM cells to logic chains. Comparing the critical charge of the FinFET based designs to that of the designs in bulk CMOS, we can see the average increases of 291% and 150% in the critical charge for 32nm and 45nm technology respectively.

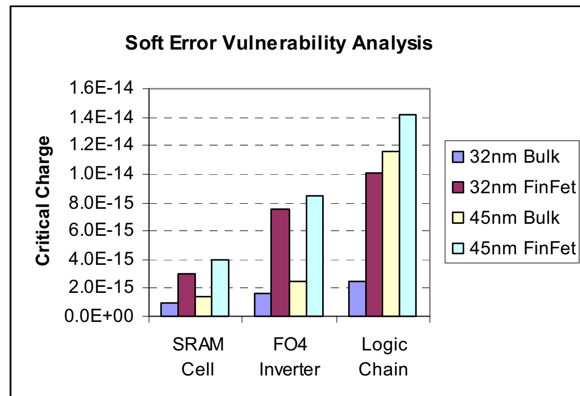

Fig. 4. Critical Charge of Different Designs in FinFET and Bulk CMOS in 32nm and 45nm technology

Fig. 5 shows the critical charge reduction when the design scales from 45nm to 32nm. Although the scaling of both FinFET and bulk CMOS causes a higher soft error susceptibility, the critical charge reduction of the FinFET device is much less than the bulk CMOS devices, when technology scales.

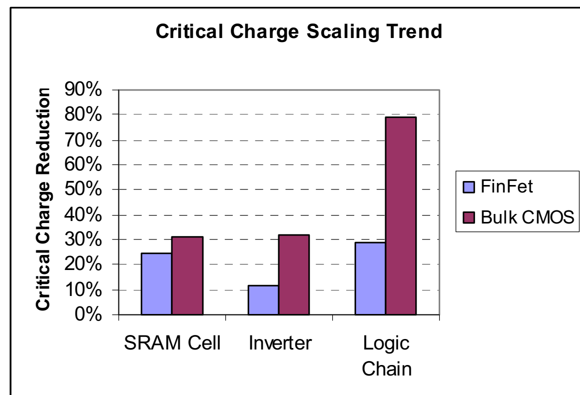

Fig. 5. Soft Error Vulnerability Scaling Trend for the FinFET Devices and Bulk CMOS devices.

Fig. 6 shows the effects the electrical masking effect of FinFET based and Bulk CMOS based inverter chains. In Fig. 6, the same height voltage pulse is

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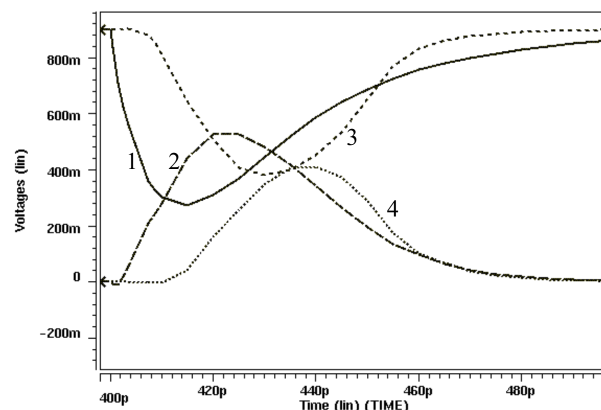
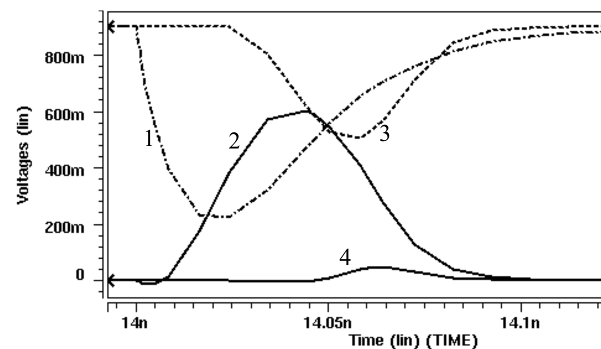
generated at the output of stage 1 of logic chain, the FinFET based logic chain has less attenuation effects than that of the bulk CMOS, which increases the soft error susceptibility of FinFET logic chain in terms of the electrical masking effects. However, Figure 4 shows that it needs much higher collected charge (>4x) for a FinFET inverter to generate an identical transient voltage pulse, comparing with a bulk CMOS inverter. Therefore, even though the electrical masking attenuation in logic chain is getting worse when switch from bulk CMOS to FinFET, the FinFET circuits still have better soft error immunity than the bulk CMOS counterparts.



(a) Electrical masking effect in FinFET logic chain



(b) Electrical masking effect in Bulk-Si logic chain

Fig. 6. Transient attenuation for an inverter chain based on (a) FinFET devices and (b) Bulk CMOS devices. The snap shot of output of stage 1, 2, 3 and 4 with the same height of the transient voltage pulse generated at the output of the stage 1

5. The Impact of Process Variation on FinFET Circuit

In this section, we study the impact of process variation on FinFET circuits and compare against that of bulk CMOS circuit. Section 5.1 gives a brief introduction on process variation, and Section 5.2 shows the impacts of process variation on SRAM and combination logic circuits.

5.1 The Impact of Process Variation

The challenges in fabricating small feature size transistors have resulted in significant variability in the transistor parameters such as channel length, gate oxide thickness and threshold voltage across identically designed neighboring transistors (intra-die variation) and across different identically designed chips (inter-die variation). The sources of variability results from different phenomena such as wafer misalignment, random dopant fluctuations, and imperfections in planarization steps. The divergence between designed and fabricated transistor parameters creates significant functional correctness concerns such as stability problems in memory cells, creation of new critical paths in the design and increased leakage currents. It has been shown that process variation can cause about 20x variation in chip leakage and 30% variation in chip frequency [13]. Process variations are of particular concern in memories since memories are typically designed using minimum feature sizes for density reasons, effects of process variation are most significant. Effects of variation on memory circuits can result in different reliability concerns of read stability, write failures, hold failures or access time increase.

Because the effect of other parameter can be translated into the effective variation in threshold voltage [14], threshold voltage fluctuation is considered as the major source of process variation when the performance impacts of the parameter fluctuations are investigated.

Traditional SRAM cell design using six transistors, as shown in Fig. 1, is used in this study. The access time distribution of the memory cell is used to evaluate the impacts of the process variation. The SRAM cell access time is defined as the time required for sufficient signal margin developed between bitline pair to trig the sense amplifier. A larger spread of the access time results in the large probability of the failure of the SRAM cells.

The distribution of the delay of the combination logic gate is used to analyze the impact of parameter fluctuation on logic circuits. Similar to the section 4, FO4 inverter gate is used to evaluate the delay of the combinational logic gate. The larger the spread in the delay distribution of the logic gates, the more vulnerable the circuits to the process variations.

5.2 Simulation Results

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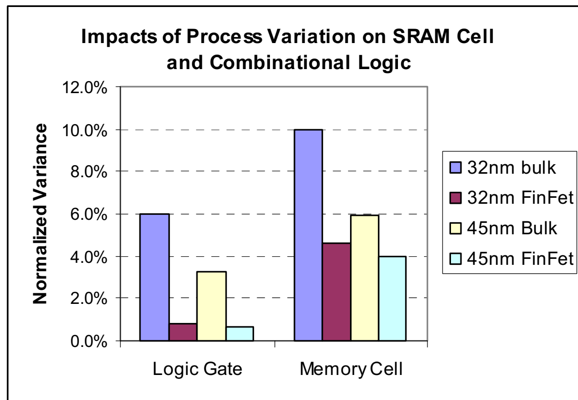
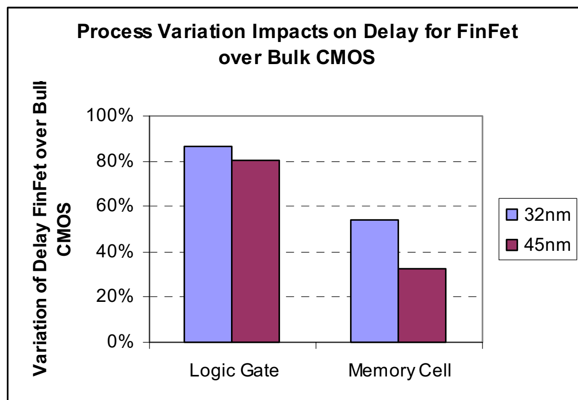
Using HSPICE and Monte Carlo analysis, we consider both the intra- and inter-die variations, assuming both inter-die and intra-die 3σ Vt deviation of 15%. We obtained the normalized variance (normalize to the mean value) of the SRAM cell access time and logic gate delay distributions with 1000 Monte Carlo simulation runs. Note that the effect of other parameter variations can be translated into the effective variation in threshold voltage [14], and we assume that the bulk CMOS and FinFET device have the same range of parameter variation.



a) Normalized variance for logic gate delay distributions and for SRAM cell access time distributions



b) Variation reduction obtained by using the FinFET devices for SRAM cell and logic gates in both 32nm and 45nm technology

Fig. 7. The Impact of Process Variation on SRAM and Logic Gate

The delay variation performance of the FinFET Based design were compared to the designs in the bulk CMOS. Compared to the FinFET based design, the larger spread in the distribution of the bulk CMOS based design can be observed in Fig 7(a). Therefore, the designs in Bulk COMS is more vulnerable to the process variation than the FinFET based design. From Fig. 7(b), we can see FinFET based designs provide the average of 83% and 43% reduction of the delay variation for logic gates and the memory cells over the designs in the Bulk CMOS.

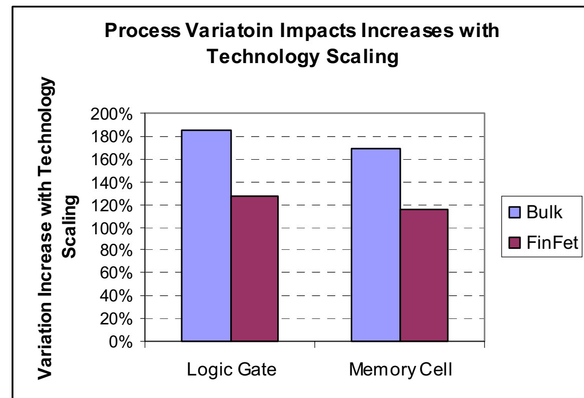
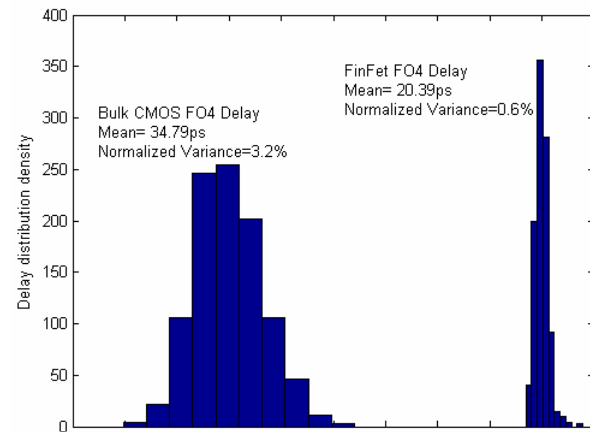
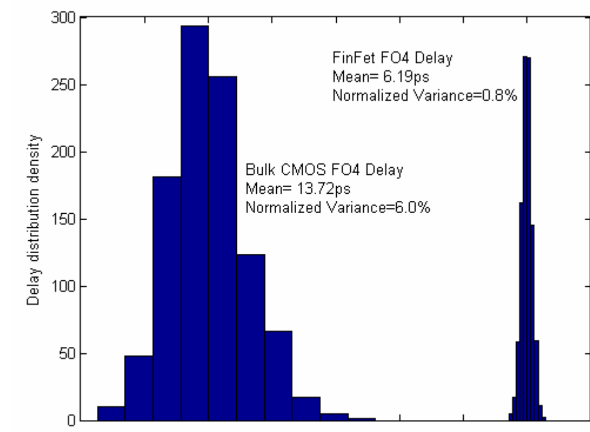


Fig. 8. Process Variation Increase with Technology Scaling from 45nm to 32nm.



a) 45nm technology node



a) 32nm technology node

Fig. 9. Impact of process variations on the FO4 delay with 3σ Vt deviation of 15%

Similar to Section 4, we show how process variation effects will scale for both FinFET and Bulk CMOS. Fig. 8 shows that when technology scales from 45nm to 32 nm, both FinFET and bulk CMOS have a higher

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level of delay variation. However, the bulk CMOS is more vulnerable to the scaling. With the device scaling, we expect the FinFET based design become more robust than the designs in bulk CMOS.

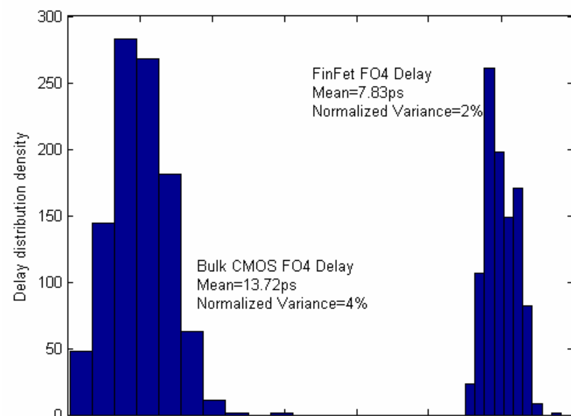

Fig. 10. Impact of process variations on the FO4 delay at 32nm technology with 3σ gate length (LG) deviation of 10%

Fig. 9 shows the impact of process variations on the FO4 delay with 3σ Vt deviation of 15%. It can be seen that the FinFET FO4 delay is much faster than the bulk CMOS, and FinFET circuits are less vulnerable to process variation. Fig. 10 shows a similar result for the simulation with a 3σ deviation of 15% for gate length.

6. Conclusion

Double-gate FinFET technology has been proposed as a promising alternative for bulk CMOS technology to continue the technology scaling. The performance or power advantages of FinFET circuits over bulk CMOS circuits have been studied by previous research. This paper provides the dependability analysis for FinFET circuits. The experiments compare the bulk CMOS circuits and FinFET circuits in 45nm and 32nm technologies, showing that FinFET circuits have better soft error immunity, and are less vulnerable to process variation. It is concluded that the FinFET-based circuit designs are much robust than the bulk CMOS counterparts.

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