

# Variation Impact on SER of Combinational Circuits

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## Abstract

*Increasing variability not only affects the behavior of contemporary ICs but also their vulnerability to transient error phenomenon especially radiation induced soft errors. Such variations in device parameters are caused by static process variations, dynamic variations in power supply and temperature and slow degradation of individual devices due to phenomena like Hot Carrier Injection (HCI) and Negative Bias Temperature Instability (NBTI). In this paper\*, we analyze the impact of such variations on the Soft Error Rates (SER) of combinational logic circuits. Other contributions of this work also include tools that model threshold degradation of NMOS due to HCI and PMOS due to NBTI in logic circuits. Results were obtained for custom designed circuits and ISCAS-85 benchmarks. A detailed analysis of effect of threshold variations on SER is also presented with interesting observations.*

## 1. Introduction

Sub-90nm circuits currently face an unmanageable problem of unpredictability in process parameters of their individual devices [1]. Such uncertainties not only affect the circuit power and performance [2], but also their resilience to transient faults like soft errors. Since the soft error resilience of any device has a strong dependence on the process parameters like device length, threshold voltage etc, the effect of process variability on SER of the circuits cannot be neglected. One of the main causes of such variations in process parameters is manufacturing parameter fluctuations due to increasingly challenging fabrication requirements [3]. Such effects are of static nature which may be characterized and detected immediately after manufacturing to some extent. Yet another reason for changes in device behavior is the dynamic and aging related variations due to runtime phenomenon like the power supply noise, temperature imbalance and device degradation. Each of these phenomenon impact the device characteristics and thereby the resilience of the devices to soft errors.

Manufacturing parameter fluctuations are one of the biggest problems faced by current circuit designers. The aggravation of such defects is attributed to technology scaling which poses very difficult fabrication challenges. The expected device parameters vary across different dies and within a die itself, namely inter-die and intra-die variations respectively [2]. Such

variations may significantly affect power and delay characteristics of the circuit and thereby impose challenges in meeting the necessary budgets. Apart from being a reliability concern by themselves, such variations introduce newer reliability concerns in the form of modulating the susceptibility and resilience of the circuits to transient errors like radiation induced soft errors. Due to reduced feature sizes, any slight change in the process parameters contributes to a significant percentage of variations and thereby their impact is quite significant. Consequently, dynamically natured variations due to power supply variations and increased temperature across chips have also been one of the important causes for variations [10, 14]. Also, variations due to device degradation because of Hot Carrier Effects (HCE) and Negative Bias Temperature Instability (NBTI), which are attributed to the circuit usage over a period of time, may lead to run time degradation and uncertainties in the circuits [4, 13]. Such changes although may contribute to more of permanent failures, the degradation may once again affect the transient error vulnerability of the circuit since they change the operating conditions and the device parameters of the circuits, both of which affect the SER of a circuit significantly.

Soft errors in combinational circuits are becoming as important as those in unprotected memory circuits as technology scales due to reduced voltage and nodal capacitance, increased speed and decreased pipeline depths [5]. Modeling SER in combinational circuits has been a challenge due to the presence of the inherent masking mechanisms. Various methodologies have been proposed to model these logical, electrical and latch window masking effects in combinational circuits [5, 6]. In this work, we used HSPICE to obtain accurate SER estimates due to variations in our custom benchmark circuits for accuracy and flexibility that HSPICE provides. We also performed SER analyses on larger ISCAS benchmarks using the Soft Error Analysis Toolset - Logic Analyzer (SEAT-LA) [6]. SEAT-LA uses an approach that is applied to designs that use cell libraries characterized for soft error analysis and utilizes analytical equations to model the propagation of a voltage pulse to the input of a flip-flop.

Although there have been many methodologies that propose to modeling and optimizations for soft errors [5, 6], it is important to address soft errors in the presence of other reliability issues as well. To the best of the author's knowledge, this is first work that has looked at effect of other reliability issues on SER. Thus, the primary contributions of this paper include: (a) Analysis of SER in combinational logic circuits under variations. (b) Tools (built using existing methodologies)

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to estimate the state of individual devices and their process parameters due to HCE and NBTI induced degradation (Section 2.3) over a period of time.

The paper is organized as follows: Section 2 presents the variation models used by us. The details of SER estimation tools are discussed in section 3. Experimental results are presented in section 4. Finally, Section 5 concludes the paper.

## 2. Modeling Variations

In this paper, we have considered three different categories of variations, namely, static, dynamic and aging related variations. The methodologies used to model these types of variations are discussed in detail in this section.

### 2.1 Static Variations

Static variations are primarily due to manufacturing uncertainties, like variations in channel length, channel width, thickness of gate oxide and threshold voltage. Inter-die variations change the value of the parameters in all the transistors in a die in the same direction. These variations are caused by processing temperatures, equipment quality, wafer polishing and placement. Examples are channel length, channel width and variations between individual metal layers used for routing [3]. These variations mainly result in differences in power and delay. On the contrary, intra-die variations can be either systematic or random. These variations arise due to misalignment of wafer, Random Dopant Fluctuations (RDF) and uneven planarization steps. Transistor parameter shifts resulting from systematic variations are correlated and are dependent on the neighboring transistor parameters. Random variations shift the transistor parameters independent of the locality. Particularly, RDF leads to non-uniform distribution in transistor threshold voltages ( $V_{th}$ ) in the circuit and is a key example to random variations. These static variations can be translated into change in the effective threshold voltage ( $V_{th}$ ) [7]. Hence the effect of change of  $V_{th}$  due to process variations on the SER is studied in this work.

### 2.2 Dynamic Variations in Power Supply and Temperature

The dynamic variations considered by us in this work are the variations due to temperature changes in circuits and power supply variations. In this section we briefly discuss the impact of such variations on circuits.

**2.2.1 Power supply variations.** The variations in power supply have been one of the most important challenges as technology scales. This is because of the decreased supply voltage which results in a much larger ratio of the peak noise voltage to the ideal supply voltage [10]. This power supply noise is primarily a voltage drop in power distribution networks resulting in different voltages at different parts of the same chip. These variations are mainly due to resistive and inductive voltage drops across power supply networks. A power supply noise analysis methodology for circuits and microprocessors has been discussed in [11]. A minimum power supply fluctuation

of 10% is acceptable [10]. Thus, in our work we have varied the power supply for the benchmarks by 10% and presented the corresponding variation of SER in section 4.

**2.2.2 Variations in temperature.** Heat generation in chips has increased rapidly with recent scaling trends and increased transistor density. This has led to non-uniform substrate temperature profile, affecting both interconnect and transistor delays. In the case of interconnects, the rise in temperature increases the resistivity of metals thus resulting in increased delays. In devices, temperature affects both the mobility and the threshold voltage. Rise in substrate temperature reduces the mobility of electrons/holes in MOSFETs because of increased scattering at higher temperature [14]. The threshold voltage also decreases with increase in temperature because of the change in fermi-potential ( $\phi_f$ ) [14]. These two effects determine the trends in delay in logic circuits and thus, it affects the electrical masking capability of the logic circuits. The change in transistor delays also affects flip-flop characteristics like the set-up and hold times. This in turn results in a change in latch window masking capability of logic circuits. Thus, it is important to analyze these effects in detail and so far no work has contributed to such an analysis.

### 2.3 Variations Due to Aging

The aging related variations considered by us in this work are the variations due to device degradation over a period of time because of HCE, NBTI and power supply variations. To analyze the SER due to such variations, we first built tools using existing models, which are described in this section.

**2.3.1 NMOS degradation due to HCE.** The variations in threshold voltages of different devices over a period of time are considered for dynamic variations in the process parameters. Such change in process parameters are primarily due to factors like temperature and activity of the device, which impact the basic I-V characteristics of the devices.

One such phenomenon which leads to the degradation of the device due to the aforementioned factors is Hot Carrier Effect (HCE). Hot carrier effect is the phenomenon of trapping of high energy charge carriers at the gate oxide or creating new traps due to impact ionization effect. This trapping of charges increases the transistor threshold and thereby affecting the power and performance of the device. Such variations are more predominant in the NMOS transistors compared to PMOS transistors primarily due to negligible degradation rate of the saturation current of PMOS when compared to NMOS [8]. In this work we developed a tool using analytical models presented in [9] for individual devices to observe the aging impact on devices. Equation 1, 2 and 3 are the prime equations governing the degree of degradation of a device.

$$\frac{dN_{it}}{dt} [1 + AN_{it}] = KI_{bb} \quad (1)$$

$$I_{bb} = \frac{C_1}{W} I_{DS} \exp\left(-\frac{B_{it}}{E_m}\right) \quad (2)$$

$$E_m = \frac{V_{ds} - V_{dsat}}{l_d} \quad (3)$$

Where,  $N_{it}$  is the number of trapped charges per  $\text{cm}^2$ , constants,  $A = 5 \times 10^{-9} \text{ cm}^2$ ,  $K=5 \times 10^{15}$ ,  $C=2$ ,  $B_i = 4.41 \times 10^6 \text{ V/cm}$  is the ionization coefficient,  $E_m$  is related to peak electric field along the channel and is given by equation (3).  $I_{DS}$  is the drain source current which flows through the device during a transition as demonstrated in Figure 1. We use these equations along with the analytical model presented in [9] to estimate the  $V_{th}$  of a single NMOS device under constant current conditions. The degradation of  $V_{th}$  under such constant stressing conditions is demonstrated in Figure 2 for a 70nm NMOS transistor.

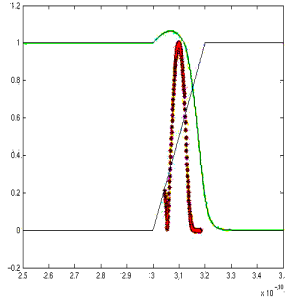


Figure 1 Device current during a transition

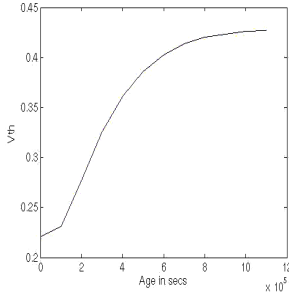


Figure 2 Variation of  $V_{th}$  of NMOS with aging

Note that this degradation is under the assumption of constant stressing of the NMOS device, which is essentially continuous current flowing through it for the given period of time. In circuits, however, current flow through the device is only during switching and over a short period of time. Hence the actual age of the circuits can be related to the stressed age using the equation (4).

$$\Delta S = \frac{T * P}{CLK} \left[ \frac{\int_{t1}^{t2} I_{sub} dt}{I_{sub\_dc}} \right] \quad (4)$$

Where,  $\Delta S$  is the stressed age,  $T$  is the actual age,  $P$  is the switching probability of the gate of the NMOS transistor under consideration,  $I_{sub}$  is the substrate current,  $CLK$  is the clock frequency and  $I_{sub\_dc}$  is the total constant current under stressed conditions that may flow during time  $T$ . The equation primarily exploits the number of transitions of the gate over a period of time and the current flowing through the device based upon the exact current estimates obtained from HSPICE. MATLAB model is integrated with the circuit simulation tool HSPICE for precise estimation of the individual device threshold changes over a period of time. We obtain the actual ages of each of the NMOS transistors in a circuit during its operation based on the actual current flowing through the devices during any transition. These numbers are used to obtain the actual ages of the devices and thereby the new threshold of the devices at the

end of a time window of observation, which is one day in our case. The thresholds are then used to obtain the new current estimates and the ages at the end of next day. Figure 3 demonstrates the flow of the tool developed by us which iteratively estimates the degradation of the devices given a SPICE model of any circuit. Note that unlike the random behavior of static process variations these dynamic variations considered by us are more deterministic due to their strong dependence on the activity of the transistors.

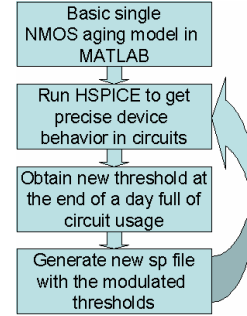


Figure 3 Tool flow for estimating degradation

**2.3.2 PMOS degradation due to NBTI.** Another phenomenon that leads to slow degradation of especially PMOS devices is NBTI. NBTI in PMOS occurs under negative gate voltage ( $V_{gs} = -V_{DD}$ ) and results in increased threshold voltage with time. The main reason for the NBTI effect is found to be the presence of increased number of positive interface traps caused by the displacement of Si-H bonds, which are induced by positive holes from the channel. NMOS transistor has a negligible level of holes in their channel and hence does not suffer from NBTI degradation [13].

There are number of works recently which have attempted to model NBTI. In this work, we follow the approach used in [13] to model the change in the threshold voltage due to NBTI. As explained here, when the PMOS is on, it is in a stressed stage and when it is off, it is in a recovery stage where the threshold voltage attempts to drop back due to the diffusion of the H atoms back to the interface to form the S-H bonds. These two stages are modeled by the following equations [13]:

During Stress,

$$\Delta V_{th} = \sqrt{K_v^2 (t - t_0)^2 + \Delta V_{th0}^2} + \delta_v \quad (5)$$

During Recovery,

$$\Delta V_{th} = (\Delta V_{th0} - \delta_v) \left[ 1 - \sqrt{\eta(t - t_0)/t} \right] \quad (6)$$

where,

$$K_v \propto \sqrt{C_{ox} (V_{gs} - V_{th})} \cdot \exp(E_{ox}/E_0) \cdot \exp(-E_a/kT)$$

Here,  $E_{ox} = (V_{gs} - V_{th})/T_{ox}$ ,  $C_{ox}$  is the oxide capacitance,  $k$  is the Boltzman constant,  $\delta_v = 5\text{mV}$ ,  $\eta$  is 0.35,  $t$  and  $t_0$  are the initial and final times,  $E_0 = 2\text{MV/cm}$  and  $E_a = 0.13\text{eV}$ . From (5) and (6), an expression for long term degradation can be derived after  $n$  cycles of recovery for a duty cycle or a stress period of  $\beta$  and a clock period of  $D$ . Thus, as in [16]:

$$\Delta V_{th} = K_v \cdot \beta^{0.25} \cdot T^{0.25} \left[ \frac{1 - (1 - \sqrt{\eta(1 - \beta)/n})^{2n}}{1 - (1 - \sqrt{\eta(1 - \beta)/n})^2} \right]^{0.5} + \delta_v \quad (7)$$

Using above equations, the change in threshold voltages are estimated taking into consideration the stress and recovery time based on the static probability of the gate voltage for each node

in a circuit. With this information, the SER for any given circuit can be estimated with degraded PMOS in these circuits.

### 3. SER Estimation Tools

In this section a brief background on the experimental set-up and methodology used for our SER analysis is presented. In our experiments we analyze soft error rates in small custom benchmark circuits that represent combinational logic in general. We use a HSPICE circuit level tool to estimate SER accurately in these custom benchmark circuits. We also estimate the SER variations for bigger ISCAS-85 benchmarks with respect to static threshold changes in circuits. This section describes the two experimental setups that are used for SER estimation in the benchmark circuits.

The HSPICE estimation tool uses an accurate method for SER estimation. This tool requires a SPICE netlist of the circuit for which the SER needs to be estimated. This tool provides an SER for a given current pulse generated by a pulse strike. A double exponential current pulse similar to the ones used in [6, 12]. The HSPICE tool then calculates the Timing Window ( $tw$ ) for which this current pulse at each node in the logic circuit causes an error at the output of the flip-flop. As defined in [6], timing window is the amount of time for which the current pulse at a node cause an error at the flip-flop output divided by the clock period. Thus,  $tw$  is the probability that an error occurs given a current pulse at a node N. If the probability of the current pulse occurring at this node N is known, then as in [6], the SER for that circuit (with N nodes and a single output O) can be calculated using the following equation:

$$SER_o = \sum_N P_N \times tw \quad (8)$$

Apart from being accurate, the HSPICE also allows the user to change parameters of individual devices that occur due to variations. But the HSPICE tool works effectively for only very small circuits with 5-10 gates. When circuits get bigger, analysis using HSPICE becomes very tedious and time consuming. Hence to analyze SER variations in bigger ISCAS benchmarks, we use SEAT-LA. SEAT-LA requires a gate level design of the circuit to estimate the SER. In [6], a detailed explanation on how SEAT-LA can be used to predict SER in logic circuits is presented.

### 4. Experimental Results

We used a set of custom designed circuit layouts and gate level designs of ISCAS-85 benchmarks for our simulations. The custom designed circuits were laid out in 70nm PTM technology [15] and simulated using HSPICE. These circuits include a ten stage inverter chain, logic chain similar to the one used in [6], C17 ISCAS benchmark, a 2X4 decoder and a four bit Ripple Carry Adder (RCA). The gate level designs of the ISCAS-85 benchmarks were tested using SEAT-LA.

#### 4.1 Static Variations

In our first set of experiments on static variations, we tested out the impact of inter-die variations on both the custom designed benchmarks and ISCAS-85 benchmarks. Results of

these tests are shown in Figure 4 and show a maximum variation of 15.93% for a  $3\sigma$  (maximum) variation of 10% in threshold voltage ( $\Delta V_{th}$ ). Importantly, we observe an increase in the SER as threshold increases. This trend is the opposite of what is expected and explained in [12].

As mentioned in [12], there are two different phenomena that determine the trend of SER with change in threshold voltage. The first being the increase in gain of static logic circuits with increase in threshold voltage. This in turn reduces the electrical masking capability of static logic circuits resulting in increase in SER. Also, the flip-flop set-up and hold time increases with increased threshold voltage. This increases the (latch-window) masking capability of the flip-flops as larger pulses are now needed to get latched on by the flip-flop. Thus, the SER trend depends on which of the above factor dominates more. In [12] it was found that the SER decreased with large increase in  $V_{th}$ . This was due to the large increase in the flip-flop set-up and hold times while the increase in gain of the logic circuits had a lot lesser effect on the overall SER trend.

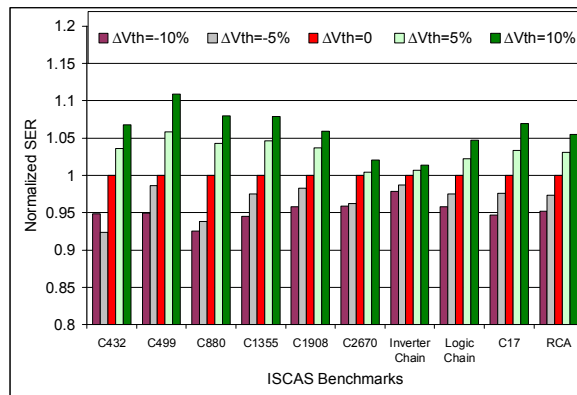


Figure 4 Normalized SER due to static variation for ISCAS and custom benchmarks

Since our initial analysis on SER variation due to variations in  $V_{th}$  had an opposite trend to what is expected as in [12], we extended our experiments to estimate the change in SER by increasing  $V_{th}$  beyond 10% for two of the smaller benchmarks. These results are presented in Figure 5. From the figure it is noted that there is an initial linear increase in SER with small increase in  $V_{th}$ . This is clearly due to the dominant influence of CMOS gate gains in the logic circuits. But as  $V_{th}$  increases further, the reduction in setup and hold times of the flip-flops at the end of the data-paths starts playing a more important role, thus reducing SER drastically after a point as seen in Figure 5.

These curves indicate interesting trade-offs that can be used for design optimizations in circuits for both power and SER mitigation. Hence, this can be used to estimate the  $V_{th}$  for which the circuits can be used to save leakage power and also decrease SER. Also, this technique can be applied for noise mitigation in general rather than just mitigating radiation induced soft errors.

To model the effect of intra-die random variations, we performed SER analysis on two of the custom benchmarks with random  $V_{th}$  assignments for the different devices. A Gaussian distribution in threshold voltage with  $\mu = 0.2$  and  $\sigma = 0.02$  for NMOS and  $\mu = 0.22$  and  $\sigma = 0.02$  for PMOS was used to assign  $V_{th}$  to each of the devices. Once the  $V_{th}$  was assigned for each device in the circuit, the circuit was simulated

analysis. Due to long simulation times, SER analyses for 10 different assignments were performed. Figure 6 shows the variation of SER normalized to SER for nominal threshold values. The peak-peak variation of 41% was found for these simulations. As seen in the Figure, large variation in SER was seen even for a small sample of  $V_{th}$ . Thus, a faster way to model SER variations with random variations is required to do a deeper analysis.

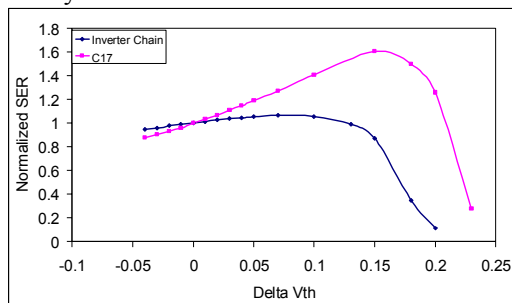


Figure 5 SER variation with increase in  $V_{th}$

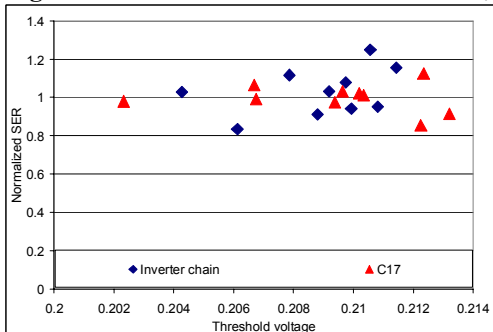


Figure 6 Impact of random  $V_{th}$  variations

## 4.2 Dynamic Variations in Power Supply and Temperature

Our next set of simulations studied the effects of power supply variations on the SER on different benchmark circuits. Figure 7 presents these and shows that for a 10% fluctuation of variation in power supply the SER varied by a maximum of 24.85% among all the circuits considered. Here as expected, the SER increased with decrease in voltage. Also, it is interesting to note that the variation in SER is almost linear with respect to change in voltage.

Next we also studied the effect of increased temperature on SER on the custom benchmark circuits. Figure 8 shows the variations in SER with increase in temperature. As seen here, there are vast differences in trends in different design. To determine the reasons for the different trends, it is important to study the effect of temperature on flip-flop characteristics. For this, the  $t_w$  for trapezoidal pulses with increasing widths were studied. Here it was noted that the timing window was much lower at higher temperatures for small pulse widths while it was similar or in fact slightly greater (than that for lower temperatures) for large pulse widths. Thus, for designs with longer data-paths, the pulse widths that reach the flip-flop are very small resulting in very small SER at higher temperatures as seen for inverter chain and decoder in Figure 8. On the other hand, for designs with very short data paths like c17, the pulse

width (due to the same strike) reaching the flip-flop is larger thus having an opposite trend in SER as seen in Figure 8.

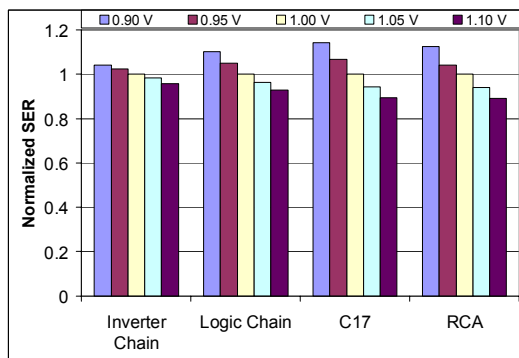


Figure 7 Variation of SER with power supply variations

## 4.3 Variations Due to Aging

Next, we performed experiments on the custom benchmark circuits to find the effect of device degradation due to HCE by using the tool discussed in section 2.3.1. Thus we studied the effect of HCE on the threshold voltages of different NMOS transistors in each of the circuits. These threshold variations were obtained by assuming a 50% switching activity at all the inputs of each of the circuit considered. The variation of average  $V_{th}$  after every 200 days in these circuits is presented in Figure 9. From Figure 9, it is clear that the  $V_{th}$  variation depends on the type of circuit. For example in circuits like inverter chain and C17, where the input transitions results in large number of transitions of devices in the circuit, there is a large increase in  $V_{th}$  with age. For circuits like logic chain and RCA, there is not a large increase in the  $V_{th}$ .

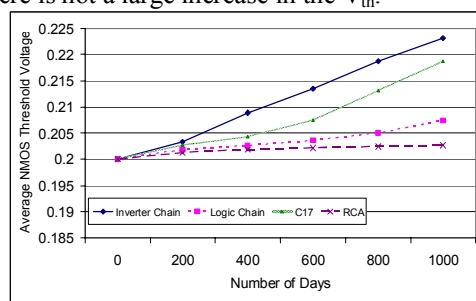


Figure 9  $V_{th}$  variations due to HCE

We also studied the degradation of PMOS devices due to NBTI modeled as presented in section 2.3.2. For this, the static probability of each of the nodes was obtained based on a 0.5 input transition probability for all the circuits using which the change in  $V_{th}$  in each PMOS device in the circuits was obtained. Figure 10 presents the average variation of  $V_{th}$  of the PMOS devices in different circuits. As seen from the figure, there is only a small increase in threshold, which is in fact smaller than those observed for HCE.

Next, SER for different bench mark circuits was obtained by incorporating the changes in  $V_{th}$  due to the two aging effects. Figure 11 presents the results obtained for aging effects on SER. As expected, the SER variations are not as much because of very small variations in the threshold voltages due to aging. Also, there is not a very clear trend in these variations mainly because the change in  $V_{th}$  is different for an NMOS and PMOS

due to the two effects which make it difficult to predict the masking effects of different designs.

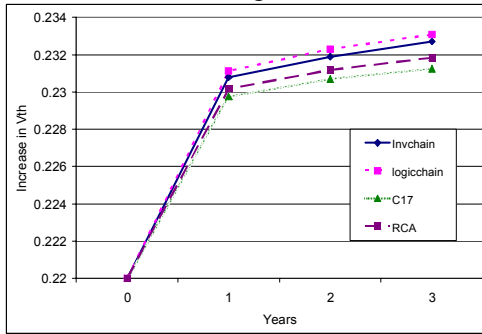


Figure 10 V<sub>th</sub> variations due to NBTI

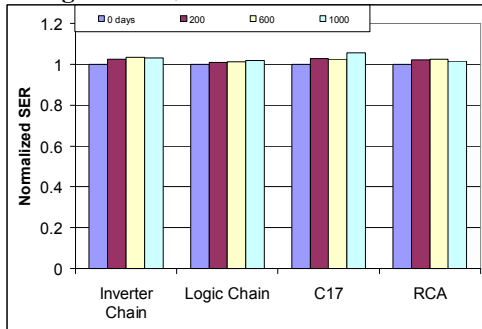


Figure 11 SER variations due to NBTI and HCE

Finally, simulations were performed on one of the benchmark circuits (inverter chain) after incorporating different variations simultaneously to find the overall impact on SER. Table 1 shows the overall impact of these variations in SER. Here, the first column (% $\Delta V_{th}$ ) is the percentage change in  $V_{th}$  due to inter-die variations, the second column (days) represents the age of the circuit in number of days, the third column (Temp) represents the temperature at which the circuit works in Celsius and the fourth column presents the normalized SER values for each case. From these results, it can be noted that temperature has the maximum impact on SER as the results are comparable to its effects on inverter chain as shown in Figure 8. As expected, aging has very little impact when compared to the other variations on SER.

## 5. Conclusion

In this work we analyze the impact of variations on SER of combinational logic circuits. The variations that were studied include static variations like inter and intra-die process variations, dynamic variations due to power supply and temperature and aging induced variation due to HCE and NBTI. First we presented ways in which we have modeled these variations based on previous works. Next we presented our tools to measure SER in various circuits. Finally we presented our results on different variations. It was found that  $V_{th}$  variation due to inter-die variations resulted in SER variation of 15.93% for a  $3\sigma$  variation of 10%. Threshold variations due to intra-die variations resulted in a peak-peak SER variation of 41% in small circuits based on small set of simulations. This necessitates a faster model to be implemented for analyzing then effect of intra-die variations on SER. It was also found that the effect of device degradation was not

significant. Power supply variations showed a maximum variation in SER of 24.85% across different circuits while the effect of temperature on SER variations was the highest especially for logic circuits with short data-paths.

Table 1 Overall variation impact on SER of inverter chain

| % $\Delta V_{th}$ | Days | Temp ( $^{\circ}$ C) | SER      |
|-------------------|------|----------------------|----------|
| 0                 | 0    | 25                   | 1        |
| 5                 | 999  | 100                  | 0.422096 |
| 10                | 600  | 100                  | 0.40085  |
| 10                | 999  | 70                   | 0.842776 |
| 10                | 999  | 100                  | 0.403683 |
| -5                | 999  | 100                  | 0.450425 |
| -10               | 600  | 100                  | 0.494334 |
| -10               | 999  | 70                   | 0.878187 |
| -10               | 999  | 100                  | 0.471671 |

## 6. References

- [1] ITRS-2003, Critical reliability challenges for the International Technology Roadmap for Semiconductors, International Sematech Technology transfer 03024377A-TR, 2003.
- [2] S. Borkar, T. Karnik, S. Narendra, J. Tschanz, A. Keshavarzi, V. De, Parameter variations and impact on circuits and micro-architecture, Proceedings of Design Automation Conference, June 2003 Page(s):338 - 342.
- [3] K. A. Bowman, S. G. Duvall, J. D. Meindl, Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration, IEEE Journal of Solid-State Circuits, Volume 37, Issue 2, Feb. 2002 Page(s):183 - 190.
- [4] X. Xuan, A. Chatterjee, and A. D. Singh, Local redesign for reliability of CMOS digital circuits under device degradation, Proceedings of International Reliability Physics Symposium (IRPS), 2004.
- [5] P. Shivakumar, M. Kistler, S. Keckler, D. Burger, and L. Alvisi, Modeling the effect of technology trends on the soft error rate of combinational logic, Proceedings of International Conference on Dependable Systems and Networks, June 2002 Page(s): 389 - 398.
- [6] R. Rajaraman, J. S. Kim, N. Vijaykrishnan, Y. Xie, M. J. Irwin, SEAT-LA: A soft error analysis tool for combinational logic, Proceedings of the International Conference on VLSI Design, Jan. 2006.
- [7] A. Agarwal, B. C. Paul, S. Mukhopadhyay and K. Roy, Process variation in embedded memories: failure analysis and variation aware architecture, IEEE Journal of Solid-state Circuits, Vol.40, pp. 1804-1814, September 2005.
- [8] P. Fang, J. Tao, J. F. Chen, C. Hu, Design in hot-carrier reliability for high-performance applications, Proceedings of IEEE Custom Integrated Circuits Conference, 1998.
- [9] Y. S. Jean and C. Y. Wu, The threshold-voltage model of MOSFET devices with localized interface charge, IEEE Transactions on Electron Devices, 1997.
- [10] A. H. Ajami, K. Banerjee and M. Pedram, Scaling analysis of on-chip power grid voltage variations in nanometer scale ULSI, International Journal of Analog Integrated Circuits and Signal Processing, Vol. 42, No. 3, pp. 277-290, Springer, 2005.
- [11] H. H. Chen and D.D. Ling, Power supply noise analysis methodology for deep-submicron VLSI chip design, Proceedings of Design Automation Conference, 1997.
- [12] V. Degalahal, R. Ramanarayanan, N. Vijaykrishnan, Y. Xie and M. J. Irwin, The effect of threshold voltages on the soft error rate, Proceedings of International symposium on Quality Electronic Design, Mar. 2004.
- [13] R. Vattikonda, W. Wang, Y. Cao, Modeling and minimization of PMOS NBTI effect for robust nanometer design, Proceedings of Design Automation Conference, Jul 2006.
- [14] J. A. Power, R. Clancy, W. A. Wall, A. Mathewson, W. A. Lane, An investigation of MOSFET statistical and temperature effects, Proceedings of the 1992 International Conference on Microelectronic Test Structures, 16-19 March 1992 Page(s):202 - 207
- [15] Predictive Tech. Model - <http://www.eas.asu.edu/~ptm/>.
- [16] [http://www.eas.asu.edu/~ptm/reliability/PTM\\_NBTI\\_Beta.pdf](http://www.eas.asu.edu/~ptm/reliability/PTM_NBTI_Beta.pdf).