

# Yuan Xie

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## Education

2002	<b>Princeton University</b> Ph.D. in Electrical Engineering	Princeton, NJ
1999	<b>Princeton University</b> M.S. in Electrical Engineering	Princeton, NJ
1997	<b>Tsinghua University</b> B.S in Electronic Engineering	Beijing, P.R.China

## Professional Experience

2008 - present	<b>Pennsylvania State University</b> Associate Professor in the Department of Computer Science Engineering	University Park, PA
2010	<b>National Tsing Hua University</b> Guest Professor in the Department of Computer Science	HsinChu, Taiwan
05-06/2010	<b>IMEC (Interuniversity Microelectronics Centre)</b> Visiting Researcher	Leuven, Belgium
2003 - 2008	<b>Pennsylvania State University</b> Assistant Professor in the Department of Computer Science Engineering	University Park, PA
2002 - 2003	<b>IBM Microelectronic Division</b> Advisory Engineer in Worldwide Design Center	Essex Junction, Vermont
1997 -2002	<b>Princeton University</b> Research Assistant in Electrical Engineering Department	Princeton, NJ
1998, 1999	<b>Mentor Graphics Inc.</b> Research Summer Intern in the Behavioral Synthesis group	Willsonville, OR

## Research Summary

Yuan Xie has published more than 100 refereed articles in journals and conferences in the areas of design automation and novel architecture for Three-dimensional IC Design (3D ICs), emerging memory technologies, low power and thermal-aware design, system-level synthesis and high-level synthesis for embedded systems. He has graduated 6 Ph.D. students and is currently supervising 11 Ph.D. graduates. He has served as an investigator on 10 research grants administered by US Federal agencies (including National Science Foundation and DARPA, Semiconductor Research Corporation) and 8 research grants from industry. These projects have resulted in the design of new CAD tools and optimizations, and novel architectures for emerging technologies such as 3D ICs and emerging memory technologies. He has received Best Paper Awards (ASP-DAC 2008, ASICON 2001) with several Best Paper Nominations (ICCAD 2006, ASP-DAC 2009 and ASP-DAC 2010). Through extensive collaboration with Industry partners (IBM, Qualcomm, Honda, Intel, Seagate), he has helped transition research ideas to industry.

## Service Summary

Yuan Xie has been active volunteer in the design automation, VLSI and computer architecture conferences. He served as program committee member, track chair and conference chair for leading conferences in these areas, including top EDA conferences such as DAC, ICCAD, ASP-DAC, and DATE (He will serve as the TPC Vice-chair for ASP-DAC 2012 and TPC chair for ASP-DAC 2013). Currently he serves as a committee member in IEEE Design Automation Technical Committee

(DATC), and serves as the Associate Editor for IEEE Transactions on CAD, IEEE Transactions on VLSI, ACM Journal of Emerging Technologies in Computing Systems, IEEE Design and Test of Computers, and IET Computers and Design Techniques. He has given 10+ tutorials in prestigious conferences and 30+ invited talks in industry/academia to promote the awareness of 3D IC technology.

## Awards and Honors

2010	Overseas and Hong Kong, Macau Young Scholars Collaborative Research Award by China NSF
2010	Association for Computing Machinery(ACM) Distinguished Speaker
2010	ASP-DAC 2010 Best Paper Award Nomination (Paper [C22])
2009	Selected as one of the 7 overseas scholars in "Dragon Star" Program supported by China NSF.
2009	Penn State Engineering Society Outstanding Research Award Nomination, Penn State
2009	ASP-DAC 2009 Best Paper Award Nomination (Paper [C33])
2008	IBM Faculty Award
2008	ASP-DAC 2008 Best Paper Award (Paper [C45])
2008	Department Faculty Teaching Award, Computer Science and Engineering Department
2007	Outstanding Teaching Award Nomination, College of Engineering, Penn State
2006	<b>National Science Foundation Faculty Early Career Development (CAREER) Award.</b>
2006	Chun-Hui Outstanding Overseas Scholar Award, Chinese Ministry of Education
2006	ICCAD 2006 Best Paper Award Nomination (Paper [C54]).
2002	SRC(Semiconductor Research Corporations) Inventor Recognition Award.
2001	International Conference on ASICs, Best Paper Award (Paper [C97]).

## Journal Publications

- [J1]. Yuan Xie. "Modeling, Architecture, and Applications for Emerging Non-volatile Memory Technologies." To appear in *IEEE Computer Design and Test*, January, 2011
- [J2]. Xiaoxia Wu, Wei Zhao, Chandra Nimmagadda, Durodami Lisk, Mark Nakamoto, Sam Gu, Riko Radojic, Matt Nowak, and Yuan Xie. "Electrical Characterization for Inter-tier Connections and Timing Analysis for 3D ICs." To appear in *IEEE Transactions on Very Large Scale Integrated Systems (TVLSI)*.
- [3]. Shengqi Yang, Pallav Gupta, Marilyn Wolf, Dimitrios Serpanos, Yuan Xie, N. Vijaykrishnan. "Power Analysis Attack Resistance Engineering by Dynamic Voltage and Frequency Scaling." To appear in *ACM Transactions in Embedded Computing Systems (TECS)*
- [4]. Feng Wang, Yibo Chen, Xiaoxia Wu, C. Nicopoulos, Yuan Xie, N. Vijaykrishnan. "Variation-aware Task Allocation and Scheduling for MPSoC." To appear in *IEEE Transactions on CAD (TCAD)*
- [5]. Xiangyu Dong, Jishen Zhao, Yuan Xie. "Cost Analysis and Cost-driven Design for 3D ICs." To appear in *IEEE Transactions on CAD (TCAD)*
- [J6]. Yu Wang, Hong Luo, Ku He, Rong Luo, Huanzhong Yang, Yuan Xie. "Temperature-Aware NBTI Modeling and the Impact of Standby Leakage Reduction Techniques on Circuit Performance Degradation." To appear in *IEEE Transactions on Dependable and Secure Computing (TDCS)*.
- [J7]. Xiaoxia Wu, Jian Li, Lixi Zhang, Evan Speight, Yuan Xie. "Hybrid Cache Architecture with Disparate Memory Technologies." To appear in *ACM Transactions on Architecture and Code Optimization (TACO)*.
- [J8]. Yu Wang, Xiaoming Chen, Wenping Wang, Yu Cao, Yuan Xie, Huazhong Yang. "Leakage Power and Circuit Aging Optimization by Gate Replacement Techniques." To appear in *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)* .
- [J9]. Feng Wang, Xiaoxia Wu, Yuan Xie. "SER Analysis for Combinational Logic Using an Accurate Electrical Masking Model." To appear in *IEEE Transactions on Dependable and Secure Computing (TDCS)*.
- [J10]. Hong Luo, Yu Wang, Rong Luo, Huazhong Yang, Yuan Xie. "Temperature-aware NBTI Modeling Techniques in Digital Circuits." *IEICE Transactions on Electronics.*, No. 6, pp. 875-886, 2009
- [J11]. Yuan Xie and Yibo Chen. "Statistical High Level Synthesis Considering Process Variations." *IEEE Computer Design and Test, Special Issue on HLS*, Vol. 26, Issue 4, pp.78-87, July-August, 2009
- [J12]. M. DeBole, R. Krishnan, V. Balakrishnan, W. Wang, H. Luo, Y. Wang, Y. Xie, Y. Cao and N. Vijaykrishnan. "New-Age: A Negative Bias Temperature Instability-Estimation Framework for Microarchitectural Components." *International Journal of Parallel Programming.*, Vol. 37, No.4, pp.417-431, August, 2009.

- [J13]. M. Mutyam, A. Mupid, F. Wang, N. Vijaykrishnan, Yuan Xie, M. Kandemir. "Process Variation Aware Adaptive Cache Architecture and Management." *IEEE Transactions on Computers.*, Vol. 58, No.7, pp.865-877, July, 2009.
- [J14]. R. Rajaraman, V. Degalahal, J. S. Kim, N. Vijaykrishnan, Y. Xie, M. J. Irwin. "Modeling Soft Errors at Device and Logic Level for Combinational Circuits." *IEEE Transactions on Dependable and Secure Computing (TDCS).*, Vol. 6, No. 3, pp.202-216, June 2009.
- [J15]. Wei-lun Hung, Yuan Xie, Narayanan Vijaykrishnan, Mahmut Kandemir, and Mary Jane Irwin. "Total Power Optimization for Combinational Logics Using Genetic Algorithms." To appear in *Journal of VLSI Signal Processing.*, Published on-line, Feb. 2009.
- [J16]. C. Celik, K.Unlu, K. Ramakrishnan, R. Rajaraman, N. Vijaykrishnan, M. J. Irwin, Y. Xie. "Thermal Neutron Induced Soft Error Rate Measurement in Semiconductor Memories and Circuits." *Journal of Radioanalytical and Nuclear Chemistry.*, Vol. 278, No.2, pp.509-512, Nov 2008.
- [J17]. S. Srinivasan, R. Krishnan, P. Mangalagiri, Yuan Xie, and N. Vijaykrishnan. "Towards Increasing FPGA Lifetime." *IEEE Transactions on Dependable and Secure Computing (TDCS)*, Vol. 5, Issue 2, pp.115-127 Apr-Jun 2008.
- [J18]. Shengqi Yang, W. Wang, W. Wolf, Yuan Xie, N. Vijaykrishnan. "Case Study of Reliability-Aware and Low-Power Design." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 16, Issue 7, pp.861-873, July 2008.
- [J19]. Yuh-fang Tsai, Feng Wang, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin. "Design Space Exploration for Three-Dimensional Cache." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol.16, Issue 4, pp.444-455, Apr. 2008 .
- [J20]. Chang-hong Lin, Yuan Xie, and W.Wolf. "Code Compression for VLIW Embedded Systems Using a Self-Generating Table." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 15. No. 10.,pp.1160-1171, Oct. 2007
- [J21]. Feng Wang, Mike Debole, Xiaoxia Wu, Yuan Xie, N. Vijaykrishnan, and M. J. Irwin. "On-chip Bus Thermal Analysis and Optimization." *IET Computer and Digital Techniques*, Vol. 1, No. 5., pp.590-599, 2007.
- [J22]. Yuan Xie, W.Wolf, and H. Lekatsas. "Decompression Unit Design for VLIW Embedded Processors." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 15. No. 8, pp.975-980, Aug. 2007.
- [J23]. Gabriel Loh, Yuan Xie, and Bryan Black. "Processor Design in Three-Dimensional Die-Stacking Technologies." *IEEE Micro*, Vol. 27. No. 3, pp.31-48, May/June 2007.
- [J24]. Yuan Xie, Lin Li, M. Kandemir, N. Vijaykrishnan, and M. J. Irwin. "Reliability-Aware Co-synthesis for Embedded Systems." *Journal of VLSI Signal Processing*, Vol. 49, No.10, pp.87-99, March 2007.
- [J25]. Yuan Xie, Wei-lun Hung. "Temperature-Aware Task Allocation and Scheduling for Embedded Multiprocessor Systems-on-Chip (MPSoC) Design." *Journal of VLSI Signal Processing*, Vol. 45, No. 3, pp.177-189, December 2006.
- [J26]. Yuan Xie, Gabriel Loh, Bryan Black, and Kerry Bernstein. " Design Space Exploration for 3D Architecture." *ACM Journal of Emerging Technologies for Computer Systems*, Vol. 2. No. 2, pp.65-103, April 2006.
- [J27]. N. Vijaykrishnan and Yuan Xie. " Reliability Concerns in Embedded System Designs." *IEEE Computer*, Vol. 39, No. 1, pp.118-120, January 2006.
- [J28]. Yuan Xie, W.Wolf, and H. Lekatsas. " Code Compression Using Variable-to-fixed Coding." *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, Vol. 14. No. 5, pp.525-536, January. 2006.
- [J29]. Yuan Xie, Jiang Xu, W.Wolf. " Augmenting Platform-based Design with Synthesis Tools." *Journal of Circuits, Systems and Computers*, Vol. 14. No. 5, pp.525-536, April. 2003.

## Book

- [1]. Yuan Xie, Jason Cong, Sachin Sapatnekar. "Three-dimensional IC: Design, CAD, and Architecture." *Springer. 2009*

## Book Chapters

- [1]. Yuan Xie, N. Vijaykrishnan, Chita Das. "3D Network-on-chip Architecture." *Three-dimensional IC: Design, CAD, and Architecture. Edited by Yuan Xie, Jason Cong, Sachin Sapatnekar. Springer.*
- [2]. Yuan Xie, Xiangyu Dong. "System-level Cost Analysis and Design Exploration for 3D ICs." *Three-dimensional IC: Design, CAD, and Architecture. Edited by Yuan Xie, Jason Cong, Sachin Sapatnekar. Springer.*
- [3]. Degalahal, V., R. Ramanarayanan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Effect of Power Optimizations on Soft Error Rate." *IFIP Series on VLSI-SoC. pp. 1-20, 2006. Edited by R. Reis. Springer.*

## Refereed Conference Publications

- [C1]. Shekhar SriKantaiah, Emre Kultursay, Tao Zhang, Mahmut Kandemir, Mary Jane Irwin, and Yuan Xie, “MorphCache: A Reconfigurable Adaptive Multi-level Cache Hierarchy for CMPs”, *To appear in the IEEE International Symposium on High-Performance Computer Architecture Conference (HPCA), 2011*
- [C2]. Cong Xu, Xiangyu Dong, Norm Jouppi, and Yuan Xie “Design Implications of Memristor-Based RRAM Cross-Point Structures”, *To appear in Proceedings of ACM/IEEE Design Automation and Test in Europe Conference (DATE), 2011*
- [C3]. Jishen Zhao, Xiangyu Dong, and Yuan Xie “An Energy-Efficient 3D CMP Design with Fine-Grained Voltage Scaling”, *To appear in Proceedings of ACM/IEEE Design Automation and Test in Europe Conference (DATE), 2011*
- [C4]. Jin Ouyang and Yuan Xie “Enabling Quality-of-Service in Nanophotonic Network-on-Chip”, *To appear in Proceedings of ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC 2011), 2011*
- [C5]. Xiangyu Dong and Yuan Xie “AdaMS: Adaptive MLC/SLC Phase-Change Memory Design for File Storage”, *To appear in Proceedings of ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC 2011), 2011*
- [C6]. Jin Ouyang and Yuan Xie “LOFT: A High Performance Network-on-Chip Providing Quality-of-Service Support”, *To appear in Proceedings of Intl. Symp. on Microarchitecture (MICRO 2010), 2010*
- [C7]. Tao Zhang, Kui Wang, Yi Feng, Yan Chen, Qun Li, Bing Shao, Xiaodi Song, Lian Duan, Yuan Xie, Xu Cheng, Yong-long Lin, “A 3D SoC Design for H.264 Application With On-Chip DRAM Stacking”, *To appear in Proceedings of IEEE International 3D System Integration Conference (3DIC), 2010*
- [C8]. Jing Xie, Xiangyu Dong, Yuan Xie “3D Memory Stacking for Fast Checkpointing/Restore Applications”, *To appear in Proceedings of IEEE International 3D System Integration Conference (3DIC), 2010*
- [C9]. Tao Zhang, Kui Wang, Yi Feng, Lian Duan, Xiaodi Song, Yuan Xie, Xu Cheng, Yong-long Lin, “A Customized Design of DRAM Controller for On-Chip 3D DRAM Stacking”, *To appear in Proceedings of Custom IC Conference (CICC 2010), 2010*
- [C10]. Xiangyu Dong, Yuan Xie, Norm Jouppi, Naveen Muralimanohar “Simple but Effective Heterogeneous Main Memory with On-Chip Memory Controller Support” *To appear in Proceedings of Supercomputing (SC 2010), 2010.*
- [C11]. Li Jiang, Qiang Xu, Lian Duan, Yuan Xie, “Modeling TSV Open Defects in 3D-Stacked DRAM”, *To appear in Proceedings of Int. Conf. on Testing (ITC 2010), Nov, 2010.*
- [C12]. Jin Ouyang, Jing Xie, Matt Poremba, Yuan Xie “Design Methodology of 3D Network-on-Chip with Inductive/Capacitive-Coupling Vertical Interconnect” *To appear in Proceedings of Int. Conf. on CAD (ICCAD), Nov, 2010.*
- [C13]. Yibo Chen, Dimin Niu, Yuan Xie, Krish Chakrabarty “Cost-Effective Integration of Three-Dimensional (3D) ICs Emphasizing Testing Cost Analysis” *To appear in Proceedings of Int. Conf. on CAD (ICCAD), Nov, 2010.*
- [C14]. Yibo Chen, Jishen Zhao, Yuan Xie “3D-NonFAR: Three-Dimensional Non-Volatile FPGA ARchitecture Using Phase Change Memory.” *To appear in Proceedings of Intl. Symp. Low Power Electronic Devices (ISLPED). August, 2010. (25% acceptance rate).*
- [C15]. Dimin Niu, Yiran Chen, Yuan Xie “Dual-element Memristor-Based Memory Design.” *To appear in Proceedings of Intl. Symp. Low Power Electronic Devices (ISLPED). August, 2010. (25% acceptance rate).*
- [C16]. Jishen Zhao, Xiangyu Dong, Yuan Xie “Cost-Aware Three-Dimensional (3D) Many-Core Multiprocessor Design.” *Proceedings of Design Automation Conference (DAC). 2010. (24% acceptance rate).*
- [C17]. Dimin Niu, Yiran Chen, Cong Xu, Yuan Xie “Impact of Process Variations on Emerging Memristor.” *To appear in Proceedings of Design Automation Conference (DAC). 2010. (24% acceptance rate).*
- [C18]. Xiaoxia Wu, Guangyu Sun, Reetuparna Das, Yuan Xie, Jian Li, Chita R. Das “Cost-driven 3D Integration with Interconnect Layers.” *To appear in Proceedings of Design Automation Conference (DAC). 2010. (24% acceptance rate).*
- [C19]. Yongsoo Joo, Dimin Niu, Guangyu Sun, Xiangyu Dong, Yuan Xie “Energy- and Endurance-Aware Design of Phase Change Memory Caches.” *To appear in Proceedings of Design Automation and Test in Europe (DATE). 2010. (25% acceptance rate).*
- [C20]. Guangyu Sun, Yongsoo Joo, Yibo Chen, Yuan Xie, Yiran Chen, Helen Li “A Hybrid Solid-State Storage Architecture for Performance, Energy Consumption and Lifetime Improvement.” *Proceedings of High Performance Computer Architecture (HPCA). 2010. (18% acceptance rate).*

- [C21]. Yuan Xie “Processor Architecture Design Using 3D Integration Technology.(Invited Paper)” *Proceedings of VLSI Design. 2010*.
- [C22]. Yibo Chen, Yu Wang, Yuan Xie, Andres Takach “Parametric Yield Driven Resource Binding in Behavioral Synthesis with Multi-Vth/Vdd Library.” *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC). 2010*. (33% acceptance rate(115/340)) (**Best Paper Nomination**).
- [C23]. Yibo Chen, Yu Wang, Yuan Xie, Andres Takach “Minimizing Leakage Power in Aging-Bounded High-level Synthesis with Design Time Multi-Vth Assignment.” *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC). 2010*. (33% acceptance rate(115/340)).
- [C24]. Dimin Niu, Yibo Chen, Xiangyu Dong, Yuan Xie “Energy and Performance Driven Circuit Design for Emerging Phase-Change Memory.” *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC). 2010*. (33% acceptance rate(115/340)).
- [C25]. Paul Falkstern, Yao-wen Chang, Yuan Xie, Yu Wang “Three Dimensional Integrated Circuit (3D IC) Floorplan and Power/Ground Network Co-synthesis.” *Proceedings of Asia and South-Pacific Design Automation Conference (ASP-DAC). 2010*. (33% acceptance rate(115/340)).
- [C26]. Xiangyu Dong, Naveen Muralimanohar, Norm Jouppi, Richard Kaufmann, Yuan Xie “Leveraging 3D PCRAM Technologies to Reduce Checkpoint Overhead for Future Exascale Systems.” *Proceedings of International Conference on High Performance Computing, Networking, Storage and Analysis (SC). 2009*. (22% acceptance rate(59/261)).
- [C27]. Xiangyu Dong, Norm Jouppi, Yuan Xie “PCRAMsim: System-Level Performance, Energy, and Area Modeling for Phase-Change RAM.” *Proceedings of International Conference on Computer-Aided Design (ICCAD). 2009*. pp 269-275. (26% acceptance rate(115/438)).
- [C28]. Balaji Vaidyanathan, Anthony S. Oates, Yuan Xie “Intrinsic NBTI-Variability Aware Statistical Pipeline Performance Assessment and Tuning.” *Proceedings of International Conference on Computer-Aided Design (ICCAD). 2009*. pp 164-171. (26% acceptance rate(115/438)).
- [C29]. Xiaoxia Wu, Jian Li, Lixi Zhang, Evan Speight, Yuan Xie. “Hybrid Cache Architecture with Disparate Memory Technologies.” *Proceedings of International Symposium on Computer Architecture (ISCA)*, pp.34-45, June. 2009.
- [C30]. Yu Wang, Xiaoming Chen, Wenping Wang, Yu Cao, Yuan Xie, Huazhong Yang. “Gate Replacement Techniques for Simultaneous Leakage and Aging Optimization.” *Proceedings of Design Automation and Test in Europe (DATE)*, pp. 324-333. April. 2009.
- [C31]. Xiaoxia Wu, Jian Li, Lixi Zhang, Evan Speight, Yuan Xie. “Power and Performance of Read-write aware hybrid caches with non-volatile memories.” *Proceedings of Design Automation and Test in Europe (DATE)*, pp. 737-742. April. 2009.
- [C32]. Guangyu Sun, Xiangyu Dong, Yuan Xie, Jian Li, Yiran Chen. “A Novel MRAM Stacking Architecture for Chip-multiprocessors (CMP).” *Proceedings of High Performance Computer Architecture (HPCA)*, pp. 239-249. Feb. 2009. (19% acceptance rate(34/185)).
- [C33]. Xiangyu Dong and Yuan Xie. “System-level Cost Analysis and Design Exploration for 3D ICs.” *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. **Best Paper Award Nomination**. (32% acceptance rate(116/355)).
- [C34]. Mike Debole, Guangyu Sun, Yuan Xie, Vijaykrishnan Narayanan “A Criticality-Driven Microarchitectural Three Dimensional (3D) Floorplanner.” *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. (32% acceptance rate(116/355)).
- [C35]. Feng Wang, Andres Takach, and Yuan Xie. “Variation-Aware Resource Sharing and Binding in Behavioral Synthesis.” *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. (32% acceptance rate(116/355)).
- [C36]. Yibo Chen and Yuan Xie. “Tolerating Process Variations in High-Level Synthesis Using Transparent Latches.” *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. (32% acceptance rate(116/355)).
- [C37]. Mike Debole, Wenping Wang, Yu Wang, Yuan Xie, Vijay Nayaranan, Yu Cao. “A Framework for Estimating NBTI Degradation of Microarchitectural Components” *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2009. (32% acceptance rate(116/355)).
- [C38]. P. Mangalagiri, S. Bae, R. Krishnan, Yuan Xie, N. Vijaykrishnan. “Thermal-Aware Reliability Analysis for Platform FPGAs ” *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp. 722-727, Nov. 2008. (122 out of 458 submissions, 27% acceptance rate).

- [C39]. Xiaoxia Wu, Yibo Chen, Krish Chakrabarty, and Yuan Xie. "Test-Access Mechanism Optimization for Core-Based Three-Dimensional SOCs." *Proceedings of International Conference on Computer Design (ICCD)*, pp.212-218 Oct. 2008.
- [C40]. Dongkook Park, Soumya Eachempati, Reetuparna Das, Asit K. Mishra, Yuan Xie, N. Vijaykrishnan, Chita R. Das "MIRA: A Multi-Layered On-Chip Interconnect Router Architecture" *Proceedings of International Symposium on Computer Architecture (ISCA)*, June. 2008. (37 out of 259 submissions, 14% acceptance rate)
- [C41]. Xiangyu Dong, Xiaoxia Wu, Guangyu Sun, Yuan Xie, Helen Li, Yiran Chen "Circuit and Microarchitecture Evaluation of 3D Stacking Magnetic RAM (MRAM) as a Universal Memory" *Proceedings of Design Automation Conference (DAC)*, pp.554-559, June. 2008. (138 out of 639 submissions, 21% acceptance rate)
- [C42]. Hai Lin, Guangyu Sun, Yunsi Fei, Yuan Xie, Anand Sivasubramaniam "Thermal-aware Design Considerations for Application-Specific Instruction Set Processor" in *Proceedings of International Symposium on Application Specific Processors*, June. 2008. (19 out of 64 submissions, 29% acceptance rate)
- [C43]. Xiangyu Dong, Xiaoxia Wu, Yuan Xie "Cost Analysis and Cost-driven EDA flow for 3D ICs" in *Proceedings of 3D-SIC Conference*, May. 2008.
- [C44]. Feng Wang, Guangyu Sun, Yuan Xie. "A Variation Aware High Level Synthesis Framework." *Proceedings of Design Automation and Test in Europe (DATE)*, pp.1063-1068, Mar. 2008. (198 out of 839 submissions, 23% acceptance rate)
- [C45]. Feng Wang, Xiaoxia Wu, Yuan Xie. "Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning." To appear in *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2008. **Best Paper Award.** (29% acceptance rate for regular papers (100/351)).
- [C46]. Feng Wang, Xiaoxia Wu, C. Nicopoulos, Yuan Xie, N. Vijaykrishnan. "Variation-aware Task Allocation and Scheduling for MPSoC." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp. 138-149, Nov. 2007. (139 out of 510 submissions, 27% acceptance rate).
- [C47]. Xiaoxia Wu, Paul Falkenstern, and Yuan Xie. "Scan Chain Design for Three-dimensional(3D) ICs." *Proceedings of International Conference on Computer Design (ICCD)*, pp.208-214, Oct. 2007. (88 out of 259 submissions, 33% acceptance rate).
- [C48]. S. Srinivasan, P. Mangalagiri, Yuan Xie, N. Vijaykrishnan. "FPGA Routing Architecture Analysis Under Variations." *Proceedings of International Conference on Computer Design (ICCD)*, pp.152-157, Oct. 2007. (88 out of 259 submissions, 33% acceptance rate).
- [C49]. J. Kim, C. Nicopoulos, D. Park, R. Das, Yuan Xie, N. Vijaykrishnan, C. Das. "A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures." *Proceedings of the Annual International Symposium on Computer Architecture (ISCA)*, pp. 138-149, June 2007. (46 papers accepted out of 204 submissions. 23% acceptance rate)
- [C50]. Feng Wang, Yuan Xie, and Hai Ju. "A Novel Criticality Computation Method in Statistical Timing Analysis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1611-1616, April 2007. (208 papers accepted out of 933 submissions. 22% acceptance rate)
- [C51]. Y. Wang, H. Luo, K. He, R. Luo, Yuan Xie, and H. Yang. "Temperature-aware NBTI Modeling and the Impact of Input Vector Control on Performance Degradation." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 546-551, April 2007. (208 papers accepted out of 933 submissions. 22% acceptance rate)
- [C52]. Feng Wang and Yuan Xie. "Soft Error Rate Analysis for Combinational Logic Using An Accurate Electrical Masking Model." *Proceedings of IEEE International Conference on VLSI Design (VLSID)*, pp. 165-170, Jan. 2007. (141 papers accepted out of 432 submissions. 32% acceptance rate)
- [C53]. Balaji Vaidyanathan, W-L. Hung, Feng Wang, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Architecting Microprocessor Components in 3D Design Space." *Proceedings of IEEE International Conference on VLSI Design (VLSID)*, pp. 103-108, Jan. 2007. (141 papers accepted out of 432 submissions. 32% acceptance rate)
- [C54]. Wei-lun Hung, Xiaoxia Wu, Yuan Xie. "Guaranteeing Performance Yield in High-Level Synthesis." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp.303-309, Nov. 2006. **Best paper award nomination.**(130 papers accepted out of 537 submissions. 24% acceptance rate).
- [C55]. S. Srinivasan, M. Prasanth, S. Karthik, Yuan Xie, N. Vijaykrishnan. "FLAW: FPGA Lifetime Awareness." *Proceedings of the 43rd Design Automation Conference (DAC)*, pp. 630-635, July. 2006. (209 papers accepted out of 865 submissions. 24% acceptance rate)
- [C56]. F. Li, C. Nicopoulos, T. Richardson, Yuan Xie, N. Vijaykrishnan, M. Kandemir. "Design and Management of 3D Chip Multiprocessors using Network-in-memory." *Proceedings of the Annual International Symposium on Computer Architecture*

(ISCA), pp. 130-141, June. 2006. (31 papers accepted out of 234 submissions. 13% acceptance rate)

[C57]. Feng Wang, Yuan Xie. "An Accurate and Efficient Model of Electrical Masking Effect for Soft Errors in Combinatorial Logic." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.

[C58]. B. Vaidyanathan, Yuan Xie, N. Vijaykrishnan. "Soft Error Analysis and Optimizations of C-elements in Asynchronous Circuits." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.

[C59]. R. Ramanarayanan, R. Krishnan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Temperature and Voltage Scaling Effects on Electrical Masking." *Proceedings of the Second Workshop on System Effects of Logic Soft Errors (SELSE)*, April 2006.

[C60]. Wei-lun Hung, G. Link, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Interconnect and Thermal-aware Floorplanning for 3D Microprocessors." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 98-104, March. 2006. (93 papers accepted out of 256 submissions. 36% acceptance rate)

[C61]. Feng Wang, Yuan Xie, N. Vijaykrishnan and M. J. Irwin. "On-chip Bus Thermal Analysis and Optimization." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 850-855, March 2006. (233 papers accepted out of 834 submissions. 28% acceptance rate)

[C62]. Feng Wang, Yuan Xie, K. Bernstein and Y. Luo. "Dependability Analysis of Nano-scale FinFET Circuits." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 399-404, March 2006.

[C63]. M. Mutyam, M. Eze, N. Vijaykrishnan, Yuan Xie. "Delay and Energy Efficient Data Transmission for On-Chip Buses." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 355-360, March 2006.

[C64]. S. Yang, W. Wolf, N. Vijaykrishnan, Yuan Xie. "Reliability-Aware SOC Voltage Islands Partition and Floorplan." *Proceedings of the IEEE Computer Society Annual Symposium on VLSI Design (ISVLSI)*, pp. 343-348, March 2006.

[C65]. O. Ozturk, F. Wang, M. Kandemir, Yuan Xie. "Optimal Topology Exploration for Application-Specific 3D Architectures." *Proceedings of Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 390-395, Jan. 2006. (135 papers accepted out of 432 submissions. 31% acceptance rate)

[C66]. Ramanarayanan, R., J. S. Kim, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "SEAT-LA: A Soft Error Analysis tool for Combinational Logic." *Proceedings of IEEE International Conference on VLSI Design*, pp. 499-502, Jan. 2006. (26.8% acceptance rate for regular papers (88 out of 328 submissions))

[C67]. T. Richardson, C. Nicopoulos, D. Park, N. Vijaykrishnan, Yuan Xie, C. R. Das. "A Hybrid SoC Interconnect with Dynamic TDMA-Based Transaction-Less Buses and On-Chip Networks." *Proceedings of IEEE International Conference on VLSI Design*, pp. 499-502, Jan. 2006. (26.8% acceptance rate for regular papers)

[C68]. R. Luo, H. Luo, H. Yang, Yuan Xie. "An Instruction Level Analytical Power Model for Designing Low Power SOC." *Proceedings of IEEE International Conference on ASICs*, pp.1070-1073, Oct. 2005.

[C69]. T. Richardson and Yuan Xie. "Evaluation of Thermal-Aware Design Techniques for Microprocessors." *Proceedings of IEEE International Conference on ASICs*, pp.62-65, Oct. 2005.

[C70]. W-L. Hung, G. Link, Yuan Xie, N. Vijaykrishnan, N. Dhanwada, J. Conner. "Temperature-Aware Voltage Islands Architecting in System-on-Chip Design." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 689-696, Oct. 2005. (101 out of 313 submissions, 32% acceptance rate)

[C71]. S. K. Narayanan, G. Chen, M. Kandemir, Yuan Xie. "Temperature-Sensitive Loop Parallelization for Chip Multiprocessors." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 677-682, Oct. 2005. (101 out of 313 submissions, 32% acceptance rate)

[C72]. Y-F. Tsai, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Three-Dimensional Cache Design Exploration Using 3DCacti." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 519-524, Oct. 2005. (101 out of 313 submissions, 32% acceptance rate)

[C73]. D. Hostetler and Yuan Xie. "Adaptive Power Management in Software Radios Using Resolution Adaptive Analog to Digital Converters." *Proceedings of IEEE International Symposium on VLSI (ISVLSI)*, pp. 186-191, May. 2005.

[C74]. W-L. Hung, Yuan Xie, N. Vijaykrishnan, C. Addo-Quaye, T. Theocharides, M. J. Irwin "Thermal-Aware Floorplanning Using Genetic Algorithms." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 634-639, Mar. 2005. (83 out of 222 submissions, 37% acceptance rate)

[C75]. S. Tosun, O. Ozturk, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "An ILP Formulation for Reliability-Oriented High-Level Synthesis." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 364-369, Mar. 2005. (83 out of 222 submissions, 37% acceptance rate)

- [C76]. S. Tosun, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "Reliability-Centric Hardware/Software Co-design." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 364-369, Mar. 2005. (83 out of 222 submissions, 37% acceptance rate)
- [C77]. S. Tosun, N. Mansouri, E. Arvas, M. Kandemir, Yuan Xie. "Reliability-centric High-level Synthesis." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 1258-1263, March 2005. (176 papers accepted out of 825 submissions. 21% acceptance rate)
- [C78]. S. Yang, W. Wolf, N. Vijaykrishnan, Yuan Xie. "Power Attack Resistant Crypto Design: A Dynamic Voltage and Frequency Switching Approach." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 64-69, March 2005. (21% acceptance rate)
- [C79]. Wei-lun Hung, Yuan Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. "Thermal-Aware Allocation and Scheduling for Systems-on-a-Chip Design." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 898-899, March 2005. (21% acceptance rate)
- [C80]. Y-F Tsai, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Leakage-Aware Interconnect for On-Chip Network." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 230-231, March 2005. (21% acceptance rate)
- [C81]. J.Conner,Yuan Xie, M. Kandemir, R. Dick, G. Link. "FD-HGAC: A Hybrid Heuristic/Genetic Algorithm Hardware/Software Co-synthesis Framework with Fault Detection." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*., pp. 709-712, Jan. 2005. (99 regular papers accepted out of 692 submissions (14.3%))
- [C82]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Yuan Xie. "Low-Leakage Robust SRAM Cell Design for Sub-100nm Technologies." *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*., pp. 539-544, Jan. 2005. 14.3% acceptance rate for regular papers (99 regular papers accepted out of 692 submissions (14.3%))
- [C83]. Y-F. Tsai, N. Vijaykrishnan, M. J. Irwin, Yuan Xie. "Influence of Leakage Reduction Techniques on Delay/Leakage Uncertainty." *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 374-379, Jan. 2005. (97 regular papers accepted out of 352 submissions (28%)).
- [C84]. S. Yang, W. Wolf, W. Wang, N. Vijaykrishnan, Yuan Xie. "Accurate Stacking Effect Macro-Modeling of Leakage Power in Sub-100nm Circuits." *Proceedings of the 18th International Conference on VLSI Design (VLSID)*, pp. 165-170, Jan. 2005. (97 regular papers accepted out of 352 submissions (28%)).
- [C85]. S. Srinivasan, A. Gayasen, N. Vijaykrishnan, M. Kandemir, Yuan Xie, M. J. Irwin. "Improving Soft-error Tolerance of FPGA Configuration Bits." *Proceedings of International Conference on Computer Aided Design (ICCAD)*, Nov. 2004. (24% acceptance rate).
- [C86]. W-L Hung, C. Addo-Quaye, T. Theocharides, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "Thermal-Aware IP Virtualization and Placement for Networks-on-Chip Architecture." *Proceedings of IEEE International Conference on Computer Design (ICCD)*, pp. 430-437, Oct. 2004. (84 out of 226 submissions, 37% acceptance rate.)
- [C87]. Yuan Xie, L. Li, M. Kandemir, N. Vijaykrishnan, M. J. Irwin. "Reliability-aware Cosynthesis for Embedded Systems." *Proceedings of IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP)*, pp. 41-50, Sept. 2004.
- [C88]. W-L. Hung, Yuan Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin. "Total Power Optimization Through Simultaneously Multiple-VDD Multiple-VTH Assignment and Device Sizing With Stack Forcing." *Proceedings of International Symposium on Low Power Electronics and Design (ISLPED 2004)*, pp. 144-149, Aug. 2004. 34% acceptance rate)
- [C89]. W. Xu, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "Design of a Nanosensor Array Architecture." *Proceedings of Great Lakes Symposium on VLSI(GLSVLSI)*, pp. 298-303, Apr. 2004. (23 full papers accepted out of 235 submissions, 10% rate)
- [C90]. V. Degalahal, R. Ramnarayanan, N. Vijaykrishnan, Yuan Xie, M. J. Irwin. "The Effect of Threshold Voltages on the Soft Error Rate." *Proceedings of International Symposium on Quality Electronic Design (ISQED)*, pp. 503-508, Mar. 2004. (49 papers accepted out of 148 submissions, 33%)
- [C91]. C-H. Lin, W. Wolf, and Yuan Xie. "LZW-based Code Compression for VLIW Embedded Systems." *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 76-81, Feb. 2004. (181 papers accepted out of 780 submissions (23%))
- [C92]. Yuan Xie. "Analysis of Two Code Compression Algorithms for Embedded Systems." *Proceedings of International Conference on ASIC (ASICON)*, pp. 773-776. Oct. 2003.

- [C93]. Yuan Xie, Wayne Wolf, H. Lektasas. “Code Compression Using Arithmetic Coding Based Variable-to-fixed Coding.” *Proceedings of Data Compression Conference(DCC 2003)*, pp. 382-391, Mar. 2003.
- [C94]. Yuan Xie, W. Wolf, and H. Lektasas. “Profile-driven Code Compression.” *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 76-81, Mar. 2003. (152 out of 590 submissions (25%))
- [C95]. Yuan Xie, W. Wolf, and H. Lektasas. “Code Compression for VLIW Using Variable-to-fixed Coding.” *Proceedings of Fifteenth International Symposium on System Synthesis (ISSS 2002)*, pp. 138-143, Oct. 2002. (24 out of 71 submissions (33%))
- [C96]. Yuan Xie, W. Wolf, and H. Lektasas. “A Code Decompression Architecture for VLIW Processors.” *Proceedings of the Thirty-Fourth International Symposium on Microarchitecture (MICRO-34)*. pp. 66-75. (29 out of 144 submissions, 20% acceptance rate)
- [C97]. Yuan Xie, W. Wolf, and H. Lektasas. “Compression Ratio and Decompression Overhead Tradeoffs in Code Compression for VLIW Architectures.” *Proceedings of the Fourth International Conference on ASIC (ASICON)*. **Best Paper Award**.
- [C98]. Yuan Xie, W. Wolf. “ASICosyn: Co-Synthesis of Conditional Task Graphs with Custom ASICs.” *Proceedings of the Fourth International Conference on ASIC (ASICON)*.
- [C99]. Yuan Xie, W. Wolf. “Allocation and Scheduling of Conditional Task Graphs in Co-synthesis.” *Proceedings of IEEE International Conference on Design Automation and Test in Europe (DATE)*, pp. 620-625, Mar. 2001. (81 full papers out of 300 submissions (27%))
- [C100]. Yuan Xie, Hua Lin, Zhao Wu, W. Wolf. “CAD Techniques for Multimedia System Design.” *Proceedings of Synthesis and System Integration of Mixed Technologies (SASIMI)*, Mar. 2000.
- [C101]. Yuan Xie and Wayne Wolf. “Co-synthesis with Custom ASICs.” *Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC)*, pp. 129-134, Jan. 2000.

## Patent

- [1]. United States Patent. No.7,095,343. “Code Compression Algorithms and Architectures for Embedded Systems.” Issued on August 22, 2006.

## Student Supervision

### Doctoral Dissertations Supervised

- 2010      **Soumya Eachempati**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)  
*Influence of Emerging Technologies on Interconnect Architectures*  
First Employer: Intel.
- 2010      **Prasanth Mangalagiri**, Ph.D. in Computer Science and Engineering (co-advise with N. Vijaykrishnan)  
*A Reliability and Process Variation Aware Design flow for Platform FPGAS*  
First Employer: Intel.
- 2010      **Xiaoxia Wu**, Ph.D. in Computer Science and Engineering  
*Design Space Exploration for 3D ICs*  
First Employer: Qualcomm.
- 2009      **Balaji Vaidyanthan**, Ph.D. in Computer Science and Engineering  
*Reliability Analysis and Optimization for Nanoscale System-on-Chip Design*  
First Employer: TSMC, Taiwan.
- 2008      **Feng Wang**, Ph.D. in Computer Science and Engineering  
*Design Automation Techniques to Mitigate Process Variations*  
First Employer: Qualcomm.
- 2007      **Yu Wang**, Ph.D. in Electronic Engineering, Tsinghua University (co-advise with Prof. Huazhong Yang)  
*Optimization for the Leakage Current and Reliability in Digital Integrated Circuits*  
Current Job: Assistant Professor in Tsinghua University.
- 2006      **Wei-lun Hung**, Ph.D. in Computer Science and Engineering  
*Designing Cool Chips: Low Power and Thermal-Aware Design Methodologies*  
Current Employer: Sun Microsystems.

### Master Thesis Supervised

- 2008 **Paul Falkenstern**, M.S. in Computer Science and Engineering  
*Design Automation Tools for 3D ICs*  
First job: Lockheed Martin Inc.
- 2007 **Han-wei Chen**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)  
*Impact of Circuit Degradation on Design Security of Field Programmable Devices*  
Now graduate student at University of Texas at Austin.
- 2007 **Charles Addo-Quaye**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)  
*Thermal-Aware Placement and Virtualization for Three Dimensional Network-on-Chip Designs*  
Now Ph.D. student at PennState.
- 2007 **Melvin Eze**, M.S. in Computer Science and Engineering (co-advised with N.Vijaykrishnan)  
*Delay and Energy Efficient Data Transmission for On-Chip Buses*  
Now Ph.D. student at PennState.
- 2006 **Yinkun Xue**, M.S. in Computer Science and Engineering  
*Providing Energy-Aware Map Services to Mobile Devices*  
First job: Siemens Inc.
- 2005 **Thomas Richardson**, M.S. in Computer Science and Engineering  
*Analysis and Design of Scalable SoC Interconnects*  
First job: Avallink Inc.

### Current Students

- Post-Doc **Yongsoo Joo**, Ph.D. from Seoul National University, Korea.
- Post-Doc **Lian Duan**, Ph.D. from Peking University, China.
- Ph.D. **Mike Debole**, Ph.D. in Computer Science and Engineering, expected graduation date: 12/2010
- Ph.D. **Guangyu Sun**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2011
- Ph.D. **Yibo Chen**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2012
- Ph.D. **Xiangyu Dong**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2012
- Ph.D. **Jin Ouyang**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2012
- Ph.D. **Dimin Niu**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2013
- Ph.D. **Tao Zhang**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2013
- Ph.D. **Jing Xie**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2014
- Ph.D. **Jishen Zhao**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2014
- Ph.D. **Cong Xu**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2014
- Ph.D. **Qiaosha Zou**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2015
- Ph.D. **Matthew Poremba**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2015
- Ph.D. **Hsiang-Yun Cheng**, Ph.D. in Computer Science and Engineering, expected graduation date: 6/2015
- Ph.D. **Jue Wang**, Ph.D. in Computer Science and Engineering, expected graduation date: 1/2016

### Teaching

Semester	Course	Course Evaluation
Fall 2003	<b>CSE 597A</b> <i>Modern VLSI Design</i>	6.29 out of 7
Fall 2003	<b>CSE 598C</b> <i>Reliable and Low Power Design</i>	6.13 out of 7
Spring 2004	<b>CSE 477</b> <i>VLSI Digital Circuits</i>	5.50 out of 7
Fall 2004	<b>CSE 578</b> <i>CAD Tools</i>	5.91 out of 7
Spring 2005	<b>CSE 477</b> <i>VLSI Digital Circuits</i>	5.17 out of 7
Fall 2005	<b>CSE 578</b> <i>CAD Tools</i>	6.78 out of 7
Spring 2006	<b>CSE 331.1</b> <i>Computer Organization and Design</i>	5.54 out of 7
Spring 2006	<b>CSE 331.2</b> <i>Computer Organization and Design</i>	6.11 out of 7

Fall 2006	<b>CSE 578</b> <i>CAD Tools</i>	5.88 out of 7
Fall 2006	<b>CSE 431</b> <i>Introduction to Computer Architecture</i>	6.31 out of 7
Spring 2007	<b>CSE 477</b> <i>VLSI Digital Circuits</i>	6.53 out of 7
Fall 2008	<b>CSE 578</b> <i>CAD Tools</i>	6.53 out of 7
Spring 2008	<b>CSE 411</b> <i>VLSI Digital Circuits</i>	6.29 out of 7

## Short Courses

06/2009	[1]. One-week Course in China DragonStar Program, <b>Chinese Academy of Science.</b> “Advanced Modern Architecture and VLSI Design”	<b>Beijing, China</b>
05/2007	[2]. 3-week Summer Short Course, <b>Tsinghua University.</b> “Advanced VLSI Design”	<b>Beijing, China</b>
08/2006	[3]. 3-week Summer Short Course, <b>Tsinghua University.</b> “Advanced VLSI Design”	<b>Beijing, China</b>
05/2004	[4]. 2-day Industrial Short Course, <b>Pittsburgh Digital Greenhouse.</b> “Design of Reliable Power-Efficient Systems”	<b>Pittsburgh, PA</b>
01/2004	[5]. 2-day Industrial Short Course, <b>Pittsburgh Digital Greenhouse.</b> “Design of Reliable Power-Efficient Systems”	<b>Pittsburgh, PA</b>

## Tutorials

11/2010 ICCAD-10	[1]. <b>Half-day Tutorial: “Manufacturing, CAD and Thermal-Aware Design for 3-D MPSoCs”</b> <i>with David Atienza (EPFL), Sani Nassif (IBM), Ayse K. Coskun (Boston University)</i> <b>IEEE/ACM Intl. Conf. on CAD</b>
6/2010 DAC-10	[2]. <b>Full-day Tutorial: “3D IC: New Dimensions in IC Design”</b> <i>with Ruchir Puri (IBM), Tanay Karnik (Intel), David Atienza (EPFL), Paul Marchal (IMEC)</i> <b>IEEE/ACM Design Automation Conference</b>
3/2010 SC-09	[3]. <b>Half-day Tutorial: “The Impact of Emerging Technology on Computer System Design”</b> <i>Norm Jouppi (HP Labs) and Yuan Xie</i> <b>Architecture Support for Programming Language and Operating Systems (ASPLOS) 2010</b>
1/2010 ASPDAC-10	[4]. <b>Full-day Tutorial: “3D Integrated Circuit Design”</b> <i>with Ruchir Puri (IBM), Paul Franzon (NCSU) and Sachin Sapatnekar (UMN)</i> <b>ACM Asia and South-Pacific Design Automation Conference</b>
1/2010 VLSI Design-10	[5]. <b>Embedded Tutorial: “Processor Design using 3D Integrations”</b> <b>IEEE Symposium on VLSI Design Conference</b>
12/2009 MICRO-2009	[6]. <b>Half-day Tutorial: “Integrated Multi-core Modeling”</b> <i>with Pradip Bose (IBM) and Eren Kursun (IBM)</i> <b>42nd International Symposium on Microarchitecture</b>
11/2009 SC-09	[7]. <b>Half-day Tutorial: “The Impact of Emerging Technology on Computer System Design”</b> <i>Norm Jouppi (HP Labs) and Yuan Xie</i> <b>Supercomputing 2009</b>
04/2009 VLSI/DAT-09	[8]. <b>Half-day Tutorial: “3D Integration”</b> <i>Yuan Xie</i> <b>International Symposium on VLSI/DAT</b>
06/2008 ISCA-08	[9]. <b>Half-day Tutorial: “3D Integration for Microarchitectures”</b> <i>organized with G. Loh (Gatech)</i> <b>International Symposium on Computer Architecture</b>
5/2006 GLSVLSI-08	[10]. <b>Half-day Tutorial: “Technology, EDA, and Architecture for Emerging 3D Integration”</b> <i>with Syed Alam (Freescale), Mike Ignatowski (IBM)</i> <b>Greatlake Symposium on VLSI (GLSVLSI), 2008</b>
12/2006 MICRO-06	[11]. <b>Half-day Tutorial: “3D Integration for Microarchitectures”</b> <i>with K. Bernstein (IBM), B. Black (Intel), and G. Loh (Gatech)</i> <b>International Symposium on Microarchitecture (MICRO-39)</b>

- 8/2006  
VLSI06 [12]. **Half-day Tutorial: “Thermal-Aware Design Techniques for Nanometer VLSI Chips”**  
**The 17th VLSI Design/CAD Symposium**
- 10/2005  
ASIC05 [13]. **Half-day Tutorial: “Thermal-Aware Design Techniques for Nanometer VLSI Chips”**  
**The 6th International Conference on ASIC (ASIC05)**
- 06/2005  
ISCA05 [14]. **Half-day Tutorial: “Robust Systems Design from Unreliable Components”**  
*with S. Mitra (Intel), L. Spainhower (IBM), and N. Vijaykrishnan (PSU)*  
**International Symposium on Computer Architecture (ISCA)**
- 01/2005  
ASP05 [15]. **Half-day Tutorial: “Designing Reliable Circuit in the Presence of Soft Errors”**  
**Asia-South-Pasific Design Automation Conference (ASP-DAC)**
- 10/2004  
ASP04 [16]. **Full-day Tutorial: “Computing in the Presence of Soft Errors ”**  
*with N. Vijaykrishnan (PSU)*  
**Intl. Conf. on Architectural Support for Programming Languages and Operating Systems**

## Invited Talks

- 10/2010 [1]. Invited talk, **National Cheng Kung University** **Tainan, Taiwan**  
“Emerging Memory Technologies and the Impact on Computer System Design”
- 10/2010 [2]. Invited talk, **National Cheng Kung University** **Tainan, Taiwan**  
“Design Challenges for 3D ICs”
- 09/2010 [3]. Invited talk, **Global Semiconductor Alliance (GSA)** **San Jose, CA**  
“ System Level Cost Analysis and Design Exploration for 3D ICs”
- 9/2010 [4]. Invited talk, **Industrial Technology Research Institute(ITRI)** **Tainan, Taiwan**  
“Design Challenges for 3D ICs”
- 9/2010 [5]. Invited talk, **Korea Advanced Institute of Science and Technology (KAIST) University** **Daejeon, Korea**  
“Design Challenges for 3D ICs”
- 7/2010 [6]. Invited talk, **China Computer Federation** **Beijing, China**  
“Emerging Technologies and the Impact on Computer System Design”
- 6/2010 [7]. Invited talk, **Qualcomm** **San Diego, CA**  
“Emerging Memory Technologies and the Impact on Computer System Design”
- 5/2010 [8]. Invited talk, **IMEC (Interuniversity Microelectronic Centre)** **Leuven, Belgium**  
“Emerging Memory Technologies and the Impact on Computer System Design”
- 5/2010 [9]. Invited talk, **ETH Zurich** **Zurich, Switzerland**  
“3D IC Design, EDA, and Architecture”
- 4/2010 [10]. Invited talk, **Carnegie Mellon University** **Pittsburgh, PA**  
“Emerging Memory Technologies and the Impact on Computer System Design”
- 4/2010 [11]. Invited talk, **Princeton University** **Princeton, NJ**  
“Emerging 3D and NVM Technologies and the Impact on Computer System Design”
- 1/2010 [12]. Invited talk, **Intel** **Hiilsboro, Oregon**  
“Modeling, Architecture, and Application for Emerging Memory Technologies”
- 1/2010 [13]. Invited talk, **Tsinghua University** **Beijing, China**  
“Modeling, Architecture, and Application for Emerging Memory Technologies”
- 1/2010 [14]. Invited talk, **Intel** **Bengalore, India**  
“Modeling, Architecture, and Application for Emerging Memory Technologies”
- 11/2009 [15]. Invited talk, **Intel** **Hiilsboro, Oregon**  
“Design Methodologies and Architecture for 3D ICs”
- 10/2009 [16]. Invited talk, **IBM T.J. Watson Research Lab** **Yorktown, NY**  
“Design Methodologies and Architecture for 3D ICs”
- 8/2009 [17]. Invited talk, **9th International Forum on Embedded MPSoC and Multicore** **Savannah, GA**  
“Enabling Many-Core Design via 3D Stacking”
- 6/2009 [18]. Invited talk, **National Chiao-Tung University (NCTU)** **HsinChu, Taiwan**  
“Design Methodologies and Architecture for 3D ICs”
- 04/2009 [19]. Invited talk, **COOLCHIPS XII** **Yokohama, Japan**

	“3D Microarchitecture”	
04/2009	[20]. Invited talk, <b>Industrial Technology Research Institute(ITRI)</b> “3D IC Design”	Hsinchu, Taiwan
02/2009	[21]. Invited talk, <b>Semiconductor Research Corporation</b> “3D IC Design and Architecture”	Raleigh, NC
02/2009	[22]. Invited talk, <b>ECE Department, Duke University</b> “New Dimensions in 3D IC Design”	Durham, NC
09/2008	[23]. Invited talk, <b>ECE Department, Univ. of Texas in Austin</b> “Potential and Challenges in 3D IC Design”	Austin, TX
09/2008	[24]. Invited talk, <b>IBM Austin Research Lab</b> “Potential and Challenges in 3D IC Design”	Austin, TX
09/2008	[25]. Invited talk, <b>Freescale</b> “Potential and Challenges in 3D IC Design”	Austin, TX
09/2008	[26]. Invited talk, <b>National Tsinghua University</b> “Reliable Circuits Design on Top of Unreliable Hardware”	Taiwan
07/2008	[27]. Invited talk, <b>National Taiwan University</b> “Design Challenges in Three-dimensional IC Design”	Taiwan
07/2008	[28]. Invited talk, <b>National Tsinghua University</b> “Design Challenges in Three-dimensional IC Design”	Taiwan
06/2008	[29]. Invited talk, <b>Beijing BeiHang University</b> “Potential and Challenges in 3D IC Design”	Beijing, China
06/2008	[30]. Invited talk, <b>Harbin Institute of Technology.</b> “Design Challenges in Three-dimensional IC Design”	China
11/2007	[31]. Invited talk, <b>Qualcomm Inc.</b> “Three-dimensional IC Design”	San Diego, CA
11/2007	[32]. Invited talk, <b>MetaRAM Inc.</b> “Three-dimensional IC Design”	San Jose, CA
10/2007	[33]. Invited talk, <b>Georgia Institute of Technology.</b> “Variation-aware Multi-Processor System-on-Chip (MPSOC) Design”	Atlanta, GA
10/2007	[34]. Invited tutorial, <b>Seagate Technology LLC.</b> “3D IC Design Tutorial”	Bloomington, MN
10/2007	[35]. Invited talk, <b>SEMATECH 3D workshop .</b> “3D Architecture Design”	Albany, New York
09/2007	[36]. Invited talk, <b>KAIST University.</b> “Design Space Explorations for 3D ICs”	Daejeon, Republic of Korea
05/2007	[37]. Invited talk, <b>Honda Research Institute.</b> “Design Automation for Three-dimensional ICs”	Tokyo, Japan
05/2007	[38]. Invited talk, <b>Peking University.</b> “New Dimension for High Performance”	Beijing, China
04/2007	[39]. Invited talk, <b>IMEC (Interuniversity Microelectronics Centre).</b> “The Challenges of Designing 3D Microarchitectures”	Leuven, Belgium
01/2007	[40]. Invited talk, <b>Dagstuhl Seminar on Power-Aware Computing Systems.</b> “Thermal Challenges in 3D Microarchitecture Design”	Dagstuhl, Germany
11/2006	[41]. Invited talk, <b>The 3rd Annual 3-D Architectures Conference.</b> “Design Space Exploration for 3D IC Design”	San Francisco, CA
10/2006	[42]. Invited talk, <b>University of Pittsburgh.</b> “The Challenges of Designing 3D Microarchitectures”	Pittsburgh, PA
08/2006	[43]. Invited talk, <b>Hongkong University of Science and Technology.</b> “3D Microarchitecture Design”	Hong Kong, China
08/2006	[44]. Invited talk, <b>Intel China Research Center.</b> “3D Microarchitecture Design”	Beijing, China

03/2006	[45]. Invited talk, <b>IBM T.J.Watson Research Center.</b> “The Challenges of Designing 3D Microarchitectures”	<b>Yorktown, NY</b>
10/2005	[46]. Invited talk, <b>IBM China Research Lab.</b> “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	<b>Shanghai, China</b>
10/2005	[47]. Invited talk, <b>Peking University.</b> “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	<b>Beijing, China</b>
10/2005	[48]. Invited talk, <b>Shanghai Jiaotong University.</b> “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	<b>Shanghai, China</b>
05/2005	[49]. Invited talk, <b>Syracuse University.</b> “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	<b>Syracuse, NY</b>
10/2005	[50]. Invited talk, <b>University of South Florida.</b> “Thermal-Aware Design Techniques for Nanometer VLSI Chip”	<b>Tempa, FL</b>
10/2004	[51]. Invited talk, <b>IBM Circuit Education Seminar.</b> “Soft Errors: Interactions with Power Optimizations”	

## Service and Activities

### Professional Community

2009-	Committee Member, IEEE Design Automation Technical Committee (DATC).
2007-	Chair of Student Technical Activities on the Technical Activities Board, IEEE Computer Society.

### Editorial

2010-	Associate Editor, ACM Journal of Emerging Technologies in Computer Systems (JETC)
2010-	Associate Editor, IEEE Transactions on CAD (TCAD).
2010-	Associate Editor, IEEE Design and Test of Computers.
2008-	Associate Editor, IET Computers and Digital Techniques (IET CDT).
2007-	Associate Editor, IEEE Transactions on VLSI Systems (TVLSI).
2009	Guest Co-Editor, IEEE Design and Test of Computers, Special Issues on 3D ICs.
2009	Guest co-Editor, IET Computers and Digital Techniques (IET CDT), Special Issues on 3D ICs.
2007	Guest co-Editor, ACM Journal of Emerging Technologies for Computer Systems (JETC), Special Issues on 3D ICs.

### TPC Chair/Co-Chair in Conferences/Workshops:

2013	Technical Program Chair for Asia and South Pacific Design Automation Conference
2012	Technical Program Vice Chair for Asia and South Pacific Design Automation Conference
2011	General Co-Chair for Greatlake Symposium on VLSI (GSVLSI), Laussane, Switzerland
2011	Technical Program Co-Chair for MPSOC Forum, Grenoble, France
2010	General Co-Chair for Workshop on Design for 3D Integration, Laussane, Switzerland
2009	Program Co-Chair for International Symposium on VLSI (ISVLSI), Orlando, Florida
2009	Program Co-chair, First workshop for Three-dimensional Architectures, in conjunction with High Performance Computer Architectures(HPCA)
2008	Program Chair for 3D IC and Architecture Workshop, Hsin Chu, Taiwan.
2009	Program Subcommittee Chair for Emerging Technology Track, and TPC member, Design Automation and Test in Europe(DATE)

### TPC member in Conferences/Workshops:

2008	Program Committee Member, IEEE/ACM Design Automation Conference (DAC)
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2009-2010 Program Committee Member, International Conference on Computer-Aided Design(ICCAD)

2008-2010 Sub-Committee Chair on Eemerging Technology, Design Automation and Test in Europe(DATE)

2008-2011 Program Committee Member, Asia and South Pacific Design Automation Conference (ASP-DAC)

2010 Program Committee Member, IFIP/ACM VLSI-SOC Conference

2010 Student Award Committee Co-Chair, High Performance Computer Architecture (HPCA)

2009,2006 Program Committee Member, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)

2009-2010 Program Committee Member, IEEE/ACM International Conference on Computer Design (ICCD)

2008-2010 Program Committee Member, IEEE/ACM International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)

2008 Program Committee Member, ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES 2008)

2008 Program Committee Member, Workshop on Interaction Between Compilers and Computer Architectures (INTERACT-12)

2008 Program Committee Member, International Conference on VLSI Design (VLSID 2008)

  

2007 Session Chair, International Conference on Computer Aided Design(ICCAD)

2007 Program Committee Member, International Workshop on Trustworthiness, Reliability and Services in Ubiquitous and Sensor Networks (TRUST 2007)

2006-2007 Program Committee Member, International Conference on Communications, Circuits, and Systems

2007-2008 Program Committee Member, Financial Chair (2008), International Symposium on Low Power Electronics and Design

2007-2008 Program Committee Member, IEEE International Symposium on Circuits and Systems (ISCAS 2007, 2008)

2007 Program Committee Member, ACM International Conference on Computing Frontiers (CF 2007)

2007-2008 Program Committee Member, EDAA/PhD Forum, in conjunction with DATE 2007/2008

2006-2009 Program Committee Member, Finance Chair (2008,2009), Greatlake Symposium on VLSI (GLSVLSI)

2006 Program Committee Member, International Conference on Nano-networks (Nano-Net 2006)

2006 Program Committee Member, IFIP International Conference on Embedded and Ubiquitous Computing

2005 Program Committee Member, International Conference on Embedded Software and System (ICESS'05)

2005 Tutorial Chair, ACM Conference on Embedded Software (EMSOFT 2005)

2004-2005 Session Chair, International Conference on Computer Design

2003 Session Chair, International Conference on ASICs

### Services to the University

2007- IEEE Computer Society Advisor, PennState

2007- Student Advisor, Engineering Advising Center, College of Engineering, PennState

2006-07 Ph.D. Candidacy Exam Chair, Computer Science Engineering Dept, PennState

2005-06 Department Colloquium Chair, Computer Science Engineering Dept, PennState

2003-05 Graduate Committee, Computer Science Engineering Dept, PennState