Enabling Power-Efficient Designs With III-V Heterojunction Tunnel FETs

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Why TFET? CMOS Scaling Challenge

- **V\textsubscript{CC} and V\textsubscript{T} (V)**
  - Slowdown of V\textsubscript{CC} scaling
  - Non-Scalability of V\textsubscript{T}

- **Year**
  - 1995 to 2015

- **Delay (us)**

- **Power Density (W/cm\textsuperscript{2})**
  - Active power density
  - Standby leakage power density

- **Gate Length (um)**

**References**

Why TFET? CMOS Scaling Challenge

- Subthreshold Swing (SS), $I_{ON}$, and Leakage $I_{OFF}$

\[
SS = \frac{dV_{GS}}{d(\log_{10} I_{DS})} > 60 \text{mV/Dec}
\]

\[
E_{tot} = I_{Leak} V_{DD} \tau + C_{eff} V_{DD}^2 \alpha
\]

A. M. Ionescu, IEDM short course 2013.

- Due to 60 mV/dec CMOS SS limit, reducing $V_T$ (so as to reduce VDD for lower power) increases the leakage power significantly;
- With a lower SS, Tunnel FETs can operate at a lower VDD and lower power.
Emerging Tunnel FETs (TFETs)

Deway et al., IEDM 11

Mohata et al., VLSI 12

K. Moselund et al., IBM

Xing et al., IEDM 12

Rooyackers et al., IEDM 13

Bijesh R. et al., IEDM 13

A. M. Ionescu, IEDM short course 2013.
III-V GaSb-InAs Heterojunction TFET (HTFET)

- HTFET: High $I_{on}$ and low SS achieved in n- and p- TFET with electrostatic improvement.
- Non-steep subthreshold slope is mainly due to the trap assisted tunneling (TAT) of the source/channel interface states. Further improvement on material interface is required.

V. Narayanan, ISLPED 2013.
III-V GaSb-InAs Heterojunction TFET (HTFET)

HTFET Structure and Operation

- Essentially a gated reverse-biased p-i-n tunnel diode with asymmetrical source/drain doping;
- Band-to-Band tunneling (BTBT) induced from the sub-thermal switching leads to <60mV/dec SS, more abrupt ON-OFF transition compared to CMOS.

Modeling HTFET: Device to Architecture

Full band Atomistic simulation (Purdue Nanohub)

I-V/C-V sweep (experimentally verified)

Verilog-A Device Model

DC Validation

Transient Validation

TCAD Model Calibration

Circuit & Architecture Design

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GaSb-InAs TFET Characteristics

Key Features Observed

- Steep-slope with High $I_{on}$ @ low $V_{CC}$
- High saturated small-signal $R_O$
- Uni-directional Tunneling
- Negative differential resistance (NDR)

H. Liu et al, ISLPED13
GaSb-InAs TFET Characteristics (cont.)

Example of Switch Design Considerations

Type 2. Transmission based Si FinFET DFF

Type 2. Transmission based HTFET DFF

Additional switch for bidirectional conduction
GaSb-InAs TFET Characteristics (cont.)

- Capacitance versus gate voltage
  - Suppressed capacitance (low voltage)
  - Enhanced Miller effect (full voltage)

S. Mookerjea et al., EDL 2009.
H. Liu et al., “Tunnel FET RF rectifier design for energy harvesting applications,” JETCAS 2014
The $g_{m,\text{HTFET}}$ is significantly larger than $g_{m,\text{CMOS}}$ at a low current. With larger small-signal $R_o$, the intrinsic gain is further improved. HTFET has >300 GHz while CMOS shows higher $f_T$ at a higher current. The peak $f_T$ at a lower current makes HTFET attractive for low-power applications.

B. Sedighi et al., “Analog Circuit Design Using Tunnel-FETs,” TCAS-I, to be published
Flicker noise is based on carrier number fluctuation

\[
\frac{S_{id}(f)}{I_D^2} = \left( \frac{2}{F} + \frac{B}{F^2} \right)^2 \frac{q^2 N_t (E_{fn})}{\varepsilon_{ox}^2 WL'\alpha f}
\]

The shot noise is modeled similar to tunnel diode

\[
i_{shot}^2 = 2qI_D\Gamma
\]

The thermal noise model is similar to the Si-FinFET thermal model

\[
i_{n,thermal}^2 = 4kT\gamma g_m\Delta f
\]

Tunnel FET Flicker Noise (interface traps)

TFET flicker noise highly depends on the spreading of the tunneled carriers in the channel (L’), which is independent of the channel-length (L_g).

TFET Drain Current Flicker Noise Power

Analytical Model:

\[
\frac{S_{id}(f)}{I_D^2} = \left( \frac{2}{F} + B \frac{B}{F^2} \right)^2 \frac{q^2 N_t(E_{fn})}{\varepsilon_{ox}^2 WL' \alpha f}
\]

B is Kane’s model parameter, f is frequency, W is the device width, \( \alpha \) is the attenuation factor, \( N_t \) is the interface trap density, F is the electrical field.

Overall Electrical Noise: HTFETs vs Si FinFETs

- A larger noise of HTFET at low $I_D$ is due to the smaller tunneling length of carriers.
- HTFET noise reduces faster is due to faster carrier density increase.
- Competitive device noise
- Lower input-referred noise for HTFET with high gains

Standard Cell Library Design Flow Enables quick evaluation of large-scale digital circuits.

- **Behavioral Verilog System Designs** (i.e., Arithmetic logics, Accelerators, Registers, etc.)
- **TFET Cell Library**
- **TFET Verilog-A models**
- **Modification of design for cells**
- **Spice Simulations**
- **Technology library database (*.db)**
- **Look up tables**
- **Optimization (timing and power)**
- **Generate Power and timing tables**
- **Architecture library database**
- **Architecture Evaluation**
  - Existing Core Models (Ivybridge, UltraSparc)
  - Architecture Simulation (Sniper, Gem5, GEMS)
  - Timing + Power with Wire Models (McPAT)
- **System Evaluation**

**Device:** 20nm TFET [1]

**Modification of circuit designs:**
Due to uni-directional conduction of TFET, some circuits (i.e., MUX, DFF, Etc.) have been modified to retain the discharge path.

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*K. Swaminathan et al, DAC2014.*
Potential Design Space By TFETs

Architectural Innovation

- Heterogeneous multicore
- Simple/complex pipelined processors
- Thermal-aware design
- Domain-specific accelerators

- Ultra Low power Energy Harvesting, Wearable Computing
- Low power/Embedded Systems Mobile/Tablet Processors
- High Performance Computing
- 3D Stacking

Ultra Low power Energy Harvesting, Wearable Computing

Low power/Embedded Systems Mobile/Tablet Processors

High Performance Computing

3D Stacking

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Digital Benchmarking: Tunnel FET vs. CMOS

HTFET accelerators outperform a range of CMOS designs
- 6X energy reduction over iso-voltage CMOS design
- 30% less energy than iso-performance CMOS design

\[ \sum_{i=1}^{64} (P_i - Q_i)^2 \]

CMOS-TFET Heterogeneous Multicores

- CMOS has higher peak performance @ high VDD
- TFET Processor is “cooler”
- Maximize performance using CMOS-TFET heterogeneous multicores

TFET in 3D Stacked Multicore Systems

- Relative performance of a 64-core CMOS and HTFET 3D stacked system, normalized to a single core CMOS performance.
- 18% speedup obtained by using HTFET cores over CMOS cores.
- Heterogeneous 3D stacked CMOS-HTFET multicore system can result in even higher speedups

Emerging System Design Using HTFET

Increase the harvested power

- PSU: TFET AC-DC Rectifier (H. Liu et al., ISLPED’13, JETCAS’14)
  - High sensitivity and power conversion efficiency to weak RF input (> 90% @ -42 dBm input).
  - 0.4uW output @ -33dBm RF input

UCSD: TFET RF circuits (VCO/Mixer/LNA), Parasitic Analysis; PSU: Current-mode transmitter (W. Y. Tsai, et al, VLSI-SOC’14)

- Ultra-low power, energy efficient digital processing

Reduce the power consumption

- PSU 6-bit 10MS/s SAR ADC (M. S. Kim, et al, TED to be published)
  - Low-power, low-voltages.
  - At 0.3 V supply voltage, power consumption of 0.25 µW, SNDR of 35dB (ENOB=5.6b), 0.51 fJ/Step.

- PSU Neural Amplifier (H. Liu, et al, ISLPED’14)
  - 0.5 V, 5nW per channel.
  - 39 dB voltage gain, 2kHz bandwidth
  - Noise efficiency factor: 0.64

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Steep-Slope Features: Lower threshold voltage and resistive loss
Uni-directional Conduction: Lower leakage current from output to input

H. Liu et al., “Tunnel FET RF rectifier design for energy harvesting applications,” JETCAS 2014
High-Efficiency HTFET Switched-Capacitor DC-DC Converter

- Steep-Slope Features
  - Lower threshold voltage and resistive loss
- Uni-directional Current Conduction
  - Lower leakage current from output to input
  - Lower power by simplified phase generator
  - Novel topology of doubling output gate control for lower resistive loss


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**Low-Noise HTFET Neural Amplifier**

- **Motivation: Low-Noise Amplifier for Neural Signal Recording**

  - Key Design Points:
    - ✓ High gain
    - ✓ Low input-referred noise
    - ✓ Low power


- **Steep-Slope Tunnel FET Neural Amplifier**

Low-Power HTFET SAR ADC

SAR: most digitized

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Graphs and charts showing ENOBs, SNDR, and FoM as functions of input frequencies and supply voltages for HTFET and Si FinFET ADCs.

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M. Kim., et al, TED 2014
Promising “Beyond-CMOS” candidate
- Technology scaling has forced us to plan for the Post-CMOS era
- HTFET can complement, or replace CMOS enabling new design spaces

Key devices features
- Steep-slope switching, Uni-directional current conduction,
- High small-signal $R_O$ in saturation, high $g_m/I_{ds}$, high $f_T$ at low current,
- Negative differential resistance (NDR), Competitive noise performance

Parallelism and 3D design further improves performance

Beneficial device features in analog/RF circuits design
- Amplifier
- Current-mode logic
- RF transceiver
- Rectifier
- DC-DC converter
- A/D converter
- Energy harvesting
- Power management

Future work
- Device fabrication, modeling, circuit & system design and evaluations
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