

Xiaoxia Wu

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Education

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|----------------|--|----------------------------|
| 2005 - present | Pennsylvania State University
Ph.D. candidate in Computer Science and Engineering, Advisor: Prof. Yuan Xie | University Park, PA |
| 2005 | Tsinghua University
M.S. in Electrical Engineering | Beijing, P.R.China |
| 2002 | Tsinghua University
B.S. in Electronic Engineering | Beijing, P.R.China |

Research Interests

Low power and reliable VLSI Design, Three-dimensional (3D) IC Design, VLSI EDA tools, and Computer Architecture.

Research Experience

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| 2009.5-2009.8 | Electrical Characterization for Inter-tier connections in 3D
Evaluate the resistance, capacitance, and inductance of inter-tier connections including TSVs and micro-bumps in 3D considering process variations. Examine the delay variations and deliver the Hspice model of 3D inter-tier connections to design flow team for 3D IC design. Timing corner analysis for 3D stacking: 1) library characterization using SiliconSmart; 2) timing analysis of 3D stacking at circuit level by simulating ring oscillators with different stages and architectural level by analyzing ARM cores at different corners. | Qualcomm |
| 2008.7-2008.12 | Hybrid Cache Architecture
Implemented a preliminary cycle-accurate Cache power model in Mambo simulator. Hybrid cache architecture design: 1) Evaluate the performance and power consumption of different memory technologies (SRAM, eDRAM, MRAM and PRAM); 2) Evaluate two types of hybrid cache architectures: inter-cache-Level HCA (LHCA), in which the levels in a cache hierarchy can be made of disparate memory technologies; and intra-cache-level or cache-Region-based HCA (RHCA), where a single level of cache can be partitioned into multiple regions, each of a different memory technology; 3) Explored the potential of hardware support for intra-cache data movement and power consumption management within HCA caches; 4) Evaluate 3D hybrid cache design. Preliminary results are published in ISCA 2009([C1]) and DATE 2009 ([C2]), and submitted to TACO 2009 ([J1]). | IBM Austin Research Lab |
| 2007-present | Circuit and Micro-architecture Evaluation of Magnetic RAM (MRAM) stacking Microprocessor using 3D technology
Sponsored by Seagate LLC, we collaborate with Seagate's MRAM research group, evaluate the benefits of area, power, and performance for MRAM as a universal memory replacement, develop MRAM based cache performance/energy model based on existing CACTI software, and evaluate the architectural benefits of MRAM-based cache and main memory stacking atop a microprocessor. This work is published in DAC 2008([C4]). | Penn State University |
| 2006-2008 | Three-dimensional (3D) IC Design Flow Integration
Sponsored by IBM as a subcontractor on the DARPA project "Technology and Design Infrastructure for High Performance Three-Dimensional ICs". We collaborate with IBM Yorktown and UCLA, work on the development of OpenAccess based 3D IC design flow using IBM internal tools and commercial EDA tools. Specifically, we develop 3D RC extraction using OpenAccess database, and timing interface between OpenAccess and IBM EinsTimer for 3D thermal-aware timing-driven placement, and 3D DRC and LVS verification using Cadence design kit. | Penn State University |
| 2007-present | Three-dimensional (3D) ICs Testing
Collaborate with IBM testing group, we study various 3D IC testing issues. Develop 3D scan chain design methods using Genetic Algorithm and Integer Linear Programming optimization using Randomized Rounding for single scan chain ordering and multiple scan chain partitioning. Study 3D Test Access Mechanism (TAM) for core-based 3D System-on-chip (SOC) design. Preliminary results are published in ICCD 2007([C8]), ITSW 2008([C5]), JETC 2009([J3]), and ICCD 2008([C3]), and submitted to TCAD 2009 ([J2]). | Penn State University |
| 2005-2006 | Process Variation-aware High-level Synthesis | Penn State University |

High-level synthesis considering delay and power variation. Parametric yield optimization with joint design time and post silicon tuning approach. The project results in one **Best Paper Nomination** in ICCAD 2006([C11]) and one **Best Paper Award** in ASP-DAC 2008([C6]).

- 2005 **Analysis of Subthreshold FinFET circuits for ultra-low power design** Penn State University
Compared energy, optimal point, and reliability results to bulk CMOS technology
Analysis FinFET circuit in subthreshold region for ultra-low power design using HSPICE
- 2003 **M.S. Thesis: The Implementation of USB device Interface IP Core** Tsinghua University
Realized the function of USB 1.1 device interface using verilog HDL
Tested the interface using FPGA-base board by implementing a USB mouse
- 2003 **Contactless IC Card Design.** Beijing, P.R.China
Co-op in Beijing Tsinghua Tongfang Microelectronics Co., Ltd. design and implement a contactless IC card.
Designed the testbench and test vectors for the IC card
- 2002 **B.S. Thesis: The Implementation of IC database** Beijing, P.R.China
Designed an 8-bit MCU with verilog HDL based on a VHDL version
Realized the encryption and protection of the GDSII file. Import it into an IC database as an exemplification
- 2001 **Design a Full Custom Physical Layout for a Frequency Synthesizer** Beijing, P.R.China
Designed a full custom physical layout for the dual modulus prescaler in a frequency synthesizer

Awards and Honors

- 2009 CSE Department Research Assistant Award
2008 ASP-DAC 2008 Best Paper Award
2007 Women in Engineering Program Scholarship, Penn State
2006 ICCAD 2006 Best Paper Award Nomination
2006 ACM-W scholarship, Association for Computing Machinery
2006 Amelia C.Barnes,Andrew Barnes and Kevin Barnes Scholarship, Penn State
2005 Max and Joan Schlienger Graduate Scholarship in Engineering, Penn State
2001 Weilun Fund Student Scholarship, Tsinghua University
1998 The outstanding student honor of Hunan Province

Journal Publications

- [J1]. Xiaoxia Wu, Jian Li, Lixin Zhang, Evan Speight, Ram Rajamony, Yuan Xie. "Design Exploration of Hybrid Caches with Disparate Memory Technologies." *Submitted to ACM Transactions on Architecture and Code Optimization (TACO), 2009.*
- [J2]. Xiaoxia Wu, Yibo Chen, Krishnendu Chakrabarty, Yuan Xie. "Test-Access Mechanism Optimization for Core-Based Three-Dimensional SOCs." *Submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2009.*
- [J3]. Xiaoxia Wu, Paul Falkenstern, Krishnendu Chakrabarty, Yuan Xie. "Scan-Chain Design and Optimization for Three-Dimensional Integrated Circuits." *ACM Journal on Emerging Technologies in Computing systems (JETC), 5, 2, Article 9, 2009.*
- [J4]. Feng Wang, Mike Debole, Xiaoxia Wu, Yuan Xie, N. Vijaykrishnan, M. J. Irwin. "On-chip Bus Thermal Analysis and Optimization." *IEEE Computer Design and Test, 2007.*
- [J5]. Xiaoxia Wu, Ge Yuanqing. "The implementation of USB device interface IP Core." *Microelectronics and Computer, 2005.*

Conference Publications

- [C1]. Xiaoxia Wu, Jian Li, Lixin Zhang, Evan Speight, Ram Rajamony, Yuan Xie. "Hybrid Cache Architecture with Disparate Memory Technologies." *International Symposium on Computer Architecture (ISCA), 2009.*
- [C2]. Xiaoxia Wu, Jian Li, Lixin Zhang, Even Speight, Yuan Xie. "Power and Performance of Read-Write Aware Hybrid Caches with Non-volatile Memories." *Design, Automation and Test in Europe (DATE), 2009.*
- [C3]. Xiaoxia Wu, Yibo Chen, K. Chakrabarty, Yuan Xie. "Test-Access Mechanism Optimization for Core-Based Three-Dimensional SOCs." *International Conference on Computer Design (ICCD), 2008.*
- [C4]. Xiangyu Dong, Xiaoxia Wu, Guangyu Sun, Helen Li, Yiran Chen, Yuan Xie. "Circuit and Mircoarchitecture Evaluation of 3D Magnetic RAM (MRAM) Stacking Microprocessor." *Design Automation Conference (DAC), 2008.*

- [C5]. **Xiaoxia Wu**, Krishnendu Chakrabarty, Yuan Xie. “Scan Chain Design and Optimization for Three-dimensional(3D) ICs.” *International Test Synthesis Workshop, 2008*.
- [C6]. Feng Wang, **Xiaoxia Wu**, Yuan Xie. “Variability-Driven Module Selection with Joint Design Time Optimization and Post-Silicon Tuning.” *Proceedings of Asia-South Pacific Design Automation Conference (ASP-DAC)*, Jan. 2008. **Best Paper Award (out of 350 submissions)**.
- [C7]. Feng Wang, C. Nicopoulos, **Xiaoxia Wu**, Yuan Xie, N. Vijaykrishnan. “Variation-aware Task Allocation and Scheduling for MPSoC.” *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp. 138-149, Nov. 2007.
- [C8]. **Xiaoxia Wu**, Paul Falkenstern, and Yuan Xie. “Scan Chain Design for Three-dimensional(3D) ICs.” *Proceedings of International Conference on Computer Design (ICCD)*, pp.208-214, Oct. 2007.
- [C9]. **Xiaoxia Wu**, Paul Falkenstern, and Yuan Xie. “Design Automation Challenges for 3D ICs.” *The seventh annual Emerging Information Technology Conference, 2007*.
- [C10]. **Xiaoxia Wu**, Feng Wang, and Yuan Xie. “Analysis of Subthreshold Finfet Circuit for Ultra-low Power Design.” *Proceedings of IEEE International System-on-Chip Conference (SOCC)*, pp. 91-93, Sept. 2006.
- [C11]. Wei-lun Hung, **Xiaoxia Wu**, Yuan Xie. “Guaranteeing Performance Yield in High-Level Synthesis.” *Proceedings of International Conference on Computer Aided Design (ICCAD)*, pp.303-309, Nov. 2006. **Best Paper Nomination (8 out of 537 submissions)**.

Patent

Xiaoxia Wu, Jian Li, Ram Rajamony, Evan Speight, and Lixin Zhang. “Improved Non-Uniform Cache Architecture (NUCA)”. United States Patent, file pending, November 2008.

Computer Skills

Programming C/C++, Verilog HDL, VHDL, SKILL, Assembling language

Tools SimpleScalar, Simics, CACTI,
Synopsys, Cadence ICFB, OpenAccess, Hspice, Protel, Active HDL, Modelsim, Synplify, Quartus

Teaching Experience

Fall 2009 Instructor **CSE 331** *Computer Organization and Design*

Spring 2007 Teaching assistant **CSE 477** *VLSI Digital Circuit Design*

Fall 2006 Teaching assistant **IST 220** *Communication and Network*

Fall 2006 Teaching assistant **IST 402** *Computer Security*

Spring 2006 Teaching assistant **CSE 331** *Computer Organization and Design*

Fall 2005 Teaching assistant **CSE 471** *Logic design of digital systems*