

Tutorial Outline

8:30 - 8:45	Introduction and motivation
8:45 - 9:05	Sources of power in CMOS designs
9:05 - 9:30	Power analysis tools and techniques
9:30 - 10:30	Gate & functional unit design issues & techniques
10:30 - 10:50	BREAK
10:50 - 12:15	Architectural level issues and techniques
12:15 - 1:30	LUNCH
1:30 - 2:30	Low power memory system design
2:30 - 3:30	Software level issues and techniques
3:30 - 3:50	BREAK
3:50 - 4:30	Software level issues and techniques, con't
4:30 - 4:45	Future challenges

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Future Challenges

- Controlling growth in subthreshold **leakage currents** due to lower supply voltages and, thus, lower threshold voltages
- Maintaining a near **constant supply voltage** when delivering (on average) hundreds of amps with a variation in supply current of up to hundreds of amps
- Handling **power surges** when large portions of the chip “wake up”

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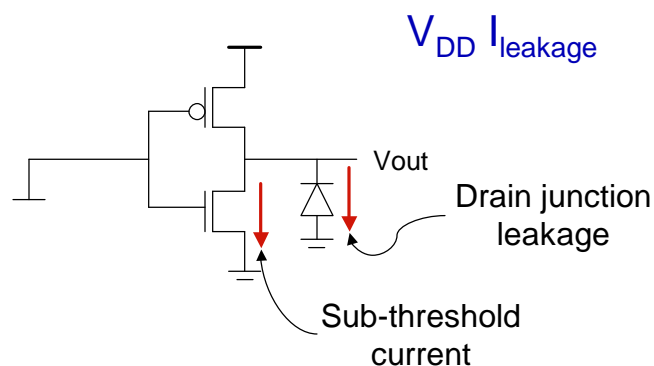
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Basic Principles of Low Power Design

$$P = C_L V_{DD}^2 f_{0 \rightarrow 1} + t_{sc} V_{DD} I_{peak} f_{0 \rightarrow 1} + V_{DD} I_{leakage}$$

- Reduce switching (supply) voltage
 - » quadratic effect -> dramatic savings
 - » negative effect on performance
- Reduce capacitance
- Reduce switching frequency
 - » switching activity
 - » clock rate
- Reduce glitching
- Reduce short circuit currents (slope engineering)
- Reduce leakage currents

Leakage Currents



Sub-threshold current is the dominant factor.
Increases **exponentially** with temperature!

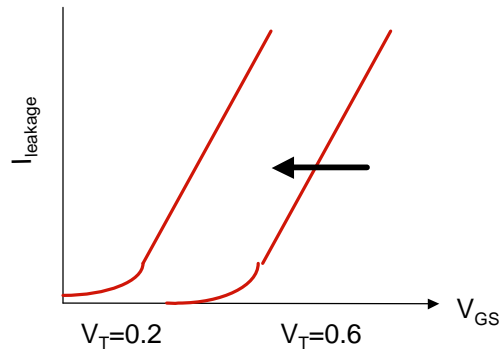
Supply Voltage Scaling

Year	1999	2002	2005	2008	2011	2014
Feature size (nm)	180	130	100	70	50	35
Logic trans/cm ²	6.2M	18M	39M	84M	180M	390M
Cost/trans (mc)	1.735	.580	.255	.110	.049	.022
#pads/chip	1867	2553	3492	4776	6532	8935
Clock (MHz)	1250	2100	3500	6000	10000	16900
Chip size (mm ²)	340	430	520	620	750	900
Wiring levels	6-7	7	7-8	8-9	9	10
Power supply (V)	1.8	1.5	1.2	0.9	0.6	0.5
High-perf pow (W)	90	130	160	170	175	183
Battery pow (W)	1.4	2	2.4	2.8	3.2	3.7

Leakage Currents

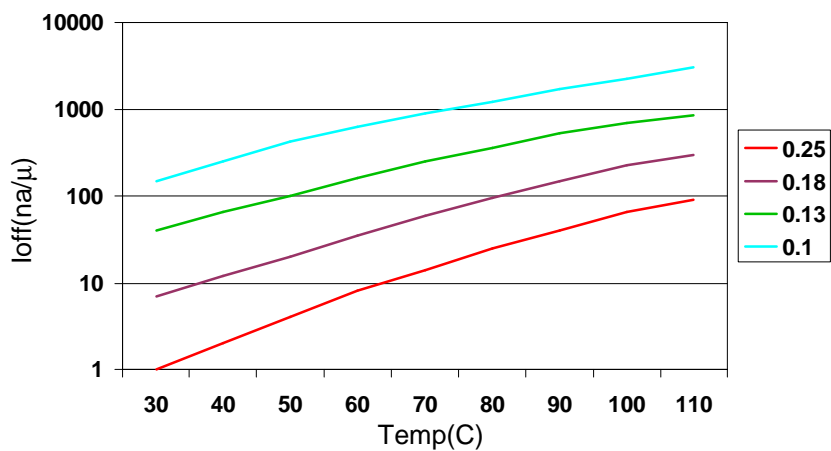
- Decreasing supply voltage means that threshold voltages will decrease to
 - » help maintain signal integrity
 - » buy back loss in speed
- But decreasing the threshold voltage means an increase in leakage current
 - » increase in sub-threshold current
 - » leakage currents **increase exponentially** with temperature!

Sub-Threshold in MOS



Continued scaling of supply voltage will make subthreshold conduction a dominate source of power dissipation.

Projected Off Currents



From De, 1999

Controlling Leakage Currents

- Transistor sizing
 - » leakage current increases with decreasing V_T and **channel length** while speed increases
- Transistor stacking
- Multiple threshold voltages
 - » use lower threshold devices only where speed is important
- Limit leakage through dynamic control (threshold is lower when circuit is active, elevated when idle)
 - » substrate biasing
- New technologies
 - » SOI

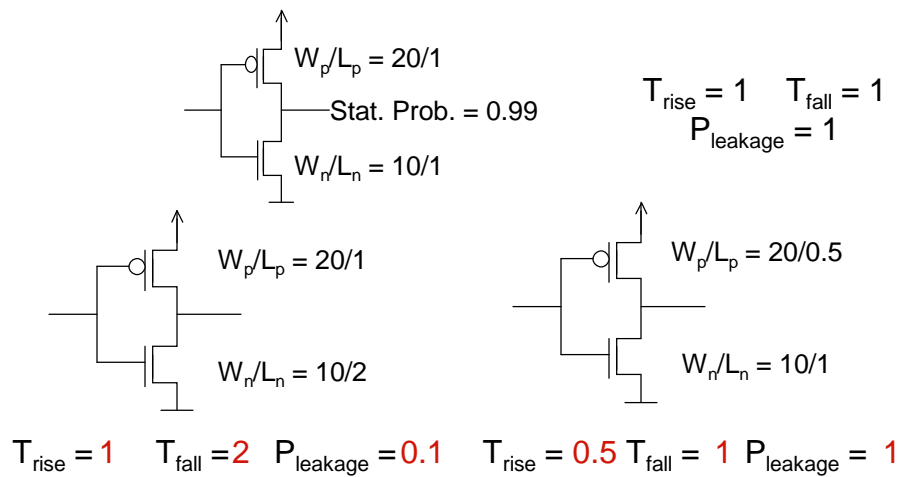
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Transistor Sizing for Leakage

Leakage power depends on logic state

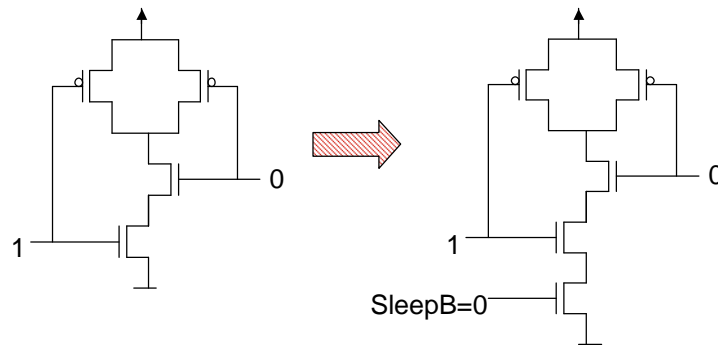


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Transistor Stacking



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Dual Threshold Voltages

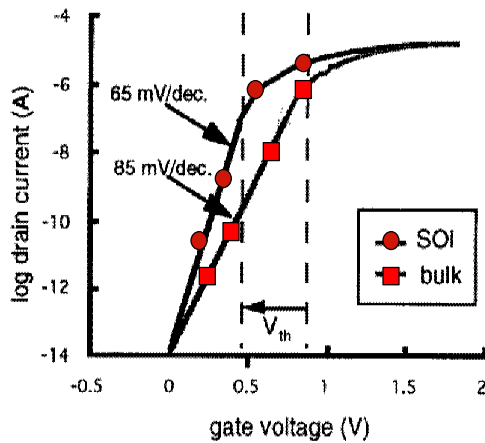
- Use two V_T 's (e.g., 0.6V and 0.3V for $V_{DD} = 2.5V$)
 - » use the **lower** threshold for gates on the critical path
 - » use the **higher** threshold for gates off the critical path
- Improves performance without an increase in power
- Cons
 - » increased fabrication complexity
 - » increased design time
 - » beware of increased leakage in low V_T portion of the circuit - could end up with increased power!

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SOI



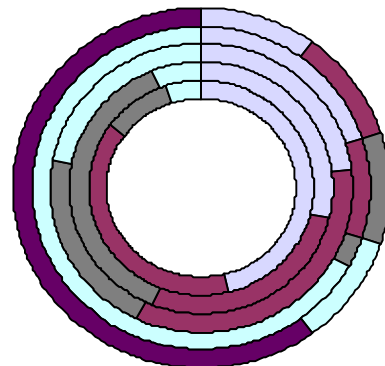
- Lower subthreshold slopes indicates sharp transition from “off” to “on”- **important for low V_{dd} device.**
- Junction area is very small - decrease in device capacitance and leakage current
- SOI devices can operate with lower threshold voltage than CMOS devices.

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Processor Power Budgets



- Clock
- Datapath
- Memory
- I/O (pads)
- RF (comm)

Inner circle: low end embedded microprocessor
 Next circle: high end CPU with on-chip cache
 Next circle: MPEG2 decoder ASIC
 Outer circle: ATM switch ASIC
 New outer circle: Wireless PDA

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Key References

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