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Nationality: Indian
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Education

Fall 2005 – Present. Ph.D candidate, Computer Science and Engineering.
Pennsylvania State University, University Park.
Advisors: Dr. Anand Sivasubramaniam, Dr. Vijaykrishnan Narayanan

B. Engg in Computer Science and Engineering, July 2004
Sri Venkateswara College of Engg, University of Madras, Chennai, TN, India
Advisor: Prof. Nagarajan Venkateswaran

Research Interests

Computer Architecture, single and multicores
Hardware Fault Tolerance and Reliability
On-chip Interconnection networks
Hybrid on-chip memory design using emerging memory technologies
Cache coherency protocols in many-core era
Transactional Memory

Work Experience

1. Co-op with Fault Aware Computing Technology (FACT) group in Intel, MA in 2007.
Manager: Shubu Mukherjee, Mentor: Arijit Biswas
2. Co-op with Research and Advanced Development Labs (RADL) in AMD, WA in 2010.
Manager: Andrew Kegel, Mentor: Jaewoong Chung
3. Spring 2006 – 2008, Teaching Assistant. Courses include,
 - Introductory System Programming
 - Intermediate C++ Programming
 - Introduction to Computer Architecture
4. Summer 2008 – Present, Research Assistant

Technical Proficiency

Simulators: SimpleScalar, GEMS full-system simulator
Languages: C++/C (with STL), Visual Basic, JAVA, PERL
Databases: SQL, Oracle, MS Access
OS: Unix, Linux, Solaris
HDLs: Verilog HDL, VHDL
Software: Adobe Photoshop, HTML, Sigma Plot, Matlab, Latex

Courses

Operating Systems Design, Programming Language Concepts, Self-* Systems, Computer Networks, Virtual Machines, Interconnection networks (related to NOCs), Multiprocessor Architecture, Compiler Construction, Topics in Computer Architecture, Storage Systems

Graduate Publications

1. "Characterizing the Soft Error Vulnerability of Multicores running Multithreaded Applications". **Niranjan Soundararajan**, Vijay Narayanan, Anand Sivasubramaniam. To Appear as poster paper in the Proceedings of **ACM SIGMETRICS 2010**, June 2010.
2. "Optimizing Power and Performance for Reliable On-Chip Networks". A. Yanamandra, S. Eachempati, **Niranjan Soundararajan**, Vijay Narayanan, Mary Jane Irwin, R. Krishnan. Proceedings of 15th Asia and South Pacific Design Automation Conference (**ASP-DAC 2010**), January 2010
3. "Quantized AVF: A Means of Capturing Vulnerability Variations over Small Windows of Time". Arijit Biswas, **Niranjan Soundararajan**, Shubu Mukherjee, Sudhanva Gurusurthi. IEEE Workshop on System Effects of Logic Soft Errors (**SELSE-5**), March 2009
4. "Impact of DVFS on the architectural vulnerability of GALS architectures". **Niranjan Soundararajan**, Vijay Narayanan, Anand Sivasubramaniam. *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED)*, August 2008
5. "Analysis and solutions to Issue Queue Process Variations". **Niranjan Soundararajan**, Aditya Yanamandra, Chrysostomos Nicopolous, Vijay Narayanan, Anand Sivasubramaniam, Mary Irwin. *Proceedings of the 38th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN-DCCS)*, June 2008
6. "Mechanisms for bounding vulnerabilities of processor structures". **Niranjan Soundararajan**, Angshuman Parashar, Anand Sivasubramaniam. *Proceedings of the 34th Annual International Symposium on Computer Architecture (ISCA)*, June 2007

Under-Graduate Publications

7. "PASCOM: Power Model for Supercomputers". A. Shriraman, N. Venkateswaran, **Niranjan Soundararajan**. ARCS 2006
8. "Fault Tolerant Memory In Processor - SuperComputer On a Chip". **Niranjan Soundararajan**, Arrvinth Shriraman. *Poster Presentation: MAPLD International Conference, 2005*
9. "Memory In Processor SuperComputer On a Chip - Processor Design and Execution Semantics for Massive On-Chip Parallelism". N.Venkateswaran, Arrvinth Shriraman, **Niranjan Soundararajan**, *Workshop on Massively Parallel Processing (WMPP) held with IPDPS 2005*
10. "Memory In Processor: A Novel Design Paradigm for Supercomputing Architectures". N. Venkateswaran, A. Krishnan, A. Shriraman, **S.Niranjan Kumar**, S. Srinivas, *ACM SIGARCH Comp. Arch News, June 2004*
11. "The MIP Project: Evolution of a Novel Supercomputer Architecture". N. Venkateswaran, Arrvinth Shriraman, Aditya Krishnan, **S.Niranjan Kumar**, S. Srinivas. *Memory performance: DEALING with Applications (MEDEA) Systems and Arch. Workshop in conjunction with PACT 2003*

Patents

- "Detecting Architectural Vulnerability of Processor Structures", Applied April 2008.
- Co-Invented with Arijit Biswas, Shubu Mukherjee – Intel Corp.

Miscellaneous

- Won Intel travel scholarship for attending HiPC 2003.
Reviewed papers for ISCA, MICRO, HPCA, TCAD and other major conferences and journals.

Research Summary

My doctoral work involves developing architectural-level techniques to address the increasing impact of different reliability phenomena in performance-critical pipeline components in single and multicores. Transistor failures occur early in their lifetime due to manufacturing defects or due to wearout towards the end of lifetime or random faults occur in between each having a different cause and, importantly, a differing impact on the underlying hardware. Given the increase failure rates, it is critical to provide solutions addressing their impact. A low performance overhead is equally critical to make adoption of these techniques viable for products available in the market.

My initial work, **ISCA 2007**, looked at developing soft error protection mechanisms aware of application requirements. Solutions proposed till then were agnostic to application needs, their protection levels being either an overkill affecting performance or not meeting reliability requirements. By catering to application-specific requirements, this technique meets reliability demands while minimizing performance losses. Related to this work my internship, with the FACT group at Intel, involved developing a runtime soft error analysis infrastructure to enable and disable protection mechanisms, **SELSE 2009**.

Multicores offer the flexibility to run applications in different configurations, in terms of the number of application threads and the number of cores on which the threads run. I explored the impact on soft error vulnerability of a multicore platform when running multi-threaded applications. The analysis revealed that making the underlying platform aware of the reliability impact across configurations even removes the need for protection mechanisms to attain specific reliability levels. I propose runtime schemes which provide considerably better performance-reliability tradeoffs over any statically chosen configuration. A part of this work will appear as a poster paper in **SIGMETRICS 2010**.

Globally Asynchronous Locally Synchronous (GALS) platforms are preferred since they reduce clock power consumption. Dynamic Voltage Frequency Scaling (DVFS) algorithms in these environments were studied from a performance per watt basis ignoring their reliability impact. Lower VF levels meant reduced operating voltage levels and slower operation, increasing the soft error vulnerability. I showed, **ISLPED 2008**, that different DVFS algorithms have varying impact on soft error vulnerability and a Non-DVFS platform offered better tradeoffs when considering reliability with performance and power.

Besides studying transient faults, I also have looked at hard faults due to Process Variations (PV) resulting from manufacturing defects and those occurring due to wearout in different issue queue designs. PV which affects the operating speeds of transistors are extremely detrimental, especially in the issue queue which has a big role in determining the both the operating frequency and overall throughput of the system. This work involved developing solutions that minimize the usage of slow entries in the issue queue. Given its performance-critical nature, the PV-aware issue queue design, **DSN 2008**, was very effective in reducing pipeline stalls and operating the system very close to its maximum throughput.

Transistors wearout during their lifetime gradually leading to slower circuits. Given the multi-dimensional requirements, performance and power, on current day circuits the operating lifetime of devices are decreasing. Two specific phenomena of concern are Negative Bias Temperature Instability (NBTI) and Hot Carrier Effects (HCE). To reduce wearout due to NBTI and HCE in the issue queue, I propose mechanisms that reduce the variation in switching activity across entries significantly decreasing the worst case read delay degradation. This work is currently under review.

While reliability has been the main focus of my Ph.d, I have/am explored other areas of architectural research as well. I have studied on-chip interconnection networks and have been part of a project developing low overhead reliable on-chip interconnection networks. Currently I am part of projects that look at adapting hybrid memory technologies (MRAM, PRAM) in low power reliable multicores.