We propose a Refresh Enabled Video Analytics (REVA) system that reduces refresh power by using semantic knowledge to modulate the refresh periods at a row-level granularity.

**Motivation**

In a purely streaming embedded system refresh can be turned off completely. However, there can be instances when a burst of RoIs is generated and the pipeline cannot sustain a high throughput. RoIs will then be needed to be buffered. In action recognition consecutive RoIs are used for classification.

We evaluated different configurations of action recognition on the Weizmann dataset. The results indicate that a purely streaming (no overlap of video segments) configuration affects accuracy considerably (by around 10%).

**Experimental Setup**

We consider a detection-object recognition-action recognition pipeline for visual scene understanding.

We used Vivado to generate memory traces based on our accelerator parameters.

These traces act as input to DRAMSim2 to enable power modeling.

Our evaluations were on a 8 Gb single rank DDR3-1600 device.

**Results**

We compare REVA with state-of-the-art architectures like Flikker. Other refresh related work includes RAIDR and Elastic Refresh but is orthogonal to our approach.

REVA is dynamically capable of changing the refresh value of an RoI, by simply modifying the refresh period in the corresponding RAT entry. This avoids any additional writes needed to re-write the RoI into frequently refreshed memory.

The expected gains from REVA’s finer grained approach always provide at least as much power savings as Flikker while being feasible for a larger set of tasks.

**Conclusions**

We demonstrate a Refresh Enabled Video Analytics system, which is tuned to optimize energy utilization of the memory by exploiting data characteristics in vision-based applications. We show that depending on the RoI stored in memory, the need for refresh varies from row to row across each memory bank. By adjusting refresh rates selectively depending on the need for re-use of different RoIs, we demonstrate 88% improvement in refresh power and 15% improvement in overall power over existing DRAM schemes.

**References**


