Mixed signal systems and integrated circuits

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3. ADC

- Dynamic performances in ADC
- ADC architectures
  - Integrating ADC
  - Successive approximation ADC
  - Flash ADC
  - Folding ADC
  - Two step parallel ADC
  - Interpolating ADC
- Design of pipeline ADC
- Basic circuit blocks for ADCs
  - Operational amplifier
  - Sample and hold switches
  - Comparators
  - Offset cancel circuits
- Implementation & design of high performance A/D and D/A converters
- Design challenges
Basic functions in ADC

Sampling: Sampling the analog signal with accurate timing.
Quantization: Express the converted data with certain accuracy.
Static performance

INL and DNL are the major static performances of ADC and DAC.

INL: Integrated Non-Linearity
DNL: Differential Non-Linearity
Quantization noise

Quantization causes noise

\[ P_n = \int_{-\Delta/2}^{\Delta/2} e^2 P(e) de = \int_{-\Delta/2}^{\Delta/2} e^2 \frac{1}{\Delta} de = \frac{\Delta^2}{12} \]

\[ \therefore P(e) = \begin{cases} \frac{1}{\Delta} & |e| < \frac{\Delta}{2} \\ 0, \text{all other } e \end{cases} \]

Higher SNR needs higher resolution

\[ P_s = \frac{(\Delta \cdot 2^{N-1})^2}{2} \]

\[ SNR = \frac{P_s}{P_n} = \frac{(\Delta \cdot 2^{N-1})^2}{2} \cdot \frac{12}{\Delta^2} = 1.5 \cdot 2^{2N} \]

\[ SNR_{dB} = 10 \log \left( \frac{P_s}{P_n} \right) = 6.02 \cdot N + 1.76 \]
Dynamic performance

Dynamic performance indicates the ratio between signal and noise or distortions. We should use suitable terms for the kind of applications.

\[ SNR = 10 \log \frac{\text{Signal power}}{\text{Total noise + floor power}} \]

\[ SFDR = 10 \log \frac{\text{Signal power}}{\text{Largest spurious power}} \]

\[ THD = 10 \log \frac{\text{Total harmonic distortion power}}{\text{Signal power}} \]

\[ SNDR = 10 \log \frac{\text{Signal power}}{\text{Noise and distortion power}} \]

\[ ENOB = \frac{SNDR - 1.76}{6.02} \]
BER requirement

The lower bit error rate requires the higher ADC/DAC resolution. Resolution (quantization noise) affects BER.

DAC requirement for QAM

ADC requirement for digital read-channel
Input signal level

SNR decreases with decreasing the input signal level. This is because the quantization noise is same, but the input signal is small.

1) No AGC: Lower SNR

2) Use AGC: Higher SNR

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![Graph showing SNR vs. input signal level](image)

**图 4-7 入力信号レベルとSNR**

Input signal level (dB)

<table>
<thead>
<tr>
<th>Input signal level (dB)</th>
<th>50</th>
<th>40</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>fin=0, 99MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fin=4, 99MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fs=20MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8-bit theoretical line
Performances and applications of ADCs

Conversion Frequency (MHz)

Resolution (bit)

- Flash
- HDD
- DVD
- Digital I/F
- VDSL
- Digital TV
- Digital Camera
- ADSL
- GSM handset
- Digital Pipeline
- Motor servo
- Cellular phone
- Conventional Audio
- CD/MD
- DVD Audio
- DVD Player

Progress of technology

Sigma Delta
ADC Architecture: Flash and pipeline

Flash is used for ultra-high speed conversion with low resolution.
Pipeline is used for high resolution with moderate conversion speed.

Flash
Deliverables; Folding Interpolation

Ultra-high speed (~2GHz)
Low resolution (<8bit)
Large power consumption

Pipeline

Suitable for CMOS Switched capacitor operation

High resolution (<14bit)
Moderate speed (<100MHz)
Low power consumption
Integrating ADC (1)

- High resolution (20bit and more)
- Very low speed (DC measurement)
- Can realize zero offset voltage
- Small analog elements and easy to be embedded with digital circuits
Integrating ADC (2)

Going to 0 -> 1, when $V_x$ becomes negative.

$$v_x(T) = -\int_0^T \frac{-v_{in}}{RC} \, d\tau = \frac{v_{in}}{RC} T$$

Phase I
Successive-Approximation ADC (1)

Binary search algorithm

Multi clock cycles are needed.
Successive-Approximation ADC (2)

Charge-Redistribution ADC

Virtual ground

\[ v_x = 0 \]

Sampling mode

Comparator

16C + 8C + 4C + 2C + C + C + C

Sampled input signal

Reference voltage

\[ v_{in} \]

\[ v_{ref} \]

\[ v_{out} \]
Successive-Approximation ADC (3)

Charge-Redistribution ADC

\[ v_x = -v_{in} \]

Hold mode

Sampled input signal

Reference voltage

\[ v_{in} \]

\[ v_{ref} \]
Successive-Approximation ADC (4)

Charge-Redistribution ADC

Determine the output bits from MSB to LSB

\[ v_x = -v_{in} + \frac{v_{ref}}{2} \]

Bit cycling mode

Sampled input signal

Reference voltage
Flash ADC

Ultra fast operation: Several GHz
No sample and hold
Low resolution: <9 bit
Large input capacitance
Area and power increase exponentially with resolution
Two step parallel ADC

One of the basic architectures for video-rate ADCs
Chopper inverter comparator

Pros: Simple, low power, small area, low voltage, and sample and hold action
Cons: large absolute offset, suffer the power supply noise, sensitive to Vdd.

S1, S2:ON, S3:OFF; Signal sampling
S1, S2:OFF, S3:ON; Offset cancel and amplify

Vin=Vr: No change
Vin>Vr: Vout goes down
Two step parallel ADC

Realizing simultaneous signal sampling
2 channel lower conversion units realize two times higher operation
Overlap scheme relaxes needed offset voltage for comparators
Two step parallel ADC: Timing chart

- simultaneous sampling
- Hold in lower conversion when upper comparators compares
- Alternative action

Clock
Upper comparators
Lower comparators (R)
Lower comparators (L)
Output data

DATA (R)  DATA (L)  DATA (R)
Overlapping scheme

Set the reference voltage range in the lower conversion wider than that of the upper conversion to form the overlapping scheme. This scheme can relax the requirement for the mismatch voltage to the upper comparators.

Otherwise, sub-ranging and two step parallel ADC cause the conversion errors.
Conversion errors in Sub-ranging ADC

- Lower conversion values
- Upper conversion values

- Same
- Larger
- Lower

- “15” is missed
- Wider period for “15”

図 3.12 上位・下位の変換の様子
図 3.13 サブレンジング型 A/D 変換器の変換特性
Accuracy of the flash ADC

High resolution flash ADC is quite difficult. Because DNL degrades directly by transistor mismatch.

\[ DNL_{(\text{LSB})} = \frac{V_a - V_q}{V_q} \]

Offset voltage (mV) at sigma

Yield (%)

DNL<0.5 LSB

DNL<1.0 LSB

Analog bipolar

Digital bipolar

MOS
Interpolation by internal division method

\[ y_0 = ax \]
\[ y_{0b} = -ax \]
\[ y_1 = a(x - x_0) \]
\[ y_{1b} = -a(x - x_0) \]

\[ y_n = \frac{1}{m} \left\{ (m - n)y_0 + ny_1 \right\} \]

Interpolation method
Capacitive interpolation

Interpolation, offset cancel, amplification, in a pipeline manner.