Lecture 05: IC Manufacturing

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Review: CMOS Inverter

- Full rail-to-rail swing $\Rightarrow$ high noise margins
- Low output impedance
- High input impedance
- No direct path steady-state between power and ground $\Rightarrow$ no static power dissipation
- Propagation delay a function of load capacitance and on resistance of transistors
CMOS Transistor
CMOS Chip
Growing the Silicon Ingot

From Smithsonian, 2000
Photolithographic Process

1. Acid etch
2. Spin, rinse, dry
3. Oxidation
4. Photoresist coating
5. Photoresist development
6. Stepper exposure
7. Optical mask
8. Photoresist removal (ashing)
9. Process step

- Oxidation
- Optical mask
- Stepper exposure
- Photoresist removal (ashing)
- Process step
- Spin, rinse, dry
- Acid etch
- Photoresist coating
- Photoresist development
A Modern CMOS Process

Dual-Well Trench-Isolated CMOS

gate oxide

field oxide

p well

n well

p- epi

SiO$_2$

Al (Cu)

TiSi$_2$

n+ p+ p-

SiO$_2$

p well

n well

p- epi

SiO$_2$
CMOS Process at a Glance

- Define active areas
- Etch and fill trenches

- Implant well regions

- Deposit and pattern polysilicon layer

- Implant source and drain regions and substrate contacts

- Create contact and via windows
- Deposit and pattern metal layers

- One full photolithography sequence per layer (mask)

- Built (roughly) from the bottom up
  1. tubs (aka wells, active areas)
  2. polysilicon
  3. source and drain diffusions
  4. metal 1
  5. metal 2

Q: Why build poly before building diffusion?
Patterning - Photolithography

1. Oxidation

2. Photoresist (PR) coating

3. Stepper exposure

4. Photoresist development and bake

5. Acid etching
   - Unexposed (negative PR)
   - Exposed (positive PR)

6. Spin, rinse, and dry

7. Processing step
   - Ion implantation
   - Plasma etching
   - Metal deposition

8. Photoresist removal (ashing)
Example of Patterning of SiO2

1&2. After oxidation and deposition of negative photoresist.

3. Stepper exposure.

4. After development and etching of resist, chemical or plasma etch of SiO₂.

5. After etching.

Self-Aligned Gates

1. Create thin oxide in the “active” regions, thick elsewhere

2. Deposit polysilicon

3. Etch thin oxide from active region (poly acts as a mask for the diffusion)

4. Implant dopant
Simplified CMOS Inverter Process
P-Well Mask
Active Mask
Poly Mask
P+ Select Mask
N+ Select Mask
Contact Mask
Metal Mask
Exponentially growing standard-cell-ASIC mask-set, NRE, and tool-set expenses are motivating many potential customers to consider alternatives (courtesy Altera).
Layout Editor: *max* Design Frame
**max Layer Representation**

- **Metals (five) and vias/contacts between the interconnect levels**
  - Note that m5 connects only to m4, m4 only to m3, etc., and m1 only to poly, ndif, and pdif
  - Some technologies support “stacked vias”

- **Active – active areas on/in substrate** (poly gates, transistor channels (nfet, pfet), source and drain diffusions (ndif, pdif), and well contacts (nwc, pwc))

- **Wells (nw) and other select areas** (pplus, nplus, prb)
CMOS Inverter \textit{max} Layout

- Metal1
- Metal2
- PFET
- PDIF
- Metal1-diff via
- GND
- Metal2-metal1 via
- Metal1-poly via
- Polysilicon
- PMOS ($4/0.24 = 16/1$)
- NMOS ($2/0.24 = 8/1$)
- V_{DD}

Diagram showing the layout of a CMOS inverter with various metal layers and polysilicon connections.
Simplified Layouts in \textit{max}

- Online design rule checking (DRC)

- Automatic fet generation (just overlap poly and diffusion and it creates a transistor)

- Simplified via/contact generation
  - v12, v23, v34, v45
  - ct, nwc, pwc

![Diagram of layout dimensions]
Design Rule Checker

poly_not_fet to all_diff minimum spacing = 0.14 um
Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers
Why Have Design Rules?

- To be able to tolerate some level of fabrication errors such as

1. Mask misalignment

2. Dust

3. Process parameters (e.g., lateral diffusion)

4. Rough surfaces
Why Have Design Rules?

Designed

Result

decreasing dimension
Intra-Layer Design Rule Origins

- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)

- Minimum spaces between objects (that are not related) on the same layer to ensure they will not short after fab
Inter-Layer Design Rule Origins

1. Transistor rules – transistor formed by overlap of active and poly layers

Transistors

Unrelated Poly & Diffusion

Catastrophic error

Thinner diffusion, but still working
Transistor Layout
IBM Research New

IBM Creates New Dimension for High-Performance Chips

Research Breakthrough Opens New Door in Chip Performance Race

November 11, 2002 – Yorktown Heights, NY -- IBM today announced that it has developed a new technique for building three-dimensional (3D) integrated circuits (ICs) that will help increase chip performance, functionality and density. This technique is an essential step toward successful realization of high performance 3D ICs.

A Representative IC 3D IC

- Multiple layers of active devices
- Vertical interconnects between layers
IBM “Assembly” Approach to 3D IC Fabrication

- Device layers stacked using wafer bonding
- Each layer fabricated by conventional processes
- Layers fabricated and tested simultaneously

- Attach circuit to glass handle wafer
- Remove original substrate
- Align & bond top circuit to bottom circuit
- Remove handle wafer & adhesives
- Form vertical interconnects
Next Lecture and Reminders

- Next lecture
  - Static complementary CMOS gate design
    - Reading assignment – Rabaey, et al, 6.1-6.2.1