CMPEN 411  VLSI Digital Circuits

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Chip Fabrication and Layout
Substrate to VDD contact

Source to VDD contact

N well, green

VDD to source connection, M1

Source to VDD connection, CONTACT

Drain, P-diffusion

Gate, poly

Metal1 to P-diffusion connection, CONTACT

Poly wire, M1

Metal2 to metal1 connection, VIA

Metal2 wire, M2

Poly wire, P
Also check the transistor layout tutorial at:
http://www.egr.msu.edu/classes/ece410/mason/files/TutorialB.pdf

or local copy at:
http://www.cse.psu.edu/~kyusun/class/cmpen411/13s/hw/msuOldTutorialB.pdf
Using ‘gimp’ program running in Linux to delete black background color.
Fig. 1. Cross-section of a 64-bit high-speed processor in a 90nm technology. (Courtesy: IBM)