CMPEN 411  VLSI Digital Circuits

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Circuit Simulation

Hspice Tip
Hspice circuit simulation program

0. Design synthesis

1. Before the expensive chip fabrication

2. Be sure correct working

3. Estimate its performance parameters
Hspice circuit simulation

Simple example of 2 input AND gate
Hspice circuit simulation: and2
Hspice circuit simulation: and2

and2.s
netlist file
Hspice circuit simulation: and2

and2.hsp
command file
Hspice circuit simulation: and2

and2.hsp command file

Combine and2.hsp and and2.s files to generate and2.sp spice simulation file:

% hsp50 and2
Hspice circuit simulation: and2

and2.sp

spice file

```
.option post
.option ACCT=1 BRIEF=1
.option NUMDGT=8 MEASDGT=8 $ for output printing
.option ACCURATE $ this is for transient analysis only
.option runlvl=0
*
* VVDD vdd! 0 5.00
Vain ain 0 PWL 0.10NS 0.00V 10.00NS 0.00V 10.10NS 5.00V 20.00NS 5.00V
+ 20.10NS 0.00V 30.00NS 0.00V 30.10NS 5.00V 40.00NS 5.00V
+ 40.10NS 0.00V 60.00NS 0.00V 60.10NS 5.00V 70.00NS 5.00V
+ 70.10NS 0.00V 80.00NS 0.00V 80.10NS 5.00V 90.00NS 5.00V
+ 90.10NS 0.00V 100.00NS 0.00V 100.10NS 5.00V 110.00NS 5.00V
+ 110.10NS 0.00V 120.00NS 0.00V
Vbin bin 0 PWL 0.10NS 0.00V 20.00NS 0.00V 20.10NS 5.00V 50.00NS 5.00V
+ 50.10NS 0.00V 80.00NS 0.00V 80.10NS 5.00V 120.00NS 5.00V
*zout 000100001010
CL zout 0 10f
.TRAN 0.01NS 120.00NS
*
** Generated for: hspiceD
** Generated on: Jan 23 16:58:23 2012
** Design library name: hw0demo
** Design cell name: and2
** Design view name: extracted
```
Hspice circuit simulation: and2

```
option post
option ACCT=1 BRIEF=1
option NUMDGT=8 MEASDGT=8 $ for output printing
.option ACCURATE $ this is for transient analysis only
.option runlvl=0

* VVDD vdd: 0 5.00
Vain ain 0 PWL 0.10NS 0.00V 10.00NS 0.00V 10.10NS 5.00V 20.00NS 5.00V
+ 20.10NS 0.00V 30.00NS 0.00V 30.10NS 5.00V 40.00NS 5.00V
+ 40.10NS 0.00V 60.00NS 0.00V 60.10NS 5.00V 70.00NS 5.00V
+ 70.10NS 0.00V 80.00NS 0.00V 80.10NS 5.00V 90.00NS 5.00V
+ 90.10NS 0.00V 100.00NS 0.00V 100.10NS 5.00V 110.00NS 5.00V
+ 110.10NS 0.00V 120.00NS 0.00V
Vbin bin 0 PWL 0.10NS 0.00V 20.00NS 0.00V 20.10NS 5.00V 50.00NS 5.00V
+ 50.10NS 0.00V 80.00NS 0.00V 80.10NS 5.00V 120.00NS 5.00V
*zout 000100001010
CL zout 0 10f
.TRAN 0.01NS 120.00NS
*
** Generated for: hspiceD
** Generated on: Jan 23 16:58:23 2012
** Design library name: hw0demo
** Design cell name: and2
** Design view name: extracted
```
Hspice circuit simulation: and2

and2.sp

spice file
**Hspice circuit simulation: and2**

```
* .option post
  .option ACCT=1 BRIEF=1
  .option NUMDGT=8 MEASDGT=8 $ for output printing
  .option ACCURATE $ this is for transient analysis only
  .option runlvl=0
*

VDDD vdd! 0 5.00
Vain ain 0 PWL 0.10NS 0.00V 10.00NS 0.00V 10.10NS 5.00V 20.00NS 5.00V 
  + 20.10NS 0.00V 30.00NS 0.00V 30.10NS 5.00V 40.00NS 5.00V 
  + 40.10NS 0.00V 60.00NS 0.00V 60.10NS 5.00V 70.00NS 5.00V 
  + 70.10NS 0.00V 80.00NS 0.00V 80.10NS 5.00V 90.00NS 5.00V 
  + 90.10NS 0.00V 100.00NS 0.00V 100.10NS 5.00V 110.00NS 5.00V 
  + 110.10NS 0.00V 120.00NS 0.00V
Vbin bin 0 PWL 0.10NS 0.00V 20.00NS 0.00V 20.10NS 5.00V 50.00NS 5.00V 
  + 50.10NS 0.00V 80.00NS 0.00V 80.10NS 5.00V 120.00NS 5.00V
*zout 000100001010
CL  zout 0 10f
.TRAN 0.01NS 120.00NS
*
```

**Generated for: hspiced
** Generated on: Jan 23 16:58:23 2012
** Design library name: hw0demo
** Design cell name: and2
** Design view name: extracted
Hspice circuit simulation: and2

and2.sp
spice file
Hspice circuit simulation: and2

% hspice and2.sp

Run simulation

---

```
# va device = 0

<table>
<thead>
<tr>
<th></th>
<th>time</th>
<th># points</th>
<th>tot. iter</th>
<th>conv. iter</th>
</tr>
</thead>
<tbody>
<tr>
<td>op point</td>
<td>0.00</td>
<td>1</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>transient</td>
<td>0.21</td>
<td>12001</td>
<td>12916</td>
<td>6367 rev= 193</td>
</tr>
<tr>
<td>readin</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>errchk</td>
<td>0.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>setup</td>
<td>0.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>output</td>
<td>0.00</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

  total cpu time        0.22 seconds
  total elapsed time    1 seconds
  job started at  14:55:11 01/24/2012
  job ended    at  14:55:12 01/24/2012

>info:       ***** hspice job concluded
Init: hspice initialization file: /home/software/synopsys-2008/hspice/hspice/hspice.ini
lic: Release hspice token(s)
real 0.46
user 0.22
sys 0.01
p218inst26.cse.psu.edu 100%
```
Hspice circuit simulation: and2

% sc and2.tr0 &

View result
Hspice circuit simulation: and2

Timing measurement on the signal plot
Hspice circuit simulation: **and2**

**and2.hsp**
command file

Add useful spice
**.MEASURE**
commands
Hspice circuit simulation: and2

Resulting and2.sp spice file with .MEASURE commands
Hspice circuit simulation: and2

.MEASURE

Results:

*****
** cell name: and2
****** transient analysis     tnom= 25.000 temp= 25.000
******

and2delayup= 255.80303957p  targ= 30.30580304n  trig= 30.05000000n
and2delaydn= 210.97350302p  targ= 40.26097350n  trig= 40.05000000n
and2delayavg= 233.38827130p
and2riset= 168.88019017p  targ= 30.39978889n  trig= 30.23090870n
and2fallt= 133.66493165p  targ= 40.32853643n  trig= 40.19487150n
and2pwravg= 42.53943953u  from= 0.  to= 120.00000000n
and2pwrmax= 4.47106810m  at= 90.10000000  from= 0.  to= 120.00000000n

***** job concluded
****** HSPICE -- A-2006.03 32-BIT (Feb 26 2008) linux *****
******
** cell name: and2
****** job statistics summary     tnom= 25.000 temp= 25.000
******

total memory used           162 kbytes
# nodes = 7  # elements= 32
# diodes= 0  # bjts = 0  # jfets = 0  # mosfets = 6
Hspice circuit simulation: .hsp file rules

and2.hsp command file

VDD line defines voltage value for the vdd! node in reference to gnd! node.
CLK line defines minimum **time step** between any signal change in nano-second.
RISE line defines signal rise time in nano-second.
FALL line defines signal fall time in nano-second.
ain, bin: List of signal names and their values at each **time step**.
* character as the first character of a line makes that line a comment. Hspice will skip the line.
Hspice circuit simulation: .hsp file rules

and2.hsp command file

Two signals \texttt{ain} and \texttt{bin} produced by above .hsp file will be 120 ns in total length, each 1 and 0 taking 10.0 ns each. The rise time and fall time is included in the 10.0 ns time step specified by CLK line.
Hspice circuit simulation:  .hsp file rules

and2.hsp command file

Time step change:  the following lines will produce the same ain signal as shown above:

VDD      5.0
CLK      5.0
RISE     0.1
FALL     0.1
ain      001100110000110011001100
Hspice circuit simulation: .hsp file rules

and2.hsp command file

Signal specification: the following lines will produce the same ain signal as shown above:

VDD  5.0
CLK  10.0
RISE 0.1
FALL 0.1
ain  010100 101010
Hspice circuit simulation: .hsp file rules

**and2.hsp command file**

.. line will be copied exactly on to the .sp file. One may add any native hspice line this way. For example, ‘..CL zout 0 10f’ line will result in ‘CL zout 0 10f’ line in the .sp file.

. line will be copied exactly on to the .sp file, including the dot. One may add any hspice dot command line this way. For example, ‘.option ACCURATE’ line will result in ‘.option ACCURATE’ line in the .sp file.
Hspice circuit simulation: .hsp file rules

and2.hsp command file

A blank line is allowed in the .hsp file. Just be sure that there is NO space characters in the blank line. For example, the following is OK:

VDD 5.0
CLK 10.0
RISE 0.1
FALL 0.1

A blank line is allowed in the .hsp file. Just be sure that there is NO space characters in the blank line. For example, the following is OK:

VDD 5.0
CLK 10.0
RISE 0.1
FALL 0.1
Tip: Increased accuracy in simulation:

Inverter circuit
Tip: Increased accuracy in simulation:

Inverter circuit
Normal
High-Speed
Simulation

```
VDD  5.0
CLK  10.0
RISE 0.1
FALL 0.1
vin  01010
..CL1 vout 0 10fF
```
Tip: Increased accuracy in simulation:

Inverter circuit
Normal
High-Speed
Simulation
**Tip:** Increased accuracy in simulation:

Inverter circuit

<table>
<thead>
<tr>
<th></th>
<th>Time</th>
<th># Points</th>
<th>Total Iter</th>
<th>Conv. Iter</th>
</tr>
</thead>
<tbody>
<tr>
<td>op point</td>
<td>0.00</td>
<td>1</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>transient</td>
<td>0.01</td>
<td>5001</td>
<td>2130</td>
<td>1048 rev= 8</td>
</tr>
<tr>
<td>readin</td>
<td>0.01</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>errchk</td>
<td>0.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>setup</td>
<td>0.00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>output</td>
<td>0.00</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Total CPU time: 0.02 seconds
Total elapsed time: 1 seconds
Job started at: 12:35:27 01/31/2013
Job ended at: 12:35:20 01/31/2013
Tip: Increased accuracy in simulation:

Inverter circuit
Normal
High-Speed Simulation
Tip: Increased accuracy in simulation:

Inverter circuit
Normal
High-Speed Simulation
Tip: Increased accuracy in simulation:

Inverter circuit
Normal
High-Speed Simulation
Tip: Increased accuracy in simulation:

Inverter circuit
More accurate Simulation
Tip: Increased accuracy in simulation:

Inverter circuit
More Accurate Simulation, Slower Simulation Speed

```
# va device = 0

analysis          time    # points  tot. iter  conv.iter
op point          0.00    1         7         
transient         0.05    50001     20044     10021  rev= 0
readin            0.01    
errchk            0.00    
setup             0.00    
output            0.00    

  total cpu time         0.06 seconds
  total elapsed time     1 seconds
  job started at 12:45:07 01/31/2013
  job ended at 12:45:07 01/31/2013

>info:       ***** hspice job concluded
Init: hspice initialization file: /home/software/synopsys-2008/hspice/hspice/hspice.ini
lic: Release hspice token(s)
real 0.29
user 0.06
sys 0.01
p218inst31.cse.psu.edu 296%
```
Tip: Increased accuracy in simulation:

Inverter circuit
More Accurate Simulation, Slower Simulation Speed
Tip: Increased accuracy in simulation:

Inverter circuit
More Accurate Simulation, Slower Simulation Speed
Tip: Increased accuracy in simulation:

Inverter circuit
More Accurate Simulation, Slower Simulation Speed

Zoom-in view
Tip: Increased accuracy in simulation:

Inverter circuit
Even More
Accurate
Simulation,
Even Slower
Simulation Speed
Tip: Increased accuracy in simulation:

Inverter circuit

Even More Accurate Simulation, Even Slower Simulation Speed
Tip: Increased accuracy in simulation:

Inverter circuit
Even More Accurate Simulation, Slower Simulation Speed
**Tip:** Increased accuracy in simulation:

Inverter circuit

Even More

Accurate

Simulation, Slow Simulation Speed
Tip: DC simulation:

Inverter Circuit

First comment out the .TRANS line by placing ‘*’ in the first column.

Add .DC line as shown, sweep Vvin voltage source from 0V to 5V in 1mV steps.

Run hspice and wave view the SCHinvDC.sw0 file.
Tip: DC simulation:

Inverter Circuit

Plot vout signal, Voltage Transfer Characteristic (VTC) curve.
**Tip: DC simulation:**

**Inverter Circuit**

\[ \text{vin} = \text{vout} \text{ at } 2.4V \text{ in this case.} \]

VTC curve can be shifted to the left or right by re-sizing the pmos or nmos transistors.

Noise margin of the inverter circuit can be determined from the VTC curve.
Tip: Transistor sizing
Tip: Transistor sizing

Inverter Circuit

Three inverters with different transistor sizes:
Tip: Transistor sizing

Inverter Circuit

Three inverters with different transistor sizes:
Tip: Transistor sizing

Inverter Circuit

Three inverters with different transistor sizes:

Wpmos : Wnmos

4.5um : 5.4um  vout1  10fF
4.5um : 2.7um  vout2  10fF
9.0um : 2.7um  vout3  10fF
Tip: Transistor sizing

Inverter Circuit

Three inverters with different transistor sizes:
Tip: Transistor sizing

Inverter Circuit

Three inverters:
Wp : Wn
4.5u : 5.4u \(v_{\text{out1}}\)
4.5u : 2.7u \(v_{\text{out2}}\)
9.0u : 2.7u \(v_{\text{out3}}\)
Tip: Transistor sizing

Inverter Circuit

Three inverters:
Wp : Wn
4.5u : 5.4u  vout1
4.5u : 2.7u  vout2
9.0u : 2.7u  vout3
Tip: Transistor sizing

Inverter Circuit

Three inverters:
Wp : Wn
4.5u : 5.4u vout1
4.5u : 2.7u vout2
9.0u : 2.7u vout3
Tip: Transistor sizing

Inverter Circuit

Three inverters:
Wp : Wn
4.5u : 5.4u vout1
4.5u : 2.7u vout2
9.0u : 2.7u vout3

VTC curves, DC analysis
Tip: Transistor sizing

Inverter Circuit

VTC curves, DC analysis

Three inverters:
Wp : Wn
4.5u : 5.4u vout1
4.5u : 2.7u vout2
9.0u : 2.7u vout3
Tip: Process variation test

Inverter Circuit

Spice program MOSFET model parameters: TT, FF, FS, SF, SS

T: Typical
F: Fast
S: Slow

PMOS
NMOS
Tip: Process variation test

Inverter Circuit
Tip: Process variation test

Inverter Circuit

```
VDD  5.0
CLK  5.0
RISE 0.1
FALL 0.1
vin  01010
..CL1 v01tt 0 10fF
..CL2 v02ff 0 10fF
..CL3 v03fs 0 10fF
..CL4 v04sf 0 10fF
..CL5 v05ss 0 10fF
```
Tip: Process variation test

Inverter Circuit

```
* Header file for an ASIC circuit HSPICE run
*
.option post
.option ACCT=1 BRIEF=1
.option NUMDGT=8 MEASDGT=8 $ for output printing
.option ACCURATE $ this is for transient analysis only
.option runlvl=0
*

VVD VDD vdd! 0 5.00
Vvin vin 0 PWL 0.10NS 0.00V 5.00NS 0.00V 5.10NS 5.00V
10.00NS 5.00V
+ 10.10NS 0.00V 15.00NS 0.00V 15.10NS 5.00V 20.00NS 5.00V
+ 20.10NS 0.00V 25.00NS 0.00V
CL1 voltt 0 10fF
CL2 vo2ff 0 10fF
CL3 vo3fs 0 10fF
CL4 vo4sf 0 10fF
CL5 vo5ss 0 10fF
```
Tip: Process variation test

Inverter Circuit

```
+ 10.10NS 0.00V 15.00NS 0.00V 15.10NS 5.00V 20.00NS 5.00V
+ 20.10NS 0.00V 25.00NS 0.00V

CL1 voltt 0 10fF
CL2 vo2ff 0 10fF
CL3 vo3fs 0 10fF
CL4 vo4sf 0 10fF
CL5 vo5ss 0 10fF

.TRAN 0.0001NS 25.00NS
*
** Generated for: hspiceD
** Generated on: Feb 5 01:41:10 2013
** Design library name: hw1
** Design cell name: inv5
** Design view name: schematic

.GLOBAL vdd!

.TEMP 25
.OPTION
* ARTIST=2
* INCOLD=2
```
Tip: Process variation test

Inverter Circuit

```plaintext
* Library name: hw1
** Cell name: inv5
*** View name: schematic
mp5 vo5ss vin vdd! vdd! ami06pss L=600e-9 W=4.5e-6 AD=6.75e-12 AS=6.75e-12 PD=12e-6 PS=12e-6 M=1
mp4 vo4sf vin vdd! vdd! ami06psf L=600e-9 W=4.5e-6 AD=6.75e-12 AS=6.75e-12 PD=12e-6 PS=12e-6 M=1
mp3 vo3fs vin vdd! vdd! ami06pfs L=600e-9 W=4.5e-6 AD=6.75e-12 AS=6.75e-12 PD=12e-6 PS=12e-6 M=1
mp2 vo2ff vin vdd! vdd! ami06pff L=600e-9 W=4.5e-6 AD=6.75e-12 AS=6.75e-12 PD=12e-6 PS=12e-6 M=1
mn1 vottt vin vdd! vdd! ami106P L=600e-9 W=4.5e-6 AD=6.75e-12 AS=6.75e-12 PD=12e-6 PS=12e-6 M=1
mn5 vo5ss vin 0 0 ami06nss L=600e-9 W=2.7e-6 AD=4.05e-12 AS=4.05e-12 PD=8.4e-6 PS=8.4e-6 M=1
mn4 vo4sf vin 0 0 ami06nsf L=600e-9 W=2.7e-6 AD=4.05e-12 AS=4.05e-12 PD=8.4e-6 PS=8.4e-6 M=1
mn3 vo3fs vin 0 0 ami06nfs L=600e-9 W=2.7e-6 AD=4.05e-12 AS=4.05e-12 PD=8.4e-6 PS=8.4e-6 M=1
mn2 vo2ff vin 0 0 ami06nff L=600e-9 W=2.7e-6 AD=4.05e-12 AS=4.05e-12 PD=8.4e-6 PS=8.4e-6 M=1
mn1 vottt vin 0 0 ami06N L=600e-9 W=2.7e-6 AD=4.05e-12 AS=4.05e-12 PD=8.4e-6 PS=8.4e-6 M=1
*END

* Tail file for the various MOSFET models
* MOSIS AMI06 models and others for HSPICE run
*
.INCLUDE "~/home/faculty/kyusun/c41i/spmod/mosis02models.sp"
*
.END
```
Tip: Process variation test

Inverter Circuit
Tip: Process variation test

Inverter Circuit
Tip: Process variation test

Inverter Circuit

Temperature

Supply Voltage
Tip: Process variation test

Inverter Circuit

Temperature

0° – 85°
-40° – 100°
-55° – 125°

Supply Voltage
Tip: Process variation test

Inverter Circuit

Temperature

Supply Voltage
4.5V – 5.5V
Tip: Process variation test

Inverter Circuit