Kyusun Choi
Assistant Professor
Department of Computer Science and Engineering
The Pennsylvania State University

Image source: http://www.target.com
Radio Technology

Military radio …
Hardware Platform

Miniaturization on Chip

Precision PLL module on Pentium chip

Image source:
ELECTRONIC CRAZY
CHIP DESIGN R&D

ANALOG & DIGITAL MIXED SIGNAL

CHIP DESIGN LABORATORY

Kyusun Choi

Computer Science and Engineering Department
The Pennsylvania State University
Applications: Ultrasound Microscope

1. Ultrasound Microscope
2. Ultrasound Endoscope
3. Ultrasound Pill-camera

Ultrasound pill-camera complements the photo pill-camera by providing the following advantages:

1. Imaging below the tissues
2. Imaging even in murky liquids
3. Imaging without illumination

Remote medical practice
Soldiers – Military
Astronauts - NASA
High Frequency Transducers

Xylophone Transducer Array

Post Transducer Array
A CMOS Ultrasonic Transceiver Chip

Test Board

The First Generation Chip

Chip Block Diagram (1 Channel)
System Architecture: Receiver

- Transducers
- Preamp
- TGC*
- A/D Converter
- SRAM (3 Kbyte)
- Control & DSP

Vin_max
Vin_min

V_{TGC}(max)

Required Min. Process Gain = Aperture of ADC
= Preamp + TGC Min. Gain (dB)
= V_{TGC}(max) (dBm) – Vin_max (dBm)
= 56 dBm – 46 dBm = 10 dB

Required TGC gain range = Attenuation rate (dB)
= Vin_max (dBm) - Vin_min (dBm)
= 46 dBm – 25 dBm = 21 dB

*TGC: Time Gain Control
Block diagram of the Receiver

**Preamp Specification**
- Gain: 5 dB ~ 19 dB (Adjustable)
- Bandwidth: 600 MHz @ 5 dB
  ~ 150 MHz @ 19 dB

**TGC Specification**
- Gain: 0 dB to 20 dB
- Bandwidth: over 300 MHz
System Architecture: ADC

Control & DSP

Receive Circuitry

A/D converter with memory

A/D Converter

SRAM (3 Kbyte)

ADC Specification
- Resolution: 48 dB (8 bit)
- Conversion Speed: 250 MHz

Block Diagram of the ADC

Output Characteristic of 1bit ADC cell
System Architecture: Memory

Block Diagram of the SRAM

SRAM Specification
- Speed: 125 MHz
- Capacity: 3 Kbyte
- Data Bus: 16 bit
**Transmitter**

The Schematic of the Transmitter shows the flow of signals from the Tx_pulse Generator to the various channels (Ch<0>, Ch<1>, Ch<8>, Ch<9>). The signals pass through Delay stages before reaching the Tx_drv stages, which drive the respective channels.

**Programmable Channel Delay**
- Min. Delay: 0 ps
- Max. Delay: 480 ps
- Delay Step: 20 ps

The Channel Delay Circuits consist of Coarse Delay and Fine Delay sections. The Coarse Delay has delays of 0 ps, 200 ps, 400 ps, and 600 ps. The Mux selects between these delays. The Fine Delay has delays of 20 ps and 40 ps, each controlled by switches.
Present work

- The 2nd generation transceiver chip is being designed
  - Design Improvement
    - Control
    - TCG
    - ADC
    - Delay Channel
    - # of channel: 16
    - Small Size: 10 mm$^2$
- Test & Image Acquisition
  - Hook up with the novel transducer array
  - FPGA Beamformer
Ultrasound Robot Eye for Autonomous Navigation
RobotEye Transducer
RobotEye Chip
RobotEye System
<table>
<thead>
<tr>
<th>fo</th>
<th>attenuation (dB/cm)</th>
<th>dynamic range (dB)</th>
<th>max. distance (ft)</th>
<th>max. distance (m)</th>
<th>Maximum 2 Way Travel Time (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.00E+04</td>
<td>4.00E-01</td>
<td>100</td>
<td>1.25E+02</td>
<td>3.81E+01</td>
<td>1.99E+02</td>
</tr>
<tr>
<td>1.20E+05</td>
<td>1.20E+00</td>
<td>100</td>
<td>4.17E+01</td>
<td>1.27E+01</td>
<td>6.63E+01</td>
</tr>
<tr>
<td>2.20E+05</td>
<td>2.20E+00</td>
<td>100</td>
<td>2.27E+01</td>
<td>6.93E+00</td>
<td>3.62E+01</td>
</tr>
<tr>
<td>3.20E+05</td>
<td>3.20E+00</td>
<td>100</td>
<td>1.56E+01</td>
<td>4.76E+00</td>
<td>2.49E+01</td>
</tr>
</tbody>
</table>

Note: Need to know minimum and maximum distance
PIEZOCAD INPUT PARAMETERS

Data file: NEW - Not saved  Date and time calculated: 08-31-2006 15:00:29
220kHz single sinewave excitation 25mm diameter Circular Transducer

EXCITATION WAVEFORM
Sine wave burst 0.22 MHz, 1. cycles, delay: 0. usec, phase: 0. degrees, 100 points

FREQUENCY AND TIME
Design center frequency $f_d = 0.220$ MHz  Frequency range of calculation: 0.000 to 1.000 MHz
Number of points in frequency domain: 64  Time domain: 256

PIEZOELECTRIC ELEMENT DESCRIPTION
Element size: 25 mm disk  Element area: 490.8739 mm$^2$
PARAMETER       VALUE          UNITS
Thickness        0.8727        mm
Parallel frequency $f_p$ 2.5208  MHz
Material         EC-38
Polarity         +

Longitudinal impedance  24.495  MRayls
Longitudinal velocity  4400.0  m/sec
Shear velocity  2200.0  m/sec
Density           7640.0  kg/m$^3$
Clamped capacit. $C_o$  12195.5  pF
Clamped dielectric const.  2450.00  E33s
Thick. coupling $k_t$  0.5300
Electrical loss tangent  0.0370  tan $\delta$
Mechanical loss tangent  0.0193  tan $\delta$
Vendor            Ede Acoustics

Data source        Data sheet

ACOUSTIC LAYERS
No Faceplates
No Backplate

ACOUSTIC LOAD IMPEDANCES: Rear: 5126 MRayls  Front: 1500 MRayls

ELECTRICAL TERMINATIONS:  Transmitter output = 50.0 Ohms  Receiver input = 50.0 Ohms

ELECTRICAL MATCHING NETWORK:
No electrical matching network.
Miniature OCXO

- Conventional OCXO
  - separate temperature control and oscillator boards
  - packaged resonator and oven block
  - high power, large size
Proof-of-Concept Miniature OCXO

- One-chip CMOS implementation
  - oscillator
  - temperature sensor
  - heater
  - control circuit
  - on-chip crystal resonator

- Advantages
  - low power consumption
  - small package size
  - low cost
Temperature Sensor

- CMOS inverter-like structure
- adjustable operating range
- 18 mV/°C sensitivity

![Temperature Sensor Diagram]
Heater

- poly resistors and NMOS transistors
- controllable current flow
- 350 mA maximum current (3.3 V supply, 1.1 Watts)
- standard design rule → reliable operation
Temperature Control Circuit

- sensor < $V_{r1}$ → increase $V_{hc}$ → increase heater current → increase temperature
- sensor > $V_{r2}$ → decrease $V_{hc}$ → decrease heater current → decrease temperature
- $V_{r1} < $ sensor < $V_{r2}$ → no change in $V_{hc}$ and heater current → maintain temperature
On-Chip Quartz Crystal Resonator

SEM image of quartz crystal on a chip

quartz crystal on a CMOS chip

MOSIS test chip with on-chip resonator

unpackaged chip wire bonded on PCB with on-chip resonator
Test FERs
**OCXO Chip**

1. **temperature sensors**
   - Multiple sensors for testing purpose

2. **heaters**

3. **oscillator**
   - Pierce-type oscillator

4. **op-amps**
   - For temperature control

5. **mounting structure**
   - Resonator mounting pads

AMI 0.5 µm process (MOSIS)
(2.5 mm X 2.0 mm)
Initial Test OCXO Implementation

- unpackaged chip wire bonded on PCB
- resonator and IC are sealed to build a temporary oven structure
- the structure covered with styrofoam to reduce heat loss
Initial Test OCXO Implementation

test boards
Conclusions

• Proof-of-concept miniature OCXO
  – chip temperature stabilized – 0.17 °C
  – resonator frequency stabilized – 0.7 ppm
  – reduced power consumption – 303 mW
  – short warm-up time – 3 minutes

• For more improvements
  – packaging issues
  – more integration
INTEGRATING QUARTZ CRYSTAL ON CHIP FOR ULTRA COMPACT AND HIGH PRECISION CLOCK GENERATION

Kyusun Choi

Computer Science and Engineering Department
Electrical Engineering Department
The Pennsylvania State University
PLL & QUARTZ CRYSTAL ON CHIP

Crystal Mounting on Unpackaged Chip
Mounted Crystal Testing

1. Mount the crystal on a unpackaged prototype chip
2. Mount the chip on a custom made test PC board
3. Test mounted crystal oscillator characteristics
PLL & QUARTZ CRYSTAL ON CHIP

Crystal Mounting on Packaged Chip
Mounted Crystal Testing

1. Mount the crystal on a packaged prototype chip
2. Mount the packaged chip on a custom made test PC board
3. Test mounted crystal oscillator characteristics
PLL & QUARTZ CRYSTAL ON CHIP

Second prototype chip design

1. 0.5um CMOS
2. Full custom layout
3. Mount structure
4. Oscillator circuit
5. PLL circuit
Featured ADC

1. Future-ready, < 0.10um, < 1.0V
   0.07um

2. CMOS, SOC applications

3. RF applications

4. High speed ADC, 3.5 GSPS, 8 bit
TIQ Flash ADC
**TIQ Comparator**

**DIFFERENTIAL INPUT VOLTAGE COMPARATOR**

Vin → Vout

**INVERTER**

Vin → Vm → Vout

Vr is provided by a voltage references source, external to the voltage comparator.

Vm is an internal parameter of an inverter, fixed by the transistor sizes.
TIQ Comparator

- High speed
- Less area
- No resistor ladder and reference voltages
- No capacitor switching
- Future ready
  - Scale down
  - Low supply voltage
  - Standard digital logic technology
  - Ideal for SOC
8-bit TIQ Flash ADC

Layout in 0.07um CMOS Rule

GLSVLSI03
8-bit ADC Simulation
Prototype Test Result

Input: 100 KHz Saw wave

6-bit TIQ ADC
0.18um CMOS

GLSVLSI03
Prototype Test Result

Input: 100 KHz Saw wave

9-bit TIQ ADC
0.25um CMOS
# ADC Comparison

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>TIQ</td>
<td>Flash</td>
<td>6-bit</td>
<td>0.7 V</td>
<td>0.07 um</td>
<td>4.76 GSPS</td>
<td>11.3 mW</td>
</tr>
<tr>
<td>TIQ</td>
<td>Flash</td>
<td>8-bit</td>
<td>0.7 V</td>
<td>0.07 um</td>
<td>3.57 GSPS</td>
<td>48.9 mW</td>
</tr>
<tr>
<td>Ref. [2]</td>
<td>Σ∆</td>
<td>10-bit</td>
<td>1.0 V</td>
<td>0.5 um</td>
<td>384 KSPS</td>
<td>1.56 mW</td>
</tr>
<tr>
<td>Ref. [3]</td>
<td>SAR</td>
<td>10-bit</td>
<td>1.0 V</td>
<td>0.18 um</td>
<td>200 KSPS</td>
<td></td>
</tr>
<tr>
<td>Ref. [4]</td>
<td>Pipeline</td>
<td>9-bit</td>
<td>1.0 V</td>
<td>0.5 um</td>
<td>5 MSPS</td>
<td>1.6 mW</td>
</tr>
<tr>
<td>Ref. [5]</td>
<td>SAR</td>
<td>8-bit</td>
<td>1.0 V</td>
<td>1.2 um</td>
<td>50 MSPS</td>
<td>0.34 mW</td>
</tr>
<tr>
<td>Ref. [6]</td>
<td>Flash + Interp.</td>
<td>6-bit</td>
<td>0.8 V</td>
<td>0.13 um</td>
<td>25 MSPS</td>
<td>0.48 mW</td>
</tr>
<tr>
<td>Ref. [7]</td>
<td>Σ∆</td>
<td>14-bit</td>
<td>1.1 V</td>
<td>0.35 um</td>
<td>16 KSPS</td>
<td></td>
</tr>
</tbody>
</table>
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY

Steven Brown
Justin Ford
Loay Naji
Kyusun Choi

chip@cse.psu.edu

Computer Science and Engineering Department
Electrical Engineering Department
The Pennsylvania State University
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY
What Is The Prototype System?

- The hardware consists of two evaluation boards: an FPGA evaluation board and an ADC/DAC evaluation board.

- The system is limited by the processing speed of the FPGA, not the ADC sampling rate (50 MSPS).
Components and System Integration

- **FPGA**: Xilinx Spartan2, 200E
- **ADC**: Analog Devices AD9041, 10 bit, 210 MSPS (run at 50 MSPS)
- **DAC**: Analog Devices AD9751, 10 bit, 300 MSPS (run at 50 MSPS)
- **ADC Data Format**: Interleaved parallel, dual 10 bit data buses
- **DAC Data Format**: Synchronized parallel, dual 10 bit data buses
- **FPGA Board**: Digilent 2E System Board with DIO1 I/O board
- **ADC/DAC Board**: Analog Devices AD9410/PCB, modified to allow independent ADC and DAC operation
What Algorithm Was Used And What Were The Alternatives?

- **Finite Impulse Response (FIR)**
  - Can be implemented without floating point numbers
  - Requires many multipliers and adders (adders are cheap in this case) to implement
  - Frequency hopping is expensive (requires updating of 50 coefficients if sharp selectivity is required)

- **Infinite Impulse Response (IIR)**
  - Must be implemented with floating point numbers
  - Requires few multipliers and adders (adders are more expensive than multipliers in this case) to implement
  - Frequency hopping is cheap (requires updating of 4 coefficients)

- **IIR** was chosen
  - Due to feedback, pipelining is difficult and is of limited usefulness
  - Speed limited for a purely IIR implementation as a result
Algorithm Identification

Considered Algorithms / Selected Algorithm

Filter Structure  # Add  # Mult  Worst case latency

Std. Direct    3   3  2×ADLAT + 1×MULAT
All-pass       7   2  4×ADLAT + 2×MULAT
Lattice        3   4  3×ADLAT + 2×MULAT
Coupled        3   5  2×ADLAT + 1×MULAT
Zero-Free Direct  2   3  2×ADLAT + 1×MULAT

6-bit Mantissa Frequency Response

Though only 6-bit results are shown here, the algorithms were simulated with up to 10 bits of mantissa. The number of exponent bits was not as significant to the quality of the results.
Floating Point Operations

IEEE format not used, Non-standard mantissa size (10 bits)
Algorithm Modeling

A MATLAB Simulink model is representative of the actual system in terms of computational accuracy and clock cycles per operation. The figures at the right show the filter response to white noise input (the response to 25 individual identically distributed realizations is averaged to produce one output) in the frequency domain.
The algorithm implemented allowed for selective testing of either a single or cascaded algorithms. The algorithm identification phase suggested that frequency selectivity could be improved by cascading two algorithms, but that three or more would not yield significant gains.

The baseband processor for Amplitude Modulation is a digital peak detector.
Acknowledgements and Disclaimers

This material is based upon work supported by the Defense Advanced Research Projects Agency (DARPA), and administered by the Army Research Office under ESP MURI Award No. DAAD19-01-1-0504. Any opinions, findings, and conclusions or recommendations expressed in this publication are those of the authors and do not necessarily reflect the views of the Defense Advanced Research Projects Agency (DAPRA), and Army Research Office.
SOFTWARE DEFINED RADIO IN AN FPGA OPERATING AT CARRIER FREQUENCY