Lecture 15:

Dynamic CMOS

### Power and Energy Design Space

<table>
<thead>
<tr>
<th>Energy</th>
<th>Constant Throughput/Latency</th>
<th>Variable Throughput/Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Active</strong></td>
<td>Design Time</td>
<td>Non-active Modules</td>
</tr>
<tr>
<td><strong>(Dynamic)</strong></td>
<td>Logic design</td>
<td>Clock Gating</td>
</tr>
<tr>
<td></td>
<td>Reduced $V_{dd}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TSizing</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Multi-$V_{dd}$</td>
<td></td>
</tr>
<tr>
<td><strong>Leakage</strong></td>
<td>Multi-$V_T$</td>
<td>Sleep Transistors</td>
</tr>
<tr>
<td><strong>(Standby)</strong></td>
<td>Stack effect</td>
<td>Multi-$V_{dd}$</td>
</tr>
<tr>
<td></td>
<td>Pin ordering</td>
<td>Variable $V_T$</td>
</tr>
<tr>
<td></td>
<td>Input control</td>
<td></td>
</tr>
</tbody>
</table>
**Industry Example: IBM Cu11 (0.13 um)**

- **ASIC Cu11 (130nm) Library**: Dual-vt library
  - Nominal Vt level (~300mv)
  - Low Vt level (~210mv)
    - Low-vt version has same physical footprint
    - ~15% improvement in gate delay
    - ~10x increase in leakage power

**Dual-VDD (Voltage Island)**

Dual-supply voltage converters
How about Gate Leakage?

- multiple gate oxide (Sylvester et.al., DATE-2004)

Figure 3. Complete $V_T-\text{T}_{ox}$ versions of NAND2 gate
# Continuation of Moore’s Law

<table>
<thead>
<tr>
<th>Process Name</th>
<th>P856</th>
<th>P858</th>
<th>Px60</th>
<th>P1262</th>
<th>P1264</th>
<th>P1266</th>
<th>P1268</th>
<th>P1270</th>
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</thead>
<tbody>
<tr>
<td>1st Production</td>
<td>1997</td>
<td>1999</td>
<td>2001</td>
<td>2003</td>
<td>2005</td>
<td>2007</td>
<td>2009</td>
<td>2011</td>
</tr>
<tr>
<td>Process Generation</td>
<td>0.25µm</td>
<td>0.18µm</td>
<td>0.13µm</td>
<td>90 nm</td>
<td>65 nm</td>
<td>45 nm</td>
<td>32 nm</td>
<td>22 nm</td>
</tr>
<tr>
<td>Wafer Size (mm)</td>
<td>200</td>
<td>200</td>
<td>200/300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>300</td>
</tr>
<tr>
<td>Inter-connect</td>
<td>Al</td>
<td>Al</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>Cu</td>
<td>?</td>
</tr>
<tr>
<td>Channel</td>
<td>Si</td>
<td>Si</td>
<td>Si</td>
<td>Strained Si</td>
<td>Strained Si</td>
<td>Strained Si</td>
<td>Strained Si</td>
<td>Strained Si</td>
</tr>
<tr>
<td>Gate dielectric</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>High-k</td>
<td>High-k</td>
</tr>
<tr>
<td>Gate electrode</td>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td>Polysilicon</td>
<td>High-k</td>
<td>Metal</td>
</tr>
</tbody>
</table>

*Introduction targeted at this time*

*Subject to change*

*Intel found a solution for High-k and metal gate*
Dynamic CMOS

- In **static** circuits at every point in time (except when switching) the output is connected to either GND or $V_{DD}$ via a low resistance path.
  - fan-in of $N$ requires $2N$ devices

- **Dynamic** circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires only $N+2$ transistors
  - takes a sequence of **precharge** and conditional **evaluation** phases to realize logic functions
Dynamic Gate

Two phase operation

\[ \text{precharge} \quad (\text{CLK} = 0) \]
\[ \text{evaluation} \quad (\text{CLK} = 1) \]
Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.

- Inputs to the gate can make **only one** transition(s) during evaluation. **(X)**

- Output state is stored on $C_L$
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is $N+2$ (versus 2N for static complementary CMOS)
  - should be smaller in area than static complementary CMOS

- Full swing outputs ($V_{OL} = GND$ and $V_{OH} = V_{DD}$)

- Non-ratioed - sizing of the devices is not important for proper functioning (only for performance)

- Faster switching speeds
  - reduced load capacitance due to lower number of transistors per gate ($C_{int}$) so a reduced logical effort
  - reduced load capacitance due to smaller fan-out ($C_{ext}$)
  - no $I_{sc}$, so all the current provided by PDN goes into discharging $C_L$
  - Ignoring the influence of precharge time on the switching speed of the gate, $t_{PLH} = 0$ but the presence of the evaluation transistor slows down the $t_{PHL}$
Properties of Dynamic Gates, con’t

- Power dissipation should be lower
  - no short circuit power consumption since the pull-up path is not on when evaluating
  - lower capacitance - both $C_{\text{int}}$ (since there are fewer transistors connected to the drain output) and $C_{\text{ext}}$ (since there the output load is one per connected gate, not two)
  - by construction can have at most one transition per cycle – no glitch power

- But power dissipation can be significantly higher due to
  - clock tree power
  - extra load on clock transistors

- Needs a precharge clock
Dynamic Behavior

<table>
<thead>
<tr>
<th>#Trns</th>
<th>$V_{OH}$</th>
<th>$V_{OL}$</th>
<th>$V_{M}$</th>
<th>$NM_H$</th>
<th>$NM_L$</th>
<th>$t_{PHL}$</th>
<th>$t_{PLH}$</th>
<th>$t_{pre}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>2.5V</td>
<td>0V</td>
<td>$V_{Tn}$</td>
<td>2.5-$V_{Tn}$</td>
<td>$V_{Tn}$</td>
<td>110ps</td>
<td>0ns</td>
<td>83ps</td>
</tr>
</tbody>
</table>
Gate Parameters are Time Independent

- The amount by which the output voltage drops is a strong function of the input voltage and the available evaluation time.
  - Noise needed to corrupt the signal has to be larger if the evaluation time is short – i.e., the switching threshold is truly time independent.
Power Consumption of Dynamic Gate

Power only dissipated when previous Out = 0
Dynamic Power Consumption is Data Dependent

Dynamic 2-input NOR Gate

Assume signal probabilities
\[ P_{A=1} = \frac{1}{2} \]
\[ P_{B=1} = \frac{1}{2} \]

Then transition probability
\[ P_{0 \rightarrow 1} = P_{\text{out}=0} \times P_{\text{out}=1} \]

Switching activity can be higher in dynamic gates!

\[ P_{0 \rightarrow 1} = \frac{3}{4} \]
Issues in Dynamic Design: Charge Leakage

Minimum clock rate of a few kHz
Issues in Dynamic Design: Charge Leakage

Leakage sources

Minimum clock rate of a few kHz
Impact of Charge Leakage

- Output settles to an intermediate voltage determined by a resistive divider of the pull-up and pull-down networks.
  - Once the output drops below the switching threshold of the fan-out logic gate, the output is interpreted as a low voltage.

![Graph showing the impact of charge leakage over time.](image-url)
A Solution to Charge Leakage

- **Keeper** compensates for the charge lost due to the pull-down leakage paths.

Same approach as level restorer for pass transistor logic
Charge stored originally on $C_L$ is redistributed (shared) over $C_L$ and $C_A$ leading to static power consumption by downstream gates and possible circuit malfunction.

When $\Delta V_{out} = - V_{DD} \left( \frac{C_a}{C_a + C_L} \right)$ the drop in $V_{out}$ is large enough to be below the switching threshold of the gate it drives causing a malfunction.
Charge Sharing Example

What is the worst case voltage drop on y? (Assume all inputs are low during precharge and that all internal nodes are initially at 0V.)

\[ y = A \oplus B \oplus C \]

\[ C_y = 50 \text{fF} \]

\[ C_a = 15 \text{fF} \]

\[ C_b = 15 \text{fF} \]

\[ C_c = 15 \text{fF} \]

\[ C_d = 10 \text{fF} \]
Charge Sharing Example

What is the worst case voltage drop on \( y \)? (Assume all inputs are low during precharge and that all internal nodes are initially at 0V.)

\[ V_{\text{out}} = -V_{\text{DD}} \left( \frac{(C_a + C_c)}{(C_a + C_c + C_y)} \right) \]

\[ = -2.5V \times \left( \frac{30}{30+50} \right) = -0.94V \]
Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)
Issues in Dynamic Design: Backgate Coupling

- Susceptible to crosstalk due to 1) high impedance of the output node and 2) backgate capacitive coupling
  - Out2 capacitively couples with Out1 through the gate-source and gate-drain capacitances of M4
Backgate Coupling Effect

- Capacitive coupling means $Out_1$ drops significantly so $Out_2$ doesn’t go all the way to ground.
Issues in Dynamic Design: Clock Feedthrough

- A special case of backgate capacitive coupling between the clock input of the precharge transistor and the dynamic output node.

Coupling between Out and CLK input of the precharge device due to the gate-drain capacitance. So voltage of Out can rise above $V_{DD}$. The fast rising (and falling edges) of the clock couple to Out.
Clock Feedthrough

Clock feedthrough

CLK

In1

In2

In3

In4

CLK

Out

Clock feedthrough

In & CLK

Out

Clock feedthrough

Voltage

0  0.5  1

Time, ns

-0.5  0.5  1

Sp11 CMPEN 411 L15 S.26
Only a single $0 \rightarrow 1$ transition allowed at the inputs during the evaluation period!
Domino Logic

CLK $\rightarrow M_p$

$1 \rightarrow 1$

$1 \rightarrow 0$

$\rightarrow$

PDN

CLK $\rightarrow Me$

CLK $\rightarrow M_p$

$0 \rightarrow 0$

$0 \rightarrow 1$

CLK $\rightarrow M_{kp}$

Out1

Out2
Why Domino?

Like falling dominos!
Domino Manchester Carry Chain

CLK

P0

P1

P2

P3

Ci,0

G0

G1

G2

G3

C_{i,4}

CLK

CLK

Sp11  CMPEN 411  L15  S.30
Domino Zero Detector

How would you build it in static CMOS?
Domino Comparator

CLK

A3 A2 A1 A0

Out

B3 B2 B1 B0

Sp11 CMPEN 411 L15 S.32
Properties of Domino Logic

- Only non-inverting logic can be implemented, fixes include:
  - can reorganize the logic using Boolean transformations
  - use differential logic (dual rail)
  - use np-CMOS (zipper)

- Very high speed
  - $t_{\text{PHL}} = 0$
  - static inverter can be optimized to match fan-out (separation of fan-in and fan-out capacitances)
Due to its high-performance, differential domino is very popular and is used in several commercial microprocessors!
Other Domino Variations

- Multiple output domino logic – exploits the fact that certain outputs are subsets of other outputs to generate a number of logic functions in a single gate.

- Compound domino
np-CMOS (Zipper)

Only $0 \to 1$ transitions allowed at inputs of PDN
Only $1 \to 0$ transitions allowed at inputs of PUN
np-CMOS Adder Circuit

- Sum0
- Sum1
- A0
- B0
- C0
- A1
- B1
- C1
- CLK
- !CLK
- !A
- !B
- !C
- !CLK
- !A1
- !B1
- !C1
- 0 → x
- 1 → x
- Sp11 CMPEN 411 L15 S.37
DCVS Logic

PDN1 and PDN2 are mutually exclusive
DCVS Logic (Differential Cascade Voltage Switch)

PDN1 and PDN2 are mutually exclusive
DCVSL Example
How to Choose a Logic Style

- Must consider ease of design, robustness (noise immunity), area, speed, power, system clocking requirements, fan-out, functionality, ease of testing

4-input NAND

<table>
<thead>
<tr>
<th>Style</th>
<th># Trans</th>
<th>Ease</th>
<th>Ratioed?</th>
<th>Delay</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comp Static</td>
<td>8</td>
<td>1</td>
<td>no</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>CPL*</td>
<td>12 + 2</td>
<td>2</td>
<td>no</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>domino</td>
<td>6 + 2</td>
<td>4</td>
<td>no</td>
<td>2</td>
<td>2 + clk</td>
</tr>
<tr>
<td>DCVSL*</td>
<td>10</td>
<td>3</td>
<td>yes</td>
<td>1</td>
<td>4</td>
</tr>
</tbody>
</table>

* Dual Rail

- Current trend is towards an increased use of complementary static CMOS: design support through DA tools, robust, more amenable to voltage scaling.
Itanium 2 Domino Circuitry

- Integer execution unit
- Multimedia execution unit
- 2 Floating point units
- Register Files
- Out of order control issue logic

What is Soft Error

- Soft errors are circuit errors caused due to excess charge carriers induced primarily by external radiations.
- These errors cause an upset event but the circuit itself is not damaged.
- Same a SEU (single event upset)
Soft Errors

- The Phenomena

A particle strike

Current

n channel

p substrate

B
Soft Errors

- The Phenomena

A particle strike

Bit Flip !!!

1→0

0→1

A particle strike

Sp11  CMPEN 411  L15  S.45
What cause Soft Errors?

- At ground level, there are three major contributors to Soft errors.
  1. Cosmic Ray induced neutrons
  2. Alpha particles emitted by decaying radioactive impurities in packaging or interconnect materials.
  3. Neutron induced $^{10}\text{B}$ fission which releases a Alpha particle and $^7\text{Li}$
Evidence of Cosmic Ray Strikes

- Documented strikes in large servers found in error logs

- **Sun Microsystems, 2000**
  - Cosmic ray strikes on L2 cache with no error detection or correction
    - caused Sun’s flagship servers to suddenly and mysteriously crash!
  - Companies affected
    - Baby Bell (Atlanta), America Online, Ebay, & dozens of other corporations
    - Verisign moved to IBM Unix servers (for the most part)
Reactions from Companies

- **Fujitsu SPARC in 130 nm technology**
  - 80% of 200k latches protected with parity
  - compare with very few latches protected in Mckinley
  - ISSCC, 2003

- **IBM declared 1000 years system MTBF as product goal**
  - very hard to achieve this goal in a cost-effective way
Soft errors become hard truth for logic

By Ron Wilson David Lammers, EE Times
May 03, 2004 (9:39 AM EDT)
URL: http://www.eetimes.com/article/showArticle.jhtml?articleId=19400052

Phoenix — Those nasty neutrons that have plagued memory chip designers for the past two decades are now giving logic designers a headache, too. But while error correction coding has reduced soft-error rates (SERs) in DRAMs and SRAMs, no such quick fix exists for logic, and all current solutions involve extra cost and a drag on performance.

"Logic SER may become as significant as SRAM error rates," predicted Hans Stork, the chief technology officer at Texas Instruments Inc. (Dallas), in a keynote speech here last week at the International Reliability Physics Symposium.

Soft errors in logic devices are a growing concern for mission-critical systems such as servers, automotive ICs and networking equipment. Logic chip vendors already are working with system customers on ways to guard against the effects of cosmic rays and alpha particles emitted from packaging.

However, reliability engineers at last week’s symposium said no easy solutions exist.

In the case of ASIC designs, the implications are different and the countermeasures reach deeper into the system design.
Space redundancy: Redundant Logic

Logic 1

Logic 2

Voter

Logic 3

Point of failure!!
Next Lecture and Reminders

- Next lecture
  - Timing metrics, static sequential circuits
    - Reading assignment – Rabaey, et al, 7.1-7.2