Heads up

- This lecture
  - Pass transistor logic
    - Reading assignment – Rabaey, et al, 6.2.3

- Next lecture
  - MOS transistor dynamic behavior
    - Reading assignment – Rabaey, et al, 3.2.3 & 3.3.3-3.3.5
  - Wiring capacitance
    - Reading assignment – Rabaey, et al, 4.1-4.3.1
Review: Static Complementary CMOS

- High noise margins
  - $V_{OH}$ and $V_{OL}$ are at $V_{DD}$ and GND, respectively

- Low output impedance, high input impedance

- No static power consumption
  - Never a direct path between $V_{DD}$ and GND in steady state

- Delay a function of load capacitance and transistor on resistance

- Comparable rise and fall times (under the appropriate relative transistor sizing conditions)

PUN and PDN are dual logic networks
**Review: Static Complementary CMOS**

- **Question:**

Why PUN use only PMOS and PDN use only NMOS?

**ANSWER:**

NMOS transistors pass a ______ 0 but a ______ 1

PMOS transistors pass a ______ 1 but a ______ 0

PUN and PDN are dual logic networks
NMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- NMOS switch closes when the gate input is _____

X = Y if ______

X = Y if ______

- Remember - NMOS transistors pass a _____ 0 but a _____ 1
PMOS Transistors in Series/Parallel

- Primary inputs drive both gate and source/drain terminals
- PMOS switch closes when the gate input is low

\[ \text{X} = \text{Y} \text{ if } \underline{\text{__________}} \]

\[ \text{X} = \text{Y} \text{ if } \underline{\text{__________}} \]

- Remember - PMOS transistors pass a _____ 1 but a _____ 0
Pass Transistor (PT) Logic

- Gate is ______ – a path exists to both supply rails under all circumstances
- ______ transistors instead of 2N (for CMOS)
- No static power consumption
- Ratioless
- Bidirectional (versus undirectional)
Pure PT logic is not regenerative - the signal gradually degrades after passing through a number of PTs (can fix with static CMOS inverter insertion)
Differential PT Logic (DPL/CPL)

Why NFET?
CPL Properties

- **Differential** so complementary data inputs and outputs are always available (so don’t need extra inverters)
- Still static, since the output defining nodes are always tied to $V_{DD}$ or GND through a low resistance path
- Design is **modular**; all gates use the same topology, only the inputs are permuted.
- Simple XOR makes it attractive for structures like **adders**
- Fast (assuming number of transistors in series is small)
- Additional routing overhead for complementary signals
CPL Full Adder

A
B
Cin

!Sum

A
B
Cin

Sum

A
B
Cin

!Cout

A
B
Cin

Cout
CPL Full Adder
NMOS Only PT Driving an Inverter

\[ V_x = \_\_ \_ \_ \_ \_ \_ \]

- \( V_x \) does not pull up to \( V_{DD} \), but ________

- Threshold voltage drop causes static power consumption (\( M_2 \) may be weakly conducting forming a path from \( V_{DD} \) to GND)

- Notice \( V_{Tn} \) increases for pass transistor due to body effect (\( V_{SB} \))
Voltage Swing of PT Driving an Inverter

- **Body effect** – large \( V_{SB} \) at \( x \) - when pulling high (\( B \) is tied to GND and \( S \) charged up close to \( V_{DD} \))

- So the voltage drop is even worse

\[
V_x = V_{DD} - (V_{Tn0} + \gamma(\sqrt{|2\phi_f| + V_x} - \sqrt{|2\phi_f|}))
\]
Cascaded NMOS Only PTs

Swing on $y = V_{DD} - V_{Tn1} - V_{Tn2}$

Swing on $y = V_{DD} - V_{Tn1}$

- Pass transistor gates should never be cascaded as on the left
- Logic on the right suffers from static power dissipation and reduced noise margins
Solution 1: Level Restorer

- Full swing on $x$ (due to Level Restorer) so no static power consumption by inverter
- No static backward current path through Level Restorer and PT since Restorer is only active when $A$ is high
- For correct operation $M_r$ must be sized correctly (ratioed)
Transistors Level Restorer Circuit Response

- $W/L_n = 0.50/0.25$
- $W/L_1 = 0.50/0.25$
- $W/L_r = 1.50/0.25$
- $W/L_r = 1.75/0.25$
- $W/L_r = 1.50/0.25$
- $W/L_r = 1.25/0.25$

Node $x$ never goes below $V_M$ of inverter so output never switches.

- Restorer has speed and power impacts: increases the capacitance at $x$, slowing down the gate; increases $t_r$ (but decreases $t_f$)
Solution 2: Multiple $V_T$ Transistors

- Technology solution: Use (near) zero $V_T$ devices for the NMOS PTs to eliminate most of the threshold drop (body effect still in force preventing full swing to $V_{DD}$)

![Diagram showing low $V_T$ transistors and sneak path]

- Impacts static power consumption due to subthreshold currents flowing through the PTs (even if $V_{GS}$ is below $V_T$)
Solution 3: Transmission Gates (TGs)

- Most widely used solution

- Full swing bidirectional switch controlled by the gate signal C, A = B if C = 1
Solution 3: Transmission Gates (TGs)

- Most widely used solution

![Diagram of transmission gate](image)

- Full swing bidirectional switch controlled by the gate signal $C$, $A = B$ if $C = 1$, minimum size (ratioless)
TG Multiplexer

\[ F = !(\text{In}_1 \cdot S + \text{In}_2 \cdot \overline{S}) \]
Transmission Gate XOR

How many FETs for CMOS implementation? 10-12
Transmission Gate XOR

\[ A \oplus B \]

\[ A \cdot \overline{B} \]

\[ B \cdot \overline{A} \]

an inverter

Sp09 CMPEN 411 L07 S.23
How many transistors?
Differential TG Logic (DPL)

AND/NAND

F = A \oplus B

F = A \land B

XOR/XNOR

F = A \oplus B

F = A \land B

Sp09  CMPEN 411  L07  S.25
6-transistor SRAM Storage Cell

Will cover how the cell works in detail later
MOS OR ROM Cell Array

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<thead>
<tr>
<th></th>
<th>BL(0)</th>
<th>BL(1)</th>
<th>BL(2)</th>
<th>BL(3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
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</tr>
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<td>1</td>
<td>1</td>
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0 \rightarrow 1 \quad \text{WL(0)}

0 \rightarrow 1 \quad \text{WL(1)}

0 \rightarrow 1 \quad \text{WL(2)}

0 \rightarrow 1 \quad \text{WL(3)}

\begin{itemize}
  \item predischARGE
  \item 1 \rightarrow 0
\end{itemize}
Next Lecture and Reminders

Next lecture

- MOS transistor dynamic behavior
  - Reading assignment – Rabaey, et al, 3.2.3 & 3.3.3-3.3.5
- Wiring capacitance
  - Reading assignment – Rabaey, et al, 4.1-4.3.1