CMPEN 411
VLSI Digital Circuits
Spring 2009

Lecture 06: Static CMOS Logic

Review: CMOS Process at a Glance

- Define active areas
- Etch and fill trenches
- Implant well regions
- Deposit and pattern polysilicon layer
- Implant source and drain regions and substrate contacts
- Create contact and via windows
- Deposit and pattern metal layers

- One full photolithography sequence per layer (mask)
- Built (roughly) from the bottom up:
  4 metal
  2 polysilicon exception!
  3 source and drain diffusions
  1 tubs (aka wells, active areas)
CMOS Circuit Styles

- **Static complementary CMOS** - except during switching, output connected to either $V_{DD}$ or GND via a low-resistance path
  - high noise margins
    - full rail to rail swing
    - $V_{OH}$ and $V_{OL}$ are at $V_{DD}$ and GND, respectively
  - low output impedance, high input impedance
  - no steady state path between $V_{DD}$ and GND (no static power consumption)
  - delay a function of load capacitance and transistor resistance
  - comparable rise and fall times (under the appropriate transistor sizing conditions)

- **Dynamic CMOS** - relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes
  - simpler, faster gates
  - increased sensitivity to noise
**Static Complementary CMOS**

- Pull-up network (PUN) and pull-down network (PDN)

V\(_{DD}\)

- **PMOS transistors only**
  - pull-up: make a connection from V\(_{DD}\) to F when \(F(In_1, In_2, \ldots, In_N) = 1\)

- **NMOS transistors only**
  - pull-down: make a connection from F to GND when \(F(In_1, In_2, \ldots, In_N) = 0\)

**Question**: How many transistors are used to implement \(N\)-input function \(F(In_1, In_2, \ldots, In_N)\)?
Construction of PDN

- NMOS devices in series implement a NAND function

\[ \overline{A \cdot B} \]

- NMOS devices in parallel implement a NOR function

\[ \overline{A + B} \]
Dual PUN and PDN

- PUN and PDN are dual networks
  - DeMorgan’s theorems

\[
A + B = \overline{A \cdot B} \quad \text{and} \quad \overline{A + B} = \overline{A} \cdot \overline{B} \\
A \cdot B = \overline{A + B} \quad \text{and} \quad \overline{A \cdot B} = \overline{A} + \overline{B}
\]

- a parallel connection of transistors in the PUN corresponds to a series connection of the PDN

- Complementary gate is naturally inverting (NAND, NOR, AOI, OAI)

- Number of transistors for an N-input logic gate is 2N
CMOS NAND

A • B

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<th>A</th>
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<th>F</th>
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CMOS NOR

\[
\begin{array}{c}
A + B \\
\hline
B \\
A \\
\hline
\end{array}
\]

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Complex CMOS Gate

OUT = !(D + A \cdot (B + C))
Complex CMOS Gate

\[ \text{OUT} = \neg (D + A \cdot (B + C)) \]
Naturally inverting, implementing only functions such as NAND, NOR, and XNOR in a single stage.

PMOS transistors only
- pull-up: make a connection from $V_{DD}$ to F when $F(In_1, In_2, ... In_N) = 1$

NMOS transistors only
- pull-down: make a connection from F to GND when $F(In_1, In_2, ... In_N) = 0$

Question 1: why PUN are PMOS only and PDN are NMOS only?
Threshold Drops

PUN

PDN
Threshold Drops

PUN

\[ V_{DD} \]

\[ 0 \rightarrow V_{DD} \]

\[ C_L \]

PDN

\[ V_{DD} \rightarrow 0 \]

\[ V_{GS} \]

\[ V_{DD} \rightarrow |V_{Tp}| \]
Standard Cell Layout Methodology

What logic function is this?
OAI21 Logic Graph

\[ X = \neg(C \cdot (A + B)) \]

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Two Stick Layouts of \(!{(C \cdot (A + B))}\)

crossover requiring vias

uninterrupted diffusion strip
Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph.
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.

For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same).
Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph.
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.

- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same).
OAI22 Logic Graph

\[ X = !(A+B)\cdot(C+D) \]
Some functions have no consistent Euler path like $x = !(a + bc + de)$ (but $x = !(bc + a + de)$ does!)
XNOR/XOR Implementation

- How many transistors in each?
- Can you create the stick transistor layout for the lower left circuit?
VTC is Data-Dependent

The threshold voltage of $M_2$ is higher than $M_1$ due to the body effect ($\gamma$)

$V_{Tn1} = V_{Tn0}$

$V_{Tn2} = V_{Tn0} + \gamma(\sqrt{|2\phi_F| + V_{int}} - \sqrt{|2\phi_F|})$

since $V_{SB}$ of $M_2$ is not zero (when $V_B = 0$) due to the presence of $C_{int}$
Static CMOS Full Adder Circuit
Static CMOS Full Adder Circuit (page 565)

\[ C_{out} = AB + BC_{in} + AC_{in} \]
\[ \text{Sum} = ABC_{in} + !C_{out}(A+B+C_{in}) \]

\[ C_{out} = C_{in} \land (A \lor B) \lor (A \land B) \]
\[ \text{Sum} = !C_{out} \land (A \lor B \lor C_{in}) \lor (A \land B \land C_{in}) \]

\# transistors = 24+4
Two chips you are seeing today

PowerPC 750 Copper

Microprocessor

ASIC (Application Specific IC)
Standard Cell Library

NAND

INV
Standard Cell Library
The design flow

VHDL (decoder.vhd) → Simulation → Synthesis

Standard Cell Lib

Verilog netlist (decoder.v)

Place/Route

Physical layout (decoder.cif) → Fab

Silicon Ensemble
The IBM ASIC Design Flow
Next Lecture and Reminders

Next lecture

- Pass transistor logic
  - Reading assignment – Rabaey, et al, 6.2.3