Scalable Vectorless Power Grid Current Integrity Verification

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ABSTRACT
To deal with the growing phenomenon of electromigration (EM), power grid current integrity verification becomes indispensable to designing reliable power delivery networks (PDNs). Unlike previous works that focus on vectorless voltage integrity verification of power grids, in this work, for the first time we present a scalable vectorless power grid current integrity verification framework. By taking advantage of multilevel power grid verifications, large-scale power grid current integrity verification tasks can be achieved in a very efficient way. Additionally, a novel EM-aware geometric power grid reduction method is proposed to well preserve the similar geometric and electrical properties of the original grid on the coarse-level power grids, which allows to quickly identify the potential “hot wires” that may carry greater-than-desired currents in a given power grid design. The proposed multilevel power grid verification algorithm provides flexible tradeoffs between the current integrity verification cost and solution quality, while the desired upper/lower bounds for worst case currents flowing through a wire can also be computed efficiently. Extensive experimental results show that our current integrity verification approach can efficiently handle very large power grid designs with good solution quality.

Categories and Subject Descriptors
B.7.2 [Design Aids]: simulation—Integrated Circuits

General Terms
Performance, Algorithms, Verification

Keywords
Power grid, electromigration, multigrid

1. INTRODUCTION

Power grid electromigration (EM) verification tries to find the worst current densities under a given temperature, which can be achieved by finding the worst current flowing through a wire. Efficient current integrity verification methods are key to designing reliable power delivery networks (PDNs) for nowadays nanometer integrated circuits (ICs) designs.

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In the past decade, to avoid prohibitively high cost of traditional vector-based power grid voltage integrity verification methods that rely on running numerous power grid simulations, a variety of vectorless verification techniques has been proposed [1–5].

In this work, we show that vectorless power grid current integrity verification problems share very similar properties as the original multilevel PDE-constrained optimization technique [6]. We also propose a multilevel vectorless power grid current integrity verification method that takes advantages of fast EM-aware power grid reduction method and circuit adjoint sensitivity analysis [7]. Our approach achieves desired scalability by attacking a set of power grid verification problems from the coarsest to finest grid levels, and more importantly, allowing to flexibly trade off the solution quality and computational efficiency by effectively controlling the number of current sources included in the linear program (LP). In this work, although we mainly focus on DC current verification problems, the proposed approach can potentially be extended to handle transient current verification problems. The major contributions of this work include:

1. Based on the key ideas of multilevel PDE-constrained optimization methods [6], we propose a novel multilevel vectorless power grid current integrity verification method that scales well with large power grid designs and provides insightful upper/lower bounds for the verification solutions.

2. We present a novel EM-aware power grid reduction technique to facilitate efficient coarse-level power grid verifications. To further improve the solution quality obtained on coarse-level grids, an iterative coarse grid correction scheme is introduced that enables the coarse grids to match important electrical behaviors with the original power grid.

3. We propose to quickly perform a series of coarse-level power grid current verifications and subsequently reuse part of the prior coarse-grid verification results in the fine-grid verification. Such a multilevel verification approach can quickly identify the “hot wires” on the coarsest-level grid, while incremental solution refinements can be successively performed on the finer to finest grids, which effectively trades off the overall verification cost and the final solution quality.

The rest of this paper is organized as follows. In Section 2, we briefly review the power grid modeling and analysis as well as prior vectorless power grid verification methods. In Section 3, we describe the proposed multilevel power grid current integrity verification approach in details. Section 4 demonstrates extensive experimental results of a variety of
power grid verifications to validate the proposed approach, which is followed by the conclusion of this work in Section 5.

2. BACKGROUND

2.1 Power Grid Modeling and Analysis

DC analysis for a power grid with $n$ nodes can be performed using nodal analysis (NA) as follows [8]:

$$Gx = b,$$

where $G \in \mathbb{R}^{n \times n}$ is the conductance matrix that includes all interconnected resistors, $x \in \mathbb{R}^{n \times 1}$ is a vector including all node voltage unknowns, and $b \in \mathbb{R}^{n \times 1}$ denotes the right hand side (RHS) that includes information on excitation sources and boundary conditions.

2.2 Vectorless Power Grid Voltage Verification Approaches

The concept of vectorless power grid verification has been presented in [4]. It has been shown that power grid voltage integrity verification is equivalent to solving the following LPs [2]:

$$\text{maximize : } v_i = e_i^T G^{-1} b, \text{ for } i = 1, ..., n,$$

subject to the local and global current constraints:

$$b^L \leq b \leq b^U, 0 \leq Qb \leq b_g,$$

where $e_i$ denotes a vector in which the $i$-th element is 1 and others are 0, $G$ is an $M$-matrix whose inverse only includes non-negative elements, $b^L_i$ and $b^U_i$ denote the upper and lower bounds for current source $b_i$, respectively. $Q$ is a matrix with only 1s and 0s describing the global current constraints. The local and global current constraints for different grid levels can be obtained from realistic circuit design information or early design specifications, such as the power consumption, voltage, and switching activities [2–4,9].

Recent popular works on power grid voltage integrity verification adopt a modified sparse approximate inverse (SPAI) technique to compute the approximate matrix inverse of $G$ matrix using least square (LS) optimizations [2,9]. Subsequently, they formulate the voltage integrity verification problems as LPs with the reduced sets of current sources according to the approximate matrix inverse. This technique has been shown to produce good results for power grid verification when grid sizes are not very large (during early-stage power grid designs). However, the SPAI technique may not scale comfortably to handle large grid verification problems (as shown in [2]).

3. SCALABLE POWER GRID CURRENT INTEGRITY VERIFICATION

3.1 Vectorless Power Grid Current Integrity Verification

To identify potential EM failures for a power grid design, we need to find the maximum current density of each wire. In this work, we assume that wire dimensions are known in advance, then the power grid current verification task is to find the maximum current flowing through each power grid wire under local and global current constraints. Using the same notations as (2), we propose the following LPs to find the maximum voltage difference between nodes $i$ and $j$, which is equivalent to finding the maximum current that flows between node $i$ and node $j$ through the wire with a resistance $R_{i,j}$ for power grid current integrity verification:

$$\text{maximize : } (v_i - v_j) = (e_i - e_j)^T E^{-1} b, \text{ for all grid wires,}$$

subject to the local and global current constraints:

$$b^L \leq b \leq b^U, 0 \leq Qb \leq b_g.$$

It should be noted that since any current flowing through a wire may have two directions, so a same set of LPs can be applied to find maximum voltage difference between nodes $j$ and $i$. Compared to prior power grid voltage integrity verification problem, instead of finding the maximum voltage drops across all nodes, current verification aims to find the maximum voltage differences between two nodes connected through a resistive wire. Consequently, extremely high computational cost is expected considering large-scale power grid analysis and the LP with a large number of variables. In this work, we will attack the DC current verification problem, whereas more general dynamic verification problems will be investigated in our future work.

3.2 Overview of Our Approach

Based on the ideas of traditional PDE-constrained multi-grid optimization methods (see the supplementary materials for more details), we propose a novel multilevel power grid current integrity verification framework that includes the following steps:

1. Create replicas of coarsest to finest grid problems based on the original power grid design using the proposed EM-aware power grid reduction method [8,10].

2. Construct local and global current constraints for coarse level grids using the restriction operations depicted in Fig. 1.

3. Perform global current integrity verifications: find the worst wire currents on the coarsest grid level using the proposed LP formulation (in Section 3.1) for all the wires. Identify the top wires (regions) with largest current densities for finer grid verifications, and store their verification results (excitation current distributions).

4. Perform refined verifications: verify the corresponding wires (regions) that have been identified on the coarser grids with partial solution obtained in the previous coarse grid verification. The partial solution can be obtained using the prolongation operation depicted in Fig. 2.
3.3 EM-Aware Power Grid Reduction for Coarse Grid Generation

Power grid reduction methods can be adopted to create coarse-level grids for power grid verifications. For instance, during power grid voltage integrity verifications, since the nodes (regions) that exhibit the worst voltage drops can be similarly preserved on the reduced (coarse) grids, the coarse-grid verification result can effectively facilitate fine-grid verification tasks. However, for power grid current integrity verifications, traditional power grid reduction methods may cause troubles in revealing potential “hot wires” on the reduced grid if the geometric properties of the original power grid layout are not preserved after the reduction. To better preserve the geometric properties of the original power grids, one can apply geometric multigrid reduction methods to greatly reduce the original large power grids into much smaller ones through node and wire aggregations [8, 11]. Subsequently, the reduced grids can be used during coarse-level power grid current integrity verifications, which are usually much cheaper since solving the linear systems of equations in (1) and the LP problems in (4) will involve much fewer variables than solving the original problem.

However, one major drawback of the existing geometric multigrid reduction methods [8, 11] is that the reduction error can not be easily controlled. As a result, if the coarse (reduced) grids can not well preserve the electrical properties of the original power grids, significant errors can be introduced during the coarse-grid verification procedures, which may further influence the fine-grid verification accuracy. In this work, based on our recent research [10] we propose an EM-aware power grid reduction technique that combines the prior geometric multigrid reduction procedure with a coarse grid correction scheme to significantly improve the power grid reduction accuracy. The basic idea of our approach is to scale up/down some of the power grid wires such that the new coarse grid can well capture the key electrical behaviors, such as the power dissipations (a.k.a Joule heat) and voltage drops, of the original power grid.

Considering nowadays flip-chip power grid designs, locality effects [12] are typically significant, which allows to partition and analyze the small power grid blocks separately. To more intuitively describe the coarse grid correction scheme, we will first neglect the complicated coupling effects between power grid blocks in the following discussion. Then the power dissipation of a power grid block can be computed by

$$ P_{\text{Joule}} = x^T G x, $$

where $x = G^{-1} b$, which is followed by

$$ P_{\text{Joule}} = b^T G^{-1} b = b^T G^{-1} b. $$

So if we size up all the wires in the block by a block scaling factor $\tau$, the block voltage drops after the wire sizing become $x' = G^{-1} b/\tau$, while the block power dissipation becomes

$$ P'_{\text{Joule}} = b^T G^{-1} b/\tau = P_{\text{Joule}}/\tau. $$

The above derivations indicate that we can use the block power dissipation (voltage drop) ratios of the coarse grid and the original grid to determine the block scaling factors $\tau$ that can be further used to scale up/down the coarse grid wires.

Considering the couplings between power grid blocks, the coarse grid correction problem can be formulated into the following nonlinear optimization problem that tries to best match the original grid’s block power dissipations as well as block average voltage drops on the coarse grid:

$$ \text{minimize : } \phi (\tau_1, \ldots, \tau_m) = \sum_{i=1}^{m} \left( x_{ri}^T G_{ri} x_{ri} \tau_i - x_{ri}^T G_{ri} x_{ri} \right)^2 + \alpha \sum_{i=1}^{m} \left( \frac{|x_{ri}|}{n_{ri}} - \frac{|x_{ri}'|}{n_{ri}'} \right)^2 $$

subject to the constraint:

$$ G_{ri} (\tau_1, \ldots, \tau_m) \begin{bmatrix} x_{r1} \\ \vdots \\ x_{rm} \end{bmatrix} = b_r, G \begin{bmatrix} x_1 \\ \vdots \\ x_m \end{bmatrix} = b, $$

where $G_{ri}$ ($G_i$) is the conductance matrix of the coarse (fine) grid block $i$, $m$ is the number of blocks, $\tau_i$ for $i = 1, \ldots, m$ are the block scaling factors to be found, $\alpha$ is a weighting coefficient, and $n_{ri}$ ($n_i$) is the number of nodes in the coarse (fine) grid block. It should be noted that the coarse grid conductance matrix $G_{ri}$ ($\tau_1, \ldots, \tau_m$) is now parameterized, and the block solutions $x_{ri}$ will become a function of $\tau_1, \ldots, \tau_m$.

However, there is no efficient method for solving the above nonlinear optimization problems. Fortunately, for flip-chip power grids, locality effects enable us to relax the above optimization problem, which allows to apply the following iterative coarse grid corrections (as illustrated in Fig. 3):

1. Partition the coarse and the original grid into multiple power grid blocks such that each block includes a few VDD/GND pads.
2. Perform DC analysis for the original grid and the reduced (coarse) grid, and compute each block’s power dissipation and average voltage drop.
3. Size up/down the block wires in the coarse grid using the weighted block scaling factor $\tau_i = \left( \frac{x_{ri}'}{x_{ri}} \right)^\omega \left( \frac{|x_{ri}|}{n_{ri}} \right) (1 - \omega)$.
4. Repeat steps 3 and 4 until convergence. Output the updated coarse grid circuit.

In step 4, $\omega$ is a weighting coefficient between 0 and 1. We have implemented the above coarse grid correction scheme...
and observed that solution errors can be reduced by over 3X when compared with the original coarse grid obtained using geometric multigrid reduction scheme [8,11] (see the supplementary materials for power grid reduction results).

It should be noted that unlike prior power grid reduction methods that can only preserve the electrical properties of the original grid, the proposed EM-aware power grid reduction scheme can also preserve the geometric properties of the original power grid in that the wire dimensions in the reduced power grid can be easily calculated after the reduction process. For example, since the coarse grid has the same geometric (lateral) dimensions (width and length) as the original grid but much fewer nodes/wires. Consider a resistor $R_{ij}$ between nodes $i$ and $j$ in the reduced grid. $R_{ij}$ can be considered as an equivalent wire resistor for a set of wires coming from possibly multiple metal layers of the original power grid. Since the distance between nodes $i$ and $j$ is preserved on the reduced grid, one can easily compute the effective wire cross-section area based on $R_{ij}$, and therefore estimate the wire current density. This nice property allows to quickly estimate the wire current densities even for the coarse level grids. As a result, the coarse-grid current integrity verification results can effectively facilitate identifying the worst current densities and “hot wires” in the original power grid.

### 3.4 Critical Regions for Linear Programs

To further reduce the current verification cost in the LP (4), the number of current variables should be well controlled. However, power grid current verification problems usually involve hundreds of thousands of current sources, which may take excessively long CPU time when using standard LP solvers. To effectively control the number of variables in LPs, we first define the critical region $C_{cert}$ based on power grid electrical properties such as the wire current (voltage difference across the wire) sensitivities w.r.t. the underlying current sources. $C_{cert}$ includes the most critical current sources that will significantly contribute to the wire current of our interest, such as the one shown in Fig. 4. $C_{cert}$ can be obtained by estimating the amplitudes of the wire current sensitivities w.r.t. all current sources. For instance, if we are given a threshold sensitivity value $s_{th}$ or normalized sensitivity value $\epsilon_{cert} = s_{th}/s_{max}$ where $s_{max}$ is the maximum sensitivity value of all current sources, $C_{cert}$ can be obtained in the following way: if a current source has a sensitivity value greater than the threshold value $s_{th}$, then it is included into $C_{cert}$ and thus the LP for power grid current integrity verification, since its current value change will substantially influence the worst current density of the wire/region under verification. On the other hand, if a current source’s sensitivity value is much smaller than the threshold value, it can be safely excluded from $C_{cert}$ as it will not be an important variable for finding the worst current densities. In this work, we set $\epsilon_{cert}$ to be around $5e-3$, which allows to include much fewer current sources (10% of the total currents) into the LP without loss of much accuracy.

Since power grid current sensitivities can be efficiently computed using adjoint sensitivity analysis [7] by reusing the matrix factors (from one-time Cholesky or LU decomposition) of the conductance matrix $G$, finding $C_{cert}$ is efficient. For instance, if we want to compute the wire current (voltage difference divided by the resistance) sensitivity used in current integrity verification (4), we simply set $b = e_i - e_j = [0, ..., 1, 0, ..., -1, ..., 0]^T$ to compute the sensitivity vector $s$. $C_{cert}$ can be identified subsequently based on these sensitivity values on the original and coarse-level grids easily, as shown in Fig. 4.

Once the critical region $C_{cert}$ is determined, an LP can be formulated based on previous adjoint sensitivity analy- sis result, in which only the current sources that fall into the critical region $C_{cert}$ are considered during the verification. If a circuit block sits across the boundary of $C_{cert}$, the current sources of that circuit block should also be included into $C_{cert}$. Assume that the adjoint sensitivity vector $(s)$ is computed in advance, then the power grid current integrity verification (finding the worst voltage difference $v_{wst}$) for a specific wire within $C_{cert}$ can be formulated into the following LP:

$$
\text{maximize: } \bar{v}_{wst} = \sum_{v_{ij} \in C_{cert}} s_i b_i, \\
\text{subject to the local and global current constraints: } b^L \leq b \leq b^U, 0 \leq Qb \leq b_g.
$$

where $b^L$ and $b^U$ denote the upper and lower bounds for current sources $b$, and $Q$ is a matrix that includes the global current constraints. It should be noted that the proposed critical region verification approach based on power grid electrical properties such as adjoint sensitivity information will greatly reduce the number of current sources involved in the LP, resulting in much more efficient power grid verification. In our extensive experiments, we find that for the original power grid including only 10% (when using $\epsilon_{cert} = 5e-3$) of the current sources in LP will suffice for finding accurate worst case wire current densities.

### 3.5 Upper/Lower Bounds of Worst Currents

The proposed power grid current integrity verification also provides the lower and upper bounds of the worst wire currents. Since the current sources with small sensitivity values will not be included in the LP, the maximum extra voltage difference $v_e$ they may contribute can be approximately computed based on the total current and the sensitivity threshold $s_{th}$:

$$
v_e = \max_{\forall b_i \in C_{cert}} \left( \sum_{i=1}^{n} s_i b_i \right) \leq \max_{\forall b_i \in C_{cert}} \left( \sum_{i=1}^{n} s_{th} b_i \right) \leq s_{th} |b - b_p|_1,
$$

where $b_p$ is the vector that only includes the current sources in the critical region $C_{cert}$. We assume that $s_{th}$ is much smaller than the peak sensitivity values observed in $C_{cert}$, then the upper bound of the worst case voltage difference can be approximately computed by:

$$
v_{wst} \approx \bar{v}_{wst} + v_e \approx \bar{v}_{wst} + s_{th} |b - b_p|_1.
$$

From the above results, it can be concluded that the realistic worst case voltage difference $v_{wst}$ will approximately satisfy:

$$
\bar{v}_{wst} \leq v_{wst} \leq \bar{v}_{wst}.
$$

![Figure 4: Critical and non-critical regions for power grid current integrity verification.](image-url)
It should be noted that a larger threshold sensitivity value \( s_{th} \) will result in fewer current sources to be included in the LP thus less computational cost, but the upper and lower bounds of worst case voltage difference \( v_{wst} \) will also become more conservative (looser upper/lower bounds). On the contrary, if a smaller \( s_{th} \) is chosen, more current sources will be involved in LP that gives much tighter bounds for the worst case voltage difference. Fortunately, using the proposed method, tradeoffs between the computational cost and the final solution quality can be effectively achieved by choosing different threshold sensitivity values \( s_{th} \).

### 3.6 Power Grid Current Integrity Verification Algorithm

Once we have identified a few key “hot wires” or regions on the coarsest grid, the verification results can be interpolated (prolonged) to the finer grids to facilitate the next-level power grid verification (as shown in Fig. 2). Assuming that a “hot wire” has been identified after performing exhaustive current integrity verifications on the coarsest grid, and one would like to find the worst current densities of this wire on the finer to finest grids, the following issues should be addressed first: as we move from the coarsest grid to the finer grids, the number of decision variables (current sources) that fall into the critical region \( C_{crt} \) will grow dramatically, making the resultant LP increasingly expensive to solve. To take advantage of previous coarse-level grid verifications, we further define the finer-grid solution refinement step and updated critical region (denoted by \( C_{crt}^\prime \)).

Algorithm 1: Multilevel power grid current integrity verification for a “hotspot” wire.

**Input:** the local and global current constraints \( b^L, b^H \) and \( Q \) in (11), the original power grid netlist, the sensitivity scaling factor \( \beta > 1.0 \), and the mapping operators between fine and coarse grids \( V^H \) and \( V^L \), and the coarsest grid level \( K \).

**Output:** the current vector that results in the worst case voltage difference (current density) across the wire.

1: Initialization phase:
   a) Create the multilevel coarsest to finest grid models (level 0 to level \( K \) grids) [8,11].
   b) Set up their local and global current constraints \( b^L, b^H \) and \( Q \) for all grid levels based on the inter-grid operator \( V^H \) and \( V^L \).
   c) Perform coarse grid corrections described in Section 3.3 to improve the coarse grid solution quality.

2: Global verification phase for level \( K \) grid:
   a) Perform adjoint sensitivity analysis to compute sensitivity vector \( s^K \) w.r.t. current source \( b^K \).
   b) Identify \( C^K_{crt} \) based on sensitivity threshold \( \epsilon^K \).
   c) Set up LP solver to obtain the solution \( b^K_{wst} \) using (11).
   d) Compute the upper bounds by:
      \[ v^K_{wst} = \bar{V}^K_{wst} + \epsilon^K s^K_{max} b^K - b^K_p \mid_1. \]

3: Finer-grid solution refinement phase for finer to finest grids:
   a) for \((k=K-1; k > 0; k = -)\) do
   b) Interpolate coarser level \( k + 1 \) solution vector to level \( k \) grid by:
      \[ b^K_{wst} = \bar{V}^L_{k+1} b^{K+1}_{wst}. \]
   c) Perform adjoint sensitivity analysis.
   d) Determine the updated critical region \( C^K_{crt} \) for finer-grid solution refinement using sensitivity threshold \( \epsilon^K = \beta^{k+1} \).
   e) Set up LP solver using (11) to obtain the solution vector \( b^K_{wst} \) within the updated critical region \( C^K_{crt} \).
   f) For the current sources that fall outside \( C^K_{crt} \), reuse the interpolated coarse grid solution vector \( b^K_{wst} \).
   g) Compute the refined worst case current vector by:
      \[ b^K_{wst} = \bar{b}^K_{wst} + \bar{b}^K_{wst}. \]
   12: Return the final current verification results.

After finishing the global verification task on the coarsest grid for a specific wire, the current vector \( b^K_{wst} \) that results in the worst voltage difference across the wire can be interpolated to the finer grid for next-level power grid verification:

\[ b^H_{wst} = V^H_h b^K_{wst}, \]

where \( V^H_h \) denotes the inter-grid operator shown in Fig. 2 interpolating the coarse grid vector to the finer grid vector. Since the prolonged solution vector \( b^K_{wst} \) can be very close to the true solution \( b^K_{wst} \). This suggests that during the finer grid verification, instead of doing full-blown grid verification, we can relax the power grid verification problem by performing finer-grid solution refinement only within the updated critical region \( C^K_{crt} \) that is computed in a similar way as \( C^K_{crt} \) (a smaller region as shown in Fig. 4) by setting a larger sensitivity threshold value.

The proposed multilevel power grid current integrity verification algorithm has been described in Algorithm 1. The “hot wires” will be first identified through global verifications on the coarsest grid, and finer-grid solution refinements can be subsequently performed to compute the worst case current densities of the original grids.

### 4. EXPERIMENTAL RESULTS

Extensive experiments have been conducted to validate the proposed multilevel power grid current integrity verification approach that has been implemented using C++ and CUDA. The LP is solved by the solver proposed in [13], while the power grid adjoint sensitivities are computed using the GPU-based power grid simulator [8,14]. The hardware platform is a Linux PC with Intel Core 2 Quad CPU running at 2.66 GHz clock frequency with an NVIDIA GTX 285 GPU. All runtime results are measured in seconds. A set of flip-chip power grids are generated using the typical wire resistances as well as the current source distributions of industrial designs [15].

To build the LPs for power grid current verification, adjoint sensitivity analysis is first performed to identify the critical region \( C^K_{crt} \) by examining the sensitivity values. Next, current sources can be determined for the LP subsequently. In Fig. 5, we show the relative sensitivity distributions (scaled with the largest sensitivity value) in logarithmic scale for the level 2 grid of a power grid design. As discussed in Algorithm 1, once the power grid verification proceeds to the finer grid level, the updated critical region \( C^K_{crt} \) will shrink to a smaller one based on the scaling factor \( \beta \). Subsequently, the finer-grid refinement using LP solver will be performed considering the current sources in the updated critical region \( C^K_{crt} \) as shown in Fig. 4. It is also observed in our experiments that as the verification proceeds from the coarsest grid to the finest grid, more and more current sources have to be included into the LP when a fixed critical region is used, resulting in drastically increased computational cost. On the other hand, by introducing the gradually shrinking (updated) critical regions on the finer to finest grids, the number of variables involved in LPs can be effectively reduced, leading to much lower verification cost.

We show more comprehensive results of the proposed multilevel power grid current integrity verification method in Table 1. Different sets of sensitivity threshold values \( \epsilon^{glb} \) (threshold for global grid verifications on the coarsest grid) and scaling factors \( \beta \) (for finer grids) are used for all test cases. It is obvious that when using smaller \( \epsilon^{glb} \) and \( \beta \), the number of current source variables in the LP will be greater, which makes the overall verification more accurate but less efficient. It is also observed that when using \( \epsilon^{glb} = 5e^{-3} \) and \( \beta = 2 \), the upper bound of the worst case current can...
Table 1: Results of the proposed multilevel power grid current integrity verification. $N_{nodes}$, $N_{cur}$, and $N_{lev}$ are the numbers of power grid nodes, current sources of the finest grid, verification levels, respectively. $\epsilon_{glb}$ is the normalized threshold sensitivity for global verification, and $\beta$ is the sensitivity scaling factor. $T_{glb}$, $T_{ref}$ and $T_{tot}$ are the global verification time checking 1,000 wires on the coarsest grid, verification refinement time for verifying the top five candidate wires with worst current densities on the finer grids, and the total verification time. $Err$ is the relative error of the computed upper bound ($v_{wst}$) of worst case results compared with the solution obtained using $\epsilon_{glb} = 5\epsilon - 3$ and $\beta = 2$.

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6. REFERENCES


Supplementary Material

6.1 PDE-Constrained Multilevel Optimization

PDE-constrained multilevel optimization methods have been proposed to solve general nonlinear optimization problems which are governed by system of partial differential equations (PDEs) [6], which is shown as follows:

\[
\text{maximize: } F(p) = f(v(p), p),
\]

subject to the PDE constraint:

\[
S(v, p) = 0,
\]

where \( p \) can be a set of design variables or input variables, and \( S(v, p) \) describes a system of partial differential equations that relate the PDE's solution \( v \) with the input parameter \( p \). Since the linear system of equations for power grid analysis can be considered as a partial differential equation (PDE) [11], the the voltage vector \( v \) and RHS vector \( b \) in (1) can be considered as the model parameters \( v \) and \( p \) in (18), while the worst case voltage difference of two nodes sought in the power grid current verification formulation (4) can be considered as the objective function \( F(p) \).

Obviously, there are good similarities between the standard power grid verification problems and the aforementioned PDE-constrained optimization problems, though power grid verification usually solves an LP problem instead of a nonlinear problem. However, prior PDE-constrained multilevel optimization methods do not allow local and global inequality constraints, we cannot directly apply the multilevel optimization method to power grid verification problems. Fortunately, ideas behind traditional PDE-constrained multilevel optimization methods will benefit our power grid current verification problems. A brief introduction to typical PDE-constrained multilevel optimization procedures is described as follows.

Assume that the coarser to finer (finer to coarser) problem mapping operators \( V^h_1(V^h_2) \) for different grid levels have been previously defined. Then the conventional PDE-constrained multilevel optimization methods include the following key steps [6]:

- If on the coarsest level problem, maximize \( F_h(p_h) = f_h(v(p_h), p_h) \), with initial estimate \( p_h(0) \), to obtain \( p_h(1) \).
- Otherwise:
  1. Partially maximize \( F_H(p_H) \) with initial estimate \( p_H(0) \), to obtain \( p_H(1) \).
  2. Map the fine level problem solution to the coarse level problem by \( p_{h,1} = V^h_1 p_H \), and compute the gradient difference: \( s_h = \nabla F_h(p_{h,1}) - V^h_1 \nabla F_H(p_H) \).
  3. Recursively apply multilevel optimization with initial solution guess \( p_{h,1} \) to solve the following coarse problem: maximize \( F_h(p_h) = s_h^T p_h \), subject to the constraints: \( p_h^L \leq p_h \leq p_h^U \) to get a refined solution \( p_h(1) \).
  4. Compute the new search direction \( \epsilon_H = V^h_1(p_h(2) - p_h(1)) \), apply line search \( p_{h,2} = p_{h,1} + \alpha \epsilon_H \) and maximize \( F_H(p_H) \), with initial solution \( p_{H,2} \) to obtain \( p_H(1) \).

"Partially maximize" in Step 1) is similar to the smoothing operation in traditional multigrid algorithm for numerically solving PDE problems, while the line search phase improves solution at every optimization iteration. The extra bound constraint \( p_h^L \leq p_h \leq p_h^U \) has been introduced to improve the convergence. It is interesting to see that the above optimization framework adopts the multigrid V-cycle scheme (which is key for multigrid numerical solver), though other cycle formats such as the W-cycle or the full multigrid cycle can be applied in the similar manner.

6.2 Results of the EM-Aware Power Grid Reduction Method

In this section, we validate the EM-aware power grid reduction method proposed in Section 3.3 for a set of industrial power grid test cases [15]. The power grid analysis for the full grids and the reduced grids are performed on CPU-GPU platforms based on the iterative algorithms proposed in [8,14]. The hardware platform is a Linux PC with Intel Core 2 Quad CPU running at 2.66 GHz clock frequency with an NVIDIA GTX 285 GPU.

In Fig. 6 and Fig. 7, we show the results of the proposed iterative grid correction scheme for industrial test cases. As shown, after only 10 iterations, the maximum voltage errors can be reduced to a much smaller one when compared with the initial reduced power grid model errors (without grid corrections). In the last, we show the block scaling factors for an industrial power grid design in Fig. 8. As observed, the wires on reduced power grid have been modified drastically from the original reduced grid obtained by using the naive geometric multigrid reduction (element/node aggregation) method. This also indicates the necessity of the proposed iterative grid correction procedure for achieving more accurate EM-aware power grid reductions.
Figure 8: Block wire scaling factor distribution on the reduced grid. The factor $G_1/G_0$ is the ratio of block wire conductances before and after iterative block reduced grid corrections.