

Ing-Chao (Richard) Lin

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EDUCATION

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|--------------|--|------|
| Ph.D. | Computer Science and Engineering
The Pennsylvania State University (PSU)
Advisor: Dr. V. Narayanan
Dissertation: "System-level Power and Reliability Modeling" | 2007 |
| M.S. | Computer Science and Engineering
National Taiwan University (NTU) | 2001 |
| B.Ed. | Information and Computer Education
National Taiwan Normal University (NTNU) | 1997 |

RESEACH POSITIONS

- Research Assistant**, Computer Science and Engineering, PSU Jan. 2005-Aug. 2006
Jan. 2004-May 2004
- Created a transaction-based error characterization model for bus-based System-on-Chip and proposed a prediction model to predict system reliability with 92% accuracy
 - Constructed SystemC transaction-level models for the PCI Express IP core, and implemented power estimation functions for the transaction-level models
 - Created an automated tool flow to analyze NMOS and PMOS device degradation due to HCI (Hot Carrier Injection) and NBTI (Negative Biased Temperature Instability)
 - Analyzed the degradation of AMB AHB on-chip bus due to HCI and NBTI and proposed techniques to maintain the functions of systems when systems degrade
- Research Fellow**, Computer Science and Information Engineering Sep. 1999-June 2001
NTU
- Improved the performance of the cache system of the web proxy server by 5 times by using asynchronous I/O and raw disks
 - Reduced the hardware cost and achieved higher performance in superscalar microprocessor architecture by using hybrid predictor

TEACHING POSITIONS

- Instructor**, Computer Science and Engineering, PSU Aug. 2006-Dec. 2006
- Taught 15-20 students about the principal of digital logic design both in the classroom and laboratory

- Held office hours, answered students' questions, and graded assignments and projects

Teaching Assistant, Computer Science and Engineering Aug. 2003-Dec. 2003

- Held office hours and graded homework and C/C++/Multithread/Script programming assignments for the operating system course

Instructor of Linux training course, Computer Science and Information Engineering, NTU Feb. 2000-June 2001

- Taught students concepts and practices of Linux administrator, web server and ftp server setup and management.

Teacher of Computer Science, National Keelung Senior High School, Keelung, Taiwan Aug. 1998-July 1999

- Taught students concepts and applications of computer technology, including binary number representation, web design, Visual Basic programming language and Microsoft Office
- Administrated the school's web server and mail server

WORK EXPERIENCE

Co-Op, IBM Electronic Design Automation Laboratory, Hudson Valley Research Park, New York May 2004-Nov. 2004

- Proposed a power estimation methodology for SystemC transaction-level models
- Implemented the methodology in IBM SystemC CoreConnect transaction-level models and verified the methodology by comparing transaction-level and gate-level power estimations

System Administrator and Assistant Staff, Department of International Business, NTU Feb. 2002-July 2002

- Designed and maintained the department's web site
- Assisted faculty and students with solving computer problems

PROJECT EXPERIENCE

"Transaction Level Power Modeling Methodology Using PCI- Express Core as the Design Driver," SRC 00541 2004-2005

"High Performance, Distributed and Shared Memory System," National Science Council, Taiwan, NSC 90-2213-E-002-039 2001-2002

"The Study of the Improvement of Superscalar ILP by Branch and Value Prediction," National Science Council, Taiwan, NCS 89-2218-E-131-002 2000-2001

PUBLICATIONS

I.-C. Lin and V. Narayanan, "System Level Power and Reliability Modeling," Ph.D. Forum, Design, Automation and Test in Europe Conference and Exhibition, Apr. 2007 (DATE '07)

N. Dhanwada, R. Bergamaschi², W. Dungan, I. Nair, P. Gramann, W. Dougherty¹ and I.-C. Lin, "Transaction-Level Modeling for Architectural and Power Analysis of PowerPC and CoreConnect based Systems," in Journal of Design Automation for Embedded Systems (JDAES '06)

I.-C. Lin, S. Srinivasan, V. Narayanan, N. Dhanwada, "Transaction Level Error Susceptibility Model for Bus Based SoC Architectures," in Proceeding of International Symposium on Quality Electronic Design, Mar. 2006 (ISQED '06)

I.-C. Lin and V. Narayanan, "Transaction Level Power Modeling for PCI Express," in TECHCON, Oct. 2005 (TECHCON '05)

N. Dhanwada, I.-C. Lin and V. Narayanan, "A Power Estimation Methodology for SystemC Transaction Level Models," in Proceeding of International Conference on Hardware/Software Codesign and System Synthesis, Sep. 2005 (CODES+ISSS '05)

N. Dhanwada, R. Bergamaschi, W. Dungan, I. Nair, W. Dougherty, Y. Shin, S. Bhattacharya, I. Lin, J. Darringer, S. Paliwal¹, "Simultaneous Exploration of Power, Physical Design and Architectural Performance Dimensions of the SoC Design Space using SEAS", in IP Based SoC Design Forum & Exhibition, Dec 2004 (IP/REUSE 04)

S.-L. Huang and I.-C. Lin, "The Study of The Improvement of The Superscalar ILP by Branch and Value Prediction," Technical Report, National Science Council, Taiwan (NSC 89-2218-E-131-002)

CERTIFICATES

Certificate of System-on-Chip Design May 2006
• Issued by the Department of Computer Science and Engineering, PSU
• Skilled in System-on-Chip Design

Certificate of Teacher of Computer Science in Middle and High School Education July 1999
• Issued by Ministries of Education, Taiwan

ACTIVITIES

Delegate in Graduate Student Association Aug. 2006-Present
• Elected by Department of Computer Science and Engineering

IEEE Feb. 2002-Present
• Active student member in the organization for electrical and computer engineers

Table Tennis Club Mar. 2006
• Team Ranked 2 in Pennsylvania Table Tennis Championships
Ranking 6000