

Guangyu Sun

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Planned Graduation Date: May, 2011

Education

2006 - present	Pennsylvania State University PH.D. candidate in Computer Science and Engineering	University Park, PA
2006	Tsinghua University M.S. in Microelectronics	Beijing, P.R.China
2003	Tsinghua University B.S. in Electronic Engineering	Beijing, P.R.China

Research Interests

Computer architecture with an emphasis on memory systems and the three dimension (3D) architectures; Process variations aware designs; 3D VLSI designs; CAD tools programming.

Research Experience

2010-Present	Memory hierarchy exploration for throughput computing We collaborate with Throughput Computing Lab at Intel on the memory hierarchy design for throughput computing systems. A novel model named “Moguls” is developed which explores the design of memory hierarchy to achieve the highest throughput under different constraints ([P1]).	Penn State University
2007-Present	High performance, low power, and high reliable memory systems We collaborate with IBM and Seagate to improve memory systems by leveraging various emerging memory technologies. We evaluate the benefits of the area, power, and performance for MRAM as a cache replacement ([P17]) and propose novel architectures to improve performance and reduce power of MRAM caches in CMPs ([P15]); we propose a hybrid storage using PRAM and NAND flash to improve the performance and lifetime of SSD ([P10]); we investigate the performance/power/temperature/reliability impact of replacing soft error prone SRAM or latches by MRAM in the memory hierarchy ([P4]).	Penn State University
2006-Present	Circuit and architecture level research for 3D technology <ul style="list-style-type: none">• Exploration of 3D cache design for high performance, low power, and efficient thermal control ([P14])([J3]).• Development of CAD tool for through-silicon-via (TSV) placement in 3D IC design ([P12])([P7]).• Development of 3D NUCA cache models (extensions of CACTI and SIMICS ([P15][P14]).	Penn State University
2008-Present	3D chip design and research of design flow <ul style="list-style-type: none">• 3D chip design with 32nm 3D process technology of IMEC.• Exploration and optimization of chip design flow under 32nm 3D process technology.• Chip design of 3D arithmetic units and NOC with 0.15μm 3D technology using NCSU design kit ([P12]).• Exploration of chip design flow with NCSU 3D design kit.	Penn State University
2007	Process Variations Aware Circuit and Architecture Design <ul style="list-style-type: none">• Process variations aware cache evaluation tool (an extension of CACTI).• Operating system level optimizations for process variations.• Process variations aware high-level synthesis ([P19]).	Penn State University

- 2003-2006 **M.S. Thesis: Watermark Techniques in VLSI Designs for IP Protection** Tsinghua University
- Watermark insertion techniques in the physical (layout) level VLSI design ([P21]).
 - Watermark insertion techniques in the synthesis process of VLSI design ([P20]).
 - CAD tool for watermark insertion in physical and RTL level.
- 2003 **B.S. Thesis: High Performance SRAM IP Core Design** Tsinghua University
- Chip design of a high performance SRAM IP core (National 863 Project).
 - CAD tool for SRAM IP core generation.

Awards and Honors

- 2006 College of Engineering fellowship, Penn State UNIV.
- 2005 First prize scholarship for Excellent Graduate Student, Tsinghua University, P.R.China
- 2001 Second prize of Tsinghua Scholarship for Discipline Contest Excellency, P.R.China
- 2000 Second prize in 17th College Physics Contest, P.R.China
- 1998 Second prize in 15th National Olympiad in Physics, P.R. China
- 1998 Second prize(Silver Medal) in 9th National Hope Cup Challenge Contest in Mathematics, P.R.China

Publications

- [P1]. **Guangyu Sun**, Christopher Hughes, Changkyu Kim, Jishen Zhao, Cong Xu, Yuan Xie, Yen-Kuang Chen, “Moguls: a Model to Explore Memory Hierarchy for Throughput Computing”, *to appear at 38th International Symposium on Computer Architecture (ISCA), June 2011.*
- [P2]. Asit K. Mishra, Xiangyu Dong, **Guangyu Sun**, Yuan Xie, N. Vijaykrishnan, Chita R. Das, “Architecting NoCs for Stacked 3D STT-RAM Caches in CMPs”, *to appear at 38th International Symposium on Computer Architecture (ISCA), June 2011.*
- [J3]. **Guangyu Sun** and Yuan Xie, “Performance/Thermal Aware Design of 3D Stacked L2 Caches for CMPs”, *ACM Transactions on Design Automation of Electronic Systems (TODAES, minor revision), 2011.*
- [P4]. **Guangyu Sun**, Dimin Niu, Xiangyu Dong, and Yuan Xie, “A Frequent-Value Based PRAM Memory Architecture”, *16th Asia and South Pacific Design Automation Conference (ASP-DAC), Jan. 2011.*
- [P5]. Y. Chen, H. Li, Z. Sun, X. Wang, W. Zhu, **Guangyu Sun**, and Yuan Xie, “Access Scheme of Multi-Level Cell Spin-Transfer Torque Random Access Memory and Its Optimization”, *53rd IEEE International Midwest Symposium on Circuits and Systems, Aug. 2010.*
- [P6]. **Guangyu Sun**, Xiangyu Dong, Xiaoxia Wu, and Yuan Xie, “3D Architectures of Non-Volatile Memories”, *Workshop on Technology-Architecture Interaction: Emerging Technologies and their Impact on Comp. Architecture, July 2010.*
- [P7]. **Guangyu Sun**, and Yuan Xie, “CMP Architectures with Emerging 3D and Non-Volatile Memory Technologies”, *D43D: Second Design for 3D Silicon Integration Workshop, May 2010.*
- [P8]. Xiaoxia Wu, **Guangyu Sun**, Xiangyu Dong, Reetuparna Das, Jian Li, Chita Das, Yuan Xie, “Cost-driven 3D Integration with Interconnect Layers”, *47th Design Automation Conference (DAC10), July 2010.*
- [P9]. Yongsoo Joo, Dimin Niu, Xiangyu Dong, **Guangyu Sun**, Naehyuck Chang, Yuan Xie, “Energy- and Endurance-Aware Design of Phase Change Memory Cache”, *13th Design, Automation, and Test in Europe (DATE10), Mar. 2010.*
- [P10]. **Guangyu Sun**, Yongsoo Joo, Yibo Chen, Yuan Xie, Yiran Chen, Hai Li, “A Hybrid Solid-State Storage Architecture for the Performance, Energy Consumption, and Lifetime Improvement”, *16th International Symposium on High-Performance Computer Architecture (HPCA10), Jan. 2010.*
- [J11]. Yiran Chen, Hai Li, Cheng-Kok Koh, Kaushik Roy, Jing Li, and **Guangyu Sun**, “Variable-Latency Adder (VL-Adder) Designs for Low Power and NBTI Tolerance”, *IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2009.*
- [P12]. Jin Ouyang, **Guangyu Sun**, Yibo Chen, Lian Duan, Tao Zhang, Yuan Xie, Mary Jane Irwin, “Arithmetic Unit Design Using 180nm TSV-based 3D Stacking”, *IEEE International 3D System Integration Conference (3DSiC), Oct. 2009.*
- [P13]. Ahmed Al Maashri, **Guangyu Sun**, Xiangyu Dong, Vijay Narayanan, and Yuan Xie, “3D GPU Architecture using Cache Stacking: Performance, Cost, Power and Thermal Analysis”, *IEEE International Conference on Computer Design (ICCD), Oct. 2009.*
- [P14]. **Guangyu Sun**, Xiaoxia Wu, and Yuan Xie, “Exploration of 3D Stacked L2 Cache Design for High Performance and Efficient Thermal Control”, *15th International Symposium on Low Power Electronics and Design (ISLPED), Aug. 2009.*

- [P15]. **Guangyu Sun**, Xiangyu Dong, Yuan Xie, Jian Li, and Yiran Chen, “A Novel Architecture of the 3D Stacked MRAM L2 Cache for CMPs”, *15th International Symposium on High-Performance Computer Architecture (HPCA09)*, Feb. 2009.
- [P16]. Srinath Sridharan, Michael DeBole, **Guangyu Sun**, Yuan Xie, and Vijaykrishnan Narayanan, “A Criticality-Driven Microarchitectural Three Dimensional (3D) Floorplanner”, *14th Asia and South Pacific Design Automation Conference (ASP-DAC09)*, Jan. 2009.
- [P17]. Xiangyu Dong, Xiaoxia Wu, **Guangyu Sun**, Helen Li, Yiran Chen, and Yuan Xie, “Circuit and Mircoarchitecture Evaluation of 3D Stacking Magnetic RAM (MRAM) as a Universal Memory Replacement”, *45th Design Automation Conference (DAC08)*, July 2008.
- [P18]. Hai Lin, **Guangyu Sun**, Yunsi Fei, Yie Xie, and Anand Sivasubramaniam, “Thermal-aware design considerations for application-specific instruction set processor”, *IEEE Symposium on Application Specific Processors (SASP08)*, June 2008.
- [P19]. Feng Wang, **Guangyu Sun**, and Yuan Xie, “A Variation Aware High Level Synthesis Framework”, *Design, Automation and Test in Europe (DATE08)*, Mar. 2008.
- [P20]. **Guangyu Sun**, Yi Xu, and Zhiqiang Gao, “A Watermarking System for IP Protection by Buffer Insertion Technique”, *7th International Symposium on Quality Electronic Design (ISQED06)*, Mar. 2006.
- [P21]. **Guangyu Sun**, Zhiqiang Gao, and Min Ni, “A Hierarchy Watermarking Technique for IP Core Protection”, *4th International Conference on ASIC (ASICON05)*, Oct. 2005.

Teaching Experience

- Spring 2009 Teaching assistant **CSE 411 VLSI Digital Circuit Design**
- Fall 2008 Teaching assistant **CSE 431 Introduction to Computer Architecture**
- Fall 2007 Teaching assistant **CSE 331 Computer Organization and Design**
- Fall 2007 Teaching assistant **CSE 331 Computer Organization and Design**

Part-Time Work Experience

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| 2003-2006 | Institute of Microelectronics, Tsinghua UNIV.
System and software administrator of the VLSI circuit design lab. | Beijing, P.R.China |
| Summer 2005 | HT(EDA) Company
Internship programming engineer for an back-end EDA software of VLSI designs. | Beijing, P.R.China |
| Summer 2002 | Bencent Co. Ltd.
Internship engineer for the circuit design and testing. | Shenzhen, P.R.China |

Computer Skills

- Programming C/C++, Verilog/VHDL, Perl/Python, Java, Matlab, MySQL, Assemble Language, etc.
- EDA Tools EDA tools for the whole VLSI design flow from Cadence/Synopsys/Mentor Graphics (such as Virtuoso, Design Compiler, Calibre, etc).
- Arch. Tools SIMICS, GEMS, SimpleScalar, CACTI, Hotspot, etc.

References

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