

# An Accurate and Efficient Model of Electrical Masking Effect for Soft Errors in Combinational Logic

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**Abstract**—Accurate modeling of the electrical masking effect of soft errors for combinational logic circuits represents a significant challenge in soft error rate analysis. Previous proposed models for electrical masking effect can introduce large estimation error. In this work, we use table lookup MOSFET models to accurately capture the nonlinear properties of submicron MOS transistors. Based on these models, we propose transient pulse generation model and propagation model for soft error analysis. From these models, we derive a fast and efficient method to estimate the electrical masking effect for soft error in combinational logic.

## 1. Introduction

Single Event Upset (SEU) is a voltage transient caused by neutron or alpha particles from cosmic ray or package materials [2]. The voltage transients may flip bits in memory cells or latches, causing soft errors. Soft errors in memory can be corrected by ECC(Error Correcting Code) circuitry, and many radiation harden techniques for memory cells or latches have been proposed [2-3]. However, the voltage transient caused by particle strikes can happen on any node in combinational logic. This transient pulse can propagate through logic gates and finally be latched by a sequential element, resulting in a soft error [5]. Cheap solutions to reduce soft errors caused by transients generated in combinational logic are not well understood yet. Fast and accurate analysis of transient pulse propagation in combinational logic is the first step towards the effort of finding efficient solutions.

There are three masking effects that can prevent a transient pulse in combinational logic from propagating and being latched by a memory element: *logical masking*, *electrical masking*, and *latch window masking* [5]. Logical masking happens when one of the other inputs of a gate is in controlling state (e.g., 0 for a NAND gate), so that the transient is blocked. Latch window masking means the arrival transient pulse is outside of the latching window for the sequential elements. These two masking effects have been well studied [3,5,6,10]. Electrical masking happens when the voltage transient resulting from a particle strike is attenuated by subsequent logic gates because of the electrical property of the logic gate [3]. Many models for the electrical masking effect have been proposed [5-9], however, these models introduce large errors for the estimation of transient pulse propagation, resulting in inaccurate soft error analysis for combinational logic.

The difficulty to accurately model transient propagation stems from the nonlinear properties of the MOSFET transistor over any arbitrary operating range. In this paper, we first characterize the nonlinear behavior of the MOS transistor using look up table based model. Then we accurately model two essential steps in the transient pulse simulation: *transient pulse*

*generation* and *transient pulse propagation*. Based on these models, we proposed an accurate and fast SER estimation method for the combinational logic circuits.

The rest of the paper is organized as follows: Section 2 reviews related work; Section 3 presents MOS transistor modeling; Section 4 discusses the model of transient pulse generation, pulse propagation, and overshoot/undershoot and the calculation of critical charge; Section 5 shows experimental results on the test circuits. Finally, the conclusions are provided in Section 6.

## 2. Related Work

Previous work in estimating SER in the combinational logic circuits is based on the time-consuming Monte-Carlo Simulations [11-12]. Recently many attempts have been made to estimate the SER of logic circuits quickly and accurately [5-9]. Fault simulation method [10] or BDD based techniques [6] can be used to estimate the logic masking effect. Latch window masking effect can easily be addressed [5].

However, accurately modeling the electrical masking effect for combinational logic circuits remains a significant challenge. Various techniques have been proposed to capture this effect [5-9]. Delay degradation method first used by Shivakumar [5] can lead to large errors in the estimation of the pulse propagation. As reported by Bellido-Diaz [15], a full swing signal propagating through *three* stages of NAND2 gates can generate 34% error in the pulse width estimation. Simple trapezoid or triangle waveform approximation [5-6] can have as large as 10% of pulse width estimation error even for the transient pulse propagation through a *single* gate. The analytical estimation [9] based on these approximations can lead to even larger error in the transient error analysis.

## 3. Device Modeling

Many analytic transistor models have been proposed to estimate propagation delay of the combinational logic gates [17-19]. These simple MOS models take into account the input waveform, but they fail to conform to the nonlinear properties of the submicron transistor model, which results in a large amount of accumulated error in estimating the transient pulse propagation.

In this section, we present two lookup table based device models: one is the *drain current model*, and the other is the *capacitance model*. These models effectively capture the nonlinear properties of the MOS transistors.

Shima et al. [16] originally proposed the lookup table based drain current model for a *single* transistor in their device simulator. We extend their current model to series connected transistors. We also model the parasitic capacitances using lookup tables. With lookup table based device model, arbitrary precision in modeling the nonlinear devices can be achieved by simply adding more entries to the table. In addition to the nonlinear properties of the MOS transistor, both the stacking

effects of series connected MOS transistors and the input patterns have significant impact on the accuracy of the transient error analysis. Both these two factors have been taken into account in our transistor modeling.

### 3.1 MOS Transistor Drain Current Modeling

The analytic models [17-19] used to estimate the delay of a single CMOS gate approximate the drain current as simple quadratic function or linear function in different regions. They match I-V characteristics of CMOS gates at the high current region very well. But the current at the linear region is typically underestimated in these models and the current at the linear region plays an important role in estimating the waveform of the transient pulse. Further, the current at the region between the linear and saturation region is fairly large and it is very difficult for the analytic model to accurately match the HSPICE model. Thus this inaccuracy can lead to the error that can not be neglected since the large current produces large change in the voltage. All these issues can be mitigated by using the lookup table based drain current model. With a reasonable number of the table entries in the drain current table, the model matches the I-V characteristics of the most advanced bulk CMOS model very well. Since drain current ( $I_{ds}$ ) is the function of the gate source voltage ( $V_{gs}$ ) and the drain source voltage ( $V_{ds}$ ), it can be obtained from the HSPICE simulation by sweeping  $V_{ds}$  and  $V_{gs}$ .

Modeling combinational logic gates as equivalent inverters has been widely used to compute the propagation delay. In recent soft error analysis study [7], the logic gates are collapsed to equivalent inverters to simulate the transient pulse propagation. However, the series connection of the MOS transistors can be replaced by a single transistor only when these transistors operate in the linear region [20]. But this is not always the case, and velocity saturated transistor is not linear.

Another inherent problem of the transistor stacking is that the input transition patterns may have impact on the operation region for each transistor. Modeling the region changes in the stacking transistors complicates the transient pulse simulation.

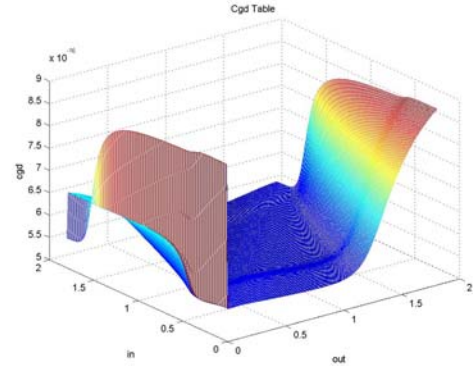
To address these effects, we model the series connected transistor as a single block, and we apply different input transitions to the block and extract the drain current for that block. The drain current ( $I_{ds}$ ) is the function of the number of series connected transistors, the biased voltages, and the input transitions.

### 3.2 Effective Capacitance Modeling

The transient response of a combinational logic gate is sensitive to the effective capacitances of the logic gates. If the effective capacitance is not accurately modeled, the error introduced can be accumulated when the transient pulse propagate through the logic chain. Although the pulse propagation delay of a single gate can be estimated by using a single load capacitance with *constant* value, which is commonly used in the fast delay estimation methods, the analysis of the transient response of the combinational circuits requires a model to characterize the nonlinear property of capacitances.

Figure 1 shows nonlinear properties of the gate to drain capacitance with different input and output voltage applied to an inverter. As shown in Section 4.3, inaccurate modeling of the gate to drain capacitance ( $C_{gd}$ ) can introduce large errors in estimating the output waveform, when we model the overshoot behavior of the gate. The capacitances of the transistors are the function of the gate source voltage ( $V_{gs}$ ), drain source voltage

( $V_{ds}$ ). In this study, similar to the transistor drain current modeling, we construct a lookup table based capacitance model by extracting the capacitance from HSPICE simulation, sweeping the gate source voltage ( $V_{gs}$ ) and drain source voltage ( $V_{ds}$ ).



**Figure 1. Nonlinear properties of gate to drain capacitance ( $C_{gd}$ ) of an inverter.  $C_{gd}$  varies with the change of the input and output voltage applied to the inverter.**

## 4. Soft Error Analysis for Combinational Logic Considering Electrical Masking Effect

The transient pulse generation and pulse propagation are two essential steps for the transient error analysis. In this section, we first present the waveform approximation method for the transient pulse. Based on this approximation method, we present a simple model to estimate the transient pulse generation and attenuation using the table based transistor models presented in Section 3.

### 4.1 Waveform Approximation

In transient analysis, a simple ramp approximation of the waveforms is widely used [5][6][9]. This method is acceptable to estimate the pulse width propagation for a *single* gate. The common form of simple ramp approximation is using trapezoidal or triangular. The slopes of the waveform are approximated by the edges of trapezoidal or triangular. However, this model is too simple to be able to compute the transient response of complex logic gates accurately. The accumulated error introduced by this method make it impossible to accurately estimate the transient pulse width after propagating through several logic gates.

In our research, we use discrete values of the waveform to approximate the transient pulse. We define a time step and at each time step the voltage value is sampled. The time step can be adaptively changed according to the voltage change, which is caused by the current ( $I_{ds}$ ) charge or discharge.

### 4.2 Pulse Generation and Propagation Modeling

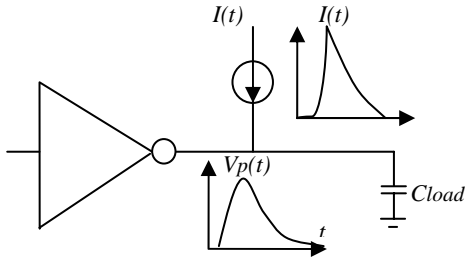
When a high-energy particle strikes a MOSFET device, electron/hole pairs are generated [2][3]. The electrons and holes move towards opposite directions if there is electric field between the source and drain terminals. This movement generates a transient current pulse, which can be modeled as a double exponential pulse [21-22]:

$$I(t) = I_{peak} \times (e^{-t/\tau_a} - e^{-t/\tau_b}) \quad (1)$$

where  $I_{peak} = \frac{Q}{\tau_a - \tau_b}$ , in which  $Q$  is the charge collected as

a result of particle strike,  $\tau_a$  is the collection time-constant,

and  $\tau_b$  is the ion-track establishment time-constant.  $\tau_a$  and  $\tau_b$  are the constants which depend only on process-related factors. The current  $I(t)$  charges/discharges the capacitance at the output node, generating a transient voltage pulse  $V_p(t)$  as shown in Figure 2.



**Figure 2. Transient pulse generation modeling**

Each CMOS logic gate consists of one pull down network and one pull up network. For example, for a NAND gate, the transistors in the pull up network connected in parallel and the transistors in the pull down network connected serially. For the parallel connected transistors, their contributions to drain current can simply add up them together. For the series connected transistor, the drain current is modeled using a lookup table method described in section 3. The total current that can cause output voltage change is equal to summation of the drain currents for these two networks.

As shown in Equation (1), the transient current caused by the particle strike is modeled as a current source  $I(t)$ . Given the input pattern of the logic gates, the transient voltage pulse generated by the particle strike can be modeled as:

$$V_p(0) = f(\text{inputpattern}) \quad (2)$$

$$V_p(T + t_{step}) =$$

$$V_p(T) + \frac{(-I_{ds\_pullup} - I_{ds\_pulldown} + I(T)) * t_{step}}{C_{load} + C_{in} + C_{miller}} \quad (3)$$

where  $I_{ds\_pullup}$  is the total drain to source current of the pull up network,  $I_{ds\_pulldown}$  is the total drain to source current of the pull down network,  $t_{step}$  is the time step for the waveform approximation,  $C_{load}$  is self load capacitance,  $C_{in}$  is the gate capacitance of driver gates, and  $C_{miller}$  is the effective parasitic capacitance between the input and output of the gate [4]. The initial value of the output voltage,  $V_p(0)$ , can be obtained as the function of the input pattern and the type of the logic gates. At time  $T + t_{step}$ , the output voltage  $V_p(T + t_{step})$  can be estimated as  $V_p(T)$  at time  $T$  plus the total charge divided by the load capacitances. The total amount of the charge can be estimated as total current multiplied by the time step  $t_{step}$ . The total current equals to the current pulse generated by particle strike and the drain current.

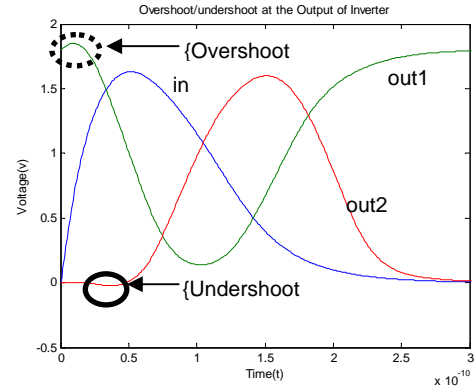
Similar to the pulse generation model, the pulse propagation can be modeled as: given the input and output voltage of a logic gate, at time  $T$ , the output voltage at the time  $(T + t_{step})$  can be approximated as:

$$V_o(T + t_{step}) = V_o(T) + \frac{(-I_{ds\_pullup} - I_{ds\_pulldown}) * t_{step}}{C_{load} + C_{in} + C_{miller}} \quad (4)$$

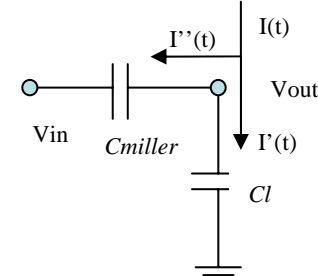
### 4.3 Overshoot/undershoot Modeling

Overshoot (undershoot), as shown in Figure 3, can be defined as the transient value of the voltage that exceeds (is lower than)

the final value [4]. As shown in section 5, overshoot/undershoot has great impact on the accuracy of estimation of the transient pulse propagation. Thus the



**a) overshoot and undershoot**



**b) simple model for the overshoot**

**Figure 3. Overshoot/undershoot in the transient pulse propagation, in is input of the transient pulse, out1 is output of first stage and out2 is the output of 2<sup>nd</sup> stage.**

overshoot and undershoot have to be taken into account in the transient error modeling. Overshoot/undershoot occurs because of the capacitance between the input and output [4]. In this study, we use a simple model to estimate the overshoot/undershoot. As shown in Figure 3, the miller capacitance ( $C_{miller}$ ) is the effective parasitic capacitance between the input and output, and  $C_l$  is the sum of the diffusion capacitances ( $C_{load}$ ) and input capacitances of the load gates ( $C_{in}$ ). The drain current ( $I_{drain}$ ) contributes the change of the voltage across the input and output and the change of the output voltage. Thus, the pulse waveform estimation, which includes the overshoot/undershoot effect, can be performed as:

$$V_o(T + t_{step}) = V_o(T) + \frac{C_{miller} * \delta V_i - I_{drain} * t_{step}}{C_{load} + C_{in} + C_{miller}} \quad (5)$$

where  $\delta V_i = (V_i(T + t_{step}) - V_i(T))$  is the change of the input voltage, and total drain current  $I_{drain} = I_{ds\_pullup} + I_{ds\_pulldown}$ .

## 5. Analysis results

In this section, we present the analysis results and show our model for electrical masking simulation can achieve high accuracy.

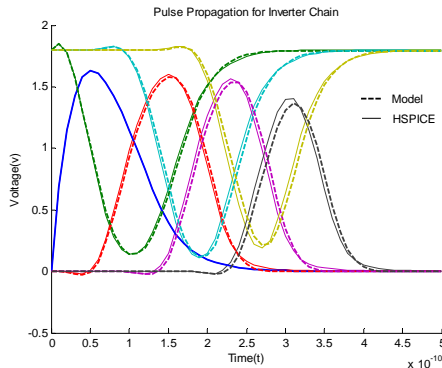
We perform the transient pulse propagation analysis on two simple logic gate networks: an inverter chain and a two-input NAND gate chain for 180nm technology. In Table 1, we show the computation error of the pulse width for transient pulse propagation against the HSPICE simulation. After six stages, the error is less than 3% for the inverter chain. For the NAND2

chain, the error introduced in our analysis is less than 6% after four stages of the propagation.

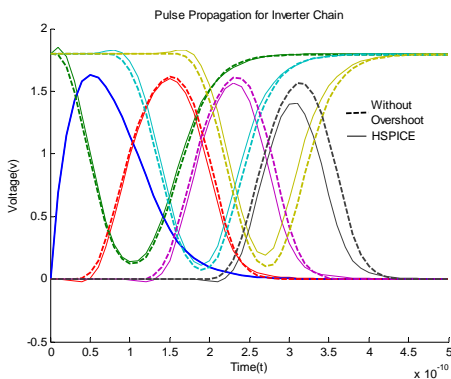
The computed propagation waveforms against HSPICE simulation waveforms are compared in Figure 4. The transient pulse propagation analysis performed with the minimal time step of 1ps and total simulation of 500ps. It can be observed from Figure 4 (a) that the waveform of the 7 stages of inverters generated from our analysis method conform to the HSPICE simulation very well. In Figure 4 (b) the computation error for pulse width can be as large as 30% if we do not include the overshoot model. Figure 5 shows that the propagated transient pulse waveforms, which are generated from our analysis method for 4-stage NAND gate logic chain, conform to the HSPICE simulation very well.

**Table1. Pulse Propagation Computation Errors against HSPICE Simulation**

180nm	# of stages	1	2	3	4	5	6
Inv	Pulse Width Error (%)	1.8	0	0	0	0	2.8
Nand2	Pulse Width Error (%)	2.1	3.2	5.4	-	-	-



**a) Waveform comparison between our transient pulse propagation analysis method with overshoot modeling and the HSPICE simulation.**



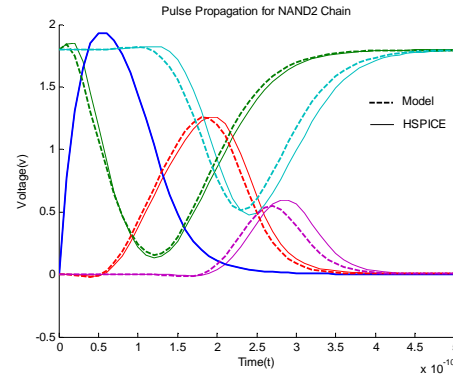
**b) waveform comparison between the transient pulse propagation analysis method without overshoot modeling and the HSPICE simulation.**

**Figure 4. The results of our transient pulse propagation analysis method compared to that of the HSPICE simulation for a 7-stage inverter chain.**

## 6. Conclusion

Accurate modeling of the electrical masking effect in combinational logic circuits is important to perform accurate soft error rate analysis. Previous proposed models for electrical masking effect can introduce large estimation errors. In this work, we have proposed accurate transient pulse generation and

propagation models which can help the electrical masking effect for soft error in combinational logic fast and accurately.



**Figure 5. The results of our transient pulse propagation analysis method compared to that of the HSPICE simulation for a 4 stage nand2 chain.**

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