

SUMMARY OF QUARTERLY TECHNICAL REPORT I

FOR

**Pittsburgh Digital Greenhouse
Electronic Design Technology Development Program**

Project Solicitation 00-2

Project Title: HIGH SPEED CMOS ANALOG-TO-DIGITAL CONVERTER
CIRCUIT FOR RADIO FREQUENCY SIGNAL

Principal Investigator: Kyusun Choi
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Report Period: 12/1/2000 to 4/2/2001

EXECUTIVE SUMMARY

The analog and digital mixed-signal circuit is an essential part of the system-on-a-chip (SOC) products because it bridges a gap between the analog physical world and the digital system on a chip. The thrust of this project is to develop a high speed CMOS analog-to-digital converter (ADC) circuit which will allow on-chip direct digitization of the wideband radio frequency (RF) signal. The prototype chips containing the ADC circuit will be fabricated.

This project features the Threshold Inverter Quantization (TIQ) technique for faster ADC operation using standard CMOS logic circuitry preferred for SOC implementation. The project tasks include:

- (1) Designing a 6 and an 8 bit TIQ based flash ADC circuits and CMOS layouts.
- (2) Fabrication of the first ADC circuit prototype in 0.25 um CMOS technology.
- (3) Testing the first prototype chips and extracting the device parameters.
- (4) Adjusting the design parameters for the second prototype ADC circuit design.
- (5) Fabrication of the second ADC circuit prototype in 0.25 um or 0.18 um CMOS technology.
- (6) Testing and evaluation of the second prototype chips.

As a preliminary result, the initial design of a 6 and an 8 bit ADC has been successfully simulated. Through the fabrication and testing of the prototype chips, we expect to identify the key engineering design challenges and possibly innovate the high speed ADC circuit.

The project duration is one year, from Dec. 1, 2000 to Nov. 30, 2001. The total project cost is \$126,037. We will provide PDG with high speed ADC core design (intellectual property) that is silicon tested, along with semiannual project reports and prototype chips.

PROJECT GOALS FOR THIS QUARTER

- (1) Design a 6 and 8 bit TIQ based flash ADC circuits and CMOS layout
- (2) Design the first prototype chip: 6 and 8 bit flash ADC
- (3) Chip fabrication submission

ACCOMPLISHED PROJECT MILESTONES FOR THIS QUARTER

- (1) Designed a 6, 8, and 9 bit TIQ based flash ADC circuits and CMOS layout in 0.25 um technology
 - Total six ADCs are designed:
 - a 6bit high speed ADC
 - a 6bit low power ADC
 - an 8bit high speed ADC
 - an 8bit low power ADC
 - a 9bit high speed ADC
 - a 9bit low power ADC
 - Circuit design, layout design, simulation, verification, and synthesis
 - TIQ comparator section design and thermometer code-to-binary code encoder design
 - TIQ comparator layout generator program design
 - ADC power optimization

- (2) Designed the first prototype chip: 6, 8, and 9 bit flash ADC.
 - Custom pad-frame design
 - Floor-plan design and place & route 6, 8, and 9 bit ADCs (total six ADCs)
 - Chip design simulation, verification, and synthesis
- (3) Fabrication submission preparation
- (4) Chip fabrication submission
 - Submission date: 4/2/2001
 - Vendor: MOSIS with TSMC 0.25 um foundry
 - Expected prototype chip delivery date: 7/16/2001

FACULTY AND STUDENTS SUPPORTED

- (1) Principal Investigator: Kyusun Choi, Assistant Professor, Department of Computer Science and Engineering
- (2) Graduate Assistant 1: Jincheol Yoo, Ph.D. student, Department of Computer Science and Engineering
- (3) Graduate Assistant 2: Daegyu Lee, MS student, Department of Computer Science and Engineering

PUBLICATION

- Paper Accepted (during this quarter) to Appear:
 - J. Yoo, K. Choi, and A. Tangel, *A 1-GSPS CMOS Flash Analog-to-Digital Converter for System-on-Chip Applications*, the IEEE Computer Society Workshop on VLSI.