Pittsburgh Digital Greenhouse
Electronic Design Technology Development Program

Project Solicitation 00-2

Project Title: HIGH SPEED CMOS ANALOG-TO-DIGITAL CONVERTER CIRCUIT FOR RADIO FREQUENCY SIGNAL

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Program Duration: 1 year: 11/15/2000 - 11/14/2001

EXECUTIVE SUMMARY

The analog and digital mixed-signal circuit is an essential part of the system-on-a-chip (SOC) products because it bridges a gap between the analog physical world and the digital system on a chip. The thrust of this project is to develop a high speed CMOS analog-to-digital converter (ADC) circuit which will allow on-chip direct digitization of the wideband radio frequency (RF) signal. The prototype chips containing the ADC circuit will be fabricated.

This project features the Threshold Inverter Quantization (TIQ) technique for faster ADC operation using standard CMOS logic circuitry preferred for SOC implementation. The project tasks include:

(1) Designing a 6 and an 8 bit TIQ based flash ADC circuits and CMOS layouts.
(2) Fabrication of the first ADC circuit prototype in 0.25 um CMOS technology.
(3) Testing the first prototype chips and extracting the device parameters.
(4) Adjusting the design parameters for the second prototype ADC circuit design.
(5) Fabrication of the second ADC circuit prototype in 0.25 um or 0.18 um CMOS technology.
(6) Testing and evaluation of the second prototype chips.

As a preliminary result, the initial design of a 6 and an 8 bit ADC has been successfully simulated. Through the fabrication and testing of the prototype chips, we expect to identify the key engineering design challenges and possibly innovate the high speed ADC circuit.

The project duration is one year, from Nov. 15, 2000 to Nov. 14, 2001. The total project cost is $126,037. We will provide PDG with high speed ADC core design (intellectual property) that is silicon tested, along with semiannual project reports and prototype chips.

TECHNICAL BACKGROUND

One of the major challenges in developing the complete SOC product for wireless digital network market is the integration of RF analog circuit devices, mostly passive discrete devices. Eventually, we want to replace the passive devices with the active devices. We also want to replace analog designs with full-digital implementations. In view of the technology trend, the speed of active devices will surpass the speed demand of RF signal. Presently 0.18um CMOS technology allows processor speeds in excess of 1 GHz, which is already above 900MHz cellular channel frequency. Ultimately, we want to directly digitize wideband RF signal and use digital signal processing, thus replacing the analog passive discrete devices. To this end, high speed analog to digital converters are absolutely necessary.

This project features the Threshold Inverter Quantization (TIQ) technique for faster ADC operation using standard CMOS logic technology that is compatible with microprocessor fabrication. Figure 1 shows the block diagram of the proposed TIQ based flash ADC. The use of an inverter as a voltage comparator is the reason for the technique's name - Threshold Inverter Quantization. The comparison voltages V_1, V_2, V_3, ... V_n of the inverters are the design parameters fixed by the transistor sizes of each inverter.

In comparison, Figure 2 shows the block diagram of a flash ADC. Here, the differential input voltage comparators are used. A resistor ladder circuit is necessary to provide the n reference voltages. To achieve high speed, such circuits are commonly implemented with bipolar transistor technology which is very costly in comparison, and it is different from the standard CMOS logic technology. For SOC implementation, BiCMOS technology would be necessary to integrate both high speed ADC and processor on one substrate.

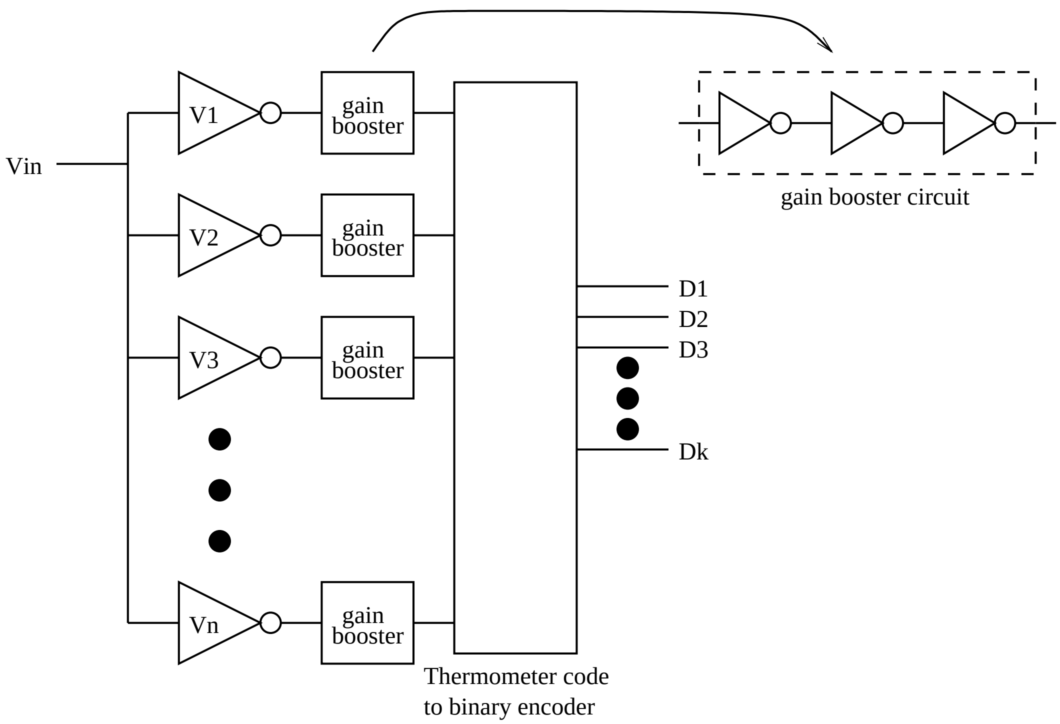
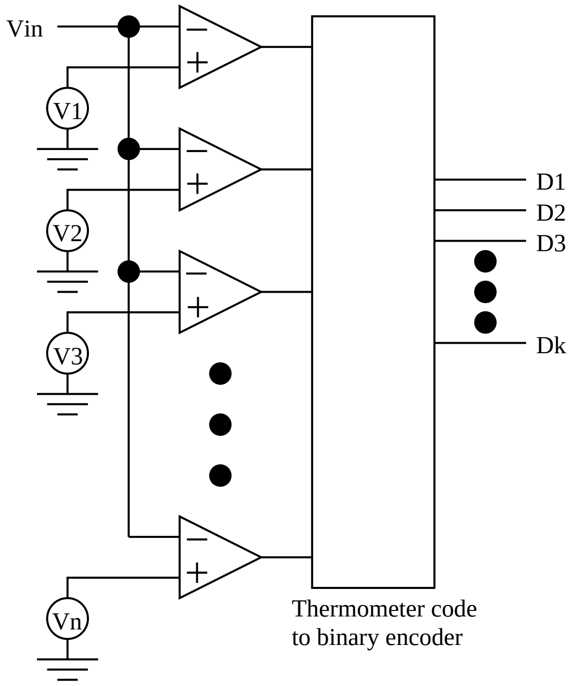
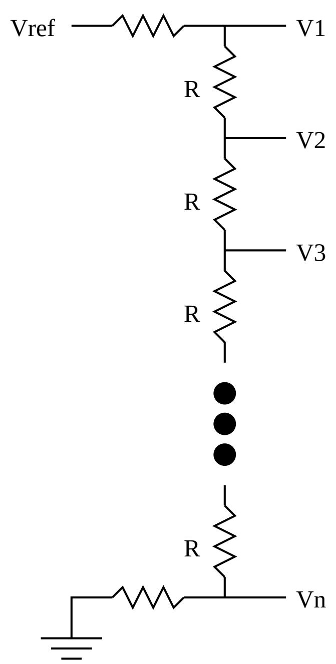


Figure 1 Block diagram of the proposed TIQ based flash ADC.



(a) Block diagram of a flash ADC.



(b) A resistor ladder circuit for the n reference voltages.

Figure 2 Block diagram of a previously known flash ADC and a resistor ladder circuit.

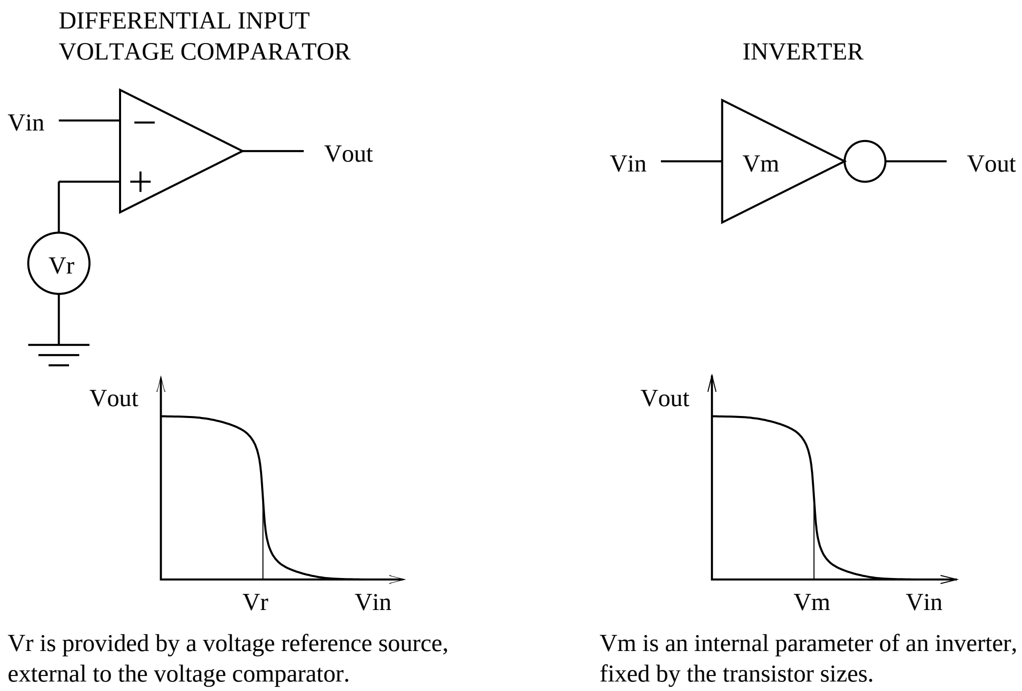


Figure 3 Similarity and difference between a voltage comparator and an inverter. The voltage transfer characteristic curves are similar but the comparison voltages Vr and Vm are fixed differently.

The result is the added processing steps to the standard CMOS technology, and "the process complexity will be a major factor in the cost of the SOC applications" [1]. Faster ADC operation with the TIQ technique using the standard CMOS technology is preferable for SOC implementation.

Figure 3 shows the similarity and difference between a differential input voltage comparator and an inverter. The inverter circuit is inherently simpler and faster than the differential input voltage comparator circuit.

The main advantage of the TIQ based ADC is the high speed using the standard CMOS technology; since, an inverter is a typically fast circuit. The gain booster circuits are minimum size inverters and the thermometer code to binary encoder is a purely digital circuit. Thus, the resulting ADC speed is comparable to the speed of a digital processor. The latest digital processor's speed is in excess of 1 GHz. Existing high speed mixed signal ADC chips commercially fabricated on an advanced BiCMOS process output around 200 MSPS rate [2]. The speed gap of 5X exists. The TIQ based ADC - implemented on the same chip as the processor - may remove the speed gap between the processor and ADC, sustaining the full processor speed by high speed on-chip signal conversion.

The other advantages of the TIQ based ADC are:

* highly adaptable to future CMOS technology development, going to smaller feature size and lower supply voltage,
* no need for a resistor ladder or the reference voltage sources, and
* no need for switches, clock signals, and coupling capacitors.

On the contrary, the following two criteria must be considered carefully to obtain a successful TIQ based ADC implementation:

(1) ADC input range varies due to process parameter changes from one fabrication to another fabrication
(2) An inverter input is single ended, not differential, causing the ADC to become more susceptible to noise.

As a working solution for the criterion (1), one may add a programmable pre-amplifier to the signal input of the TIQ based ADC to adjust signal offset and amplitude. And for the criterion (2), one may implement the inverters in highly isolated substrate from the digital circuits. The combination of the well designed layout strategy, the deep trench isolation, and the separate analog power supply may significantly minimize the effects of noise.

Previous study [3] of the TIQ based ADC reports the following results:

(1) significant speed improvements
(2) extensive simulation results for 6 bit ADC
(3) process variation effects (design corners) on ADC performance
(4) power supply noise tolerance
(5) effects of temperature variation
(6) test results of 4 bit TIQ based ADC chips fabricated with 2.0 um CMOS technology

PROPOSED PROGRAM

In this proposed project, we plan to further investigate the design and implementation of a 6 and an 8 bit TIQ based ADCs. As a preliminary result, a 6 bit TIQ based ADC simulated with 0.25 um CMOS technology resulted in 660 MSPS, shown in Figure 4. Shown in Figure 5, the initial design of an 8 bit ADC with 0.25 um CMOS has been also successfully simulated, resulting in 200 MSPS. Through the fabrication and testing of the prototype chips, we expect to identify the key engineering design challenges and possibly innovate the high speed ADC circuit.

We have three main goals for this research project. First, we want to increase the speed of a flash ADC using the TIQ technique. A 6 and an 8 bit TIQ based ADC chip will be fully custom designed. We will optimize it for speed, and minimize power and size as secondary.

Second, we will provide PDG with high speed ADC core design (intellectual property) that is silicon tested. We will fabricate the ADC chips in two different times, the first one being the pilot test fabrication for the second fabrication. The high speed ADC core has the following applications for the PDG members:

* wideband RF, baseband RF, & IF signal digitization
* wireless local loop
* local multi-point distribution service
* wireless point to point systems
* radar/communications
* universal computer network adaptor

Third, we will explore the design limits of TIQ based ADC. We will explore:

* new inverter circuits for voltage comparison
* new circuits for thermometer code to binary encoder
* faster circuits

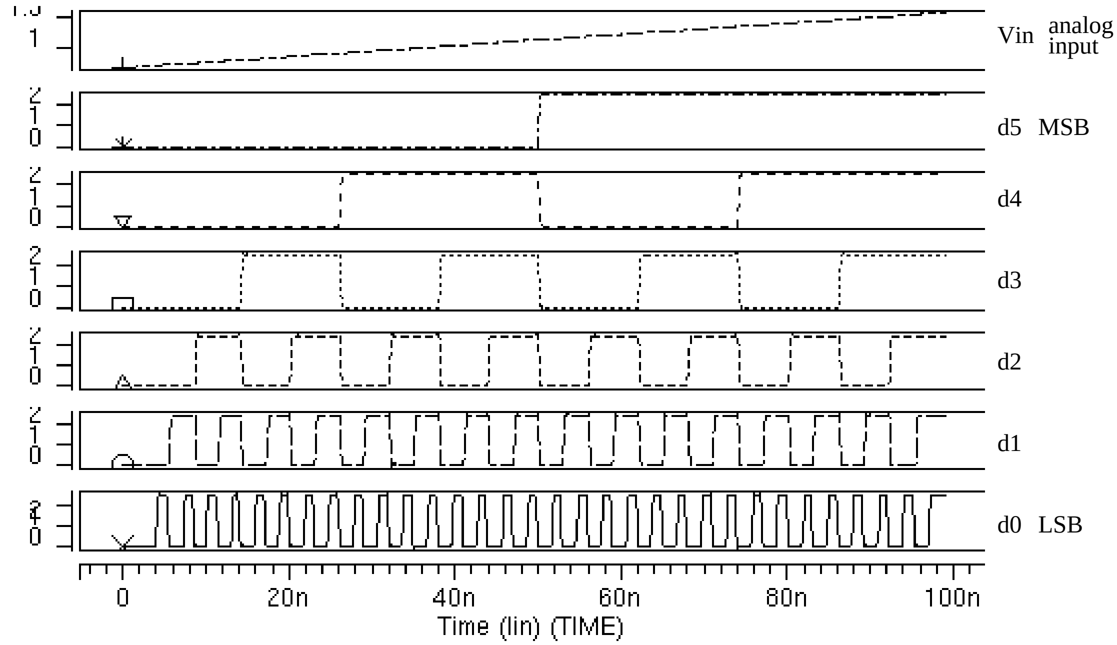


Figure 4 An Hspice simulation output of a 6 bit TIQ based ADC designed with 0.25um CMOS technology. Analog input varies from 0.68V to 1.55V, in 64 steps, 1.5nsec. sample and hold time, showing over 660 Million Samples Per Second operation speed.

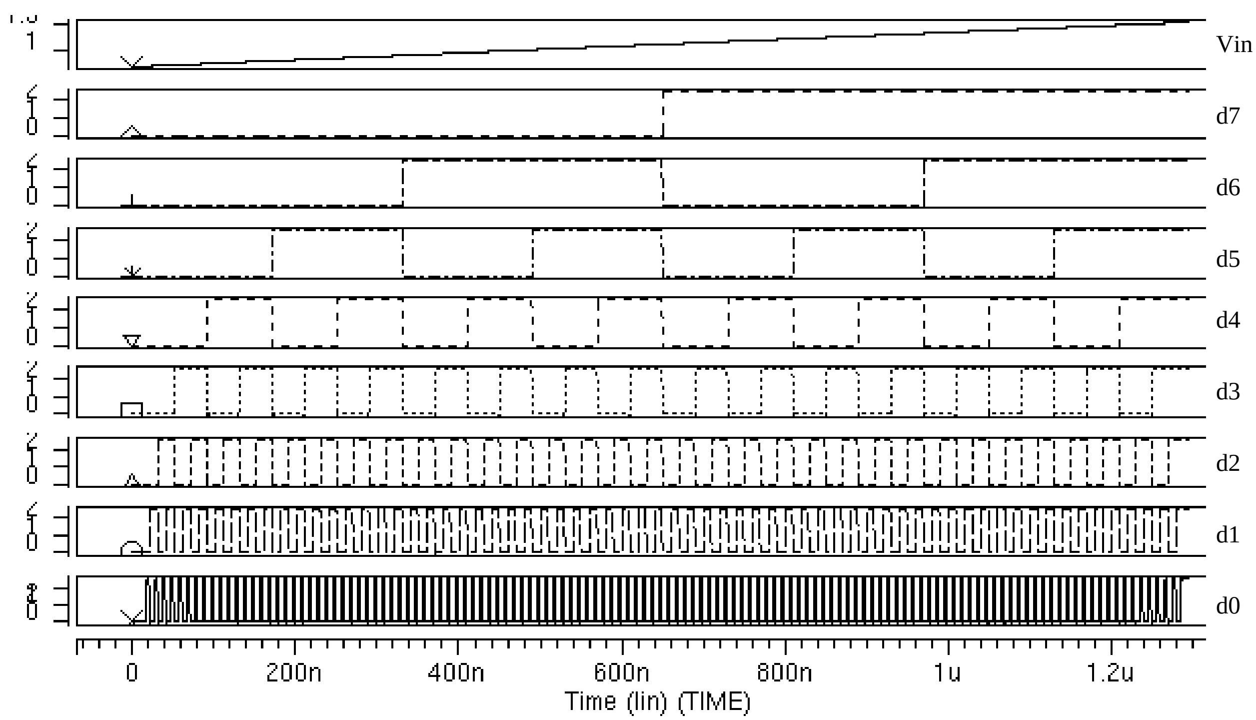


Figure 5 An Hspice simulation output of an 8 bit TIQ based ADC designed with 0.25um CMOS technology. Analog input varies from 0.67V to 1.53V, in 256 steps, 5.0 nsec. sample and hold time, showing over 200 Million Samples Per Second operation speed.

* lower energy circuits
* more stable circuits
* more noise tolerant circuits
* more ways to innovate ADC

The project duration is one year, from Nov. 15, 2000 to Nov. 14, 2001. The project tasks include:

(1) Designing a 6 and an 8 bit TIQ based flash ADC circuits and CMOS layouts.
(2) Fabrication of the first ADC circuit prototype in 0.25 um CMOS technology (MOSIS service).
(3) Testing the first prototype chips and extracting the device parameters.
(4) Adjusting the design parameters for the second prototype ADC circuit design.
(5) Fabrication of the second ADC circuit prototype in 0.25 um or 0.18 um CMOS technology.
(6) Testing and evaluation of the second prototype chips.

REFERENCES

[1] *International Technology Roadmap for Semiconductors: System-on-a-Chip*, 1999 Edition, Pg. 26.

[2] *AD9054A Data Sheet*, Analog Devices Inc., Norwood, MA, posted at: www.analog.com.

[3] Tangel, A. (1999) *VLSI implementation of the threshold inverter quantization (TIQ) technique for CMOS flash A/D converter applications*, Ph.D. Thesis, The Pennsylvania State University.

PROJECT PLAN, SOW, MILESTONES, AND DELIVERABLES

Detail project plan and deliverable schedule is shown in Table 1. The list of work component is shown in Table 2. The project deliverables are:

* one mid-project progress report
* final project report
* first prototype chip design (circuits and layouts)
* sample chips for the first prototype
* second prototype chip design (circuits and layouts)
* sample chips for the second prototype
* project presentations

Available resources are:

* facilities and laboratory space,
* workstations and CAD tools,
* equipments and supplies.

Needed resources are personnel and budget. The project will employ following three staff for the duration of 1 year:

* Principal Investigator - Overseeing project development and operation, establish and maintaining links with PDG, and responsible for graduate assistant hiring and work assignment.
* Graduate Assistant 1 (50%) - Responsible for the assigned work from Table 2.
* Graduate Assistant 2 (50%) - Responsible for the assigned work from Table 2.

Table 1. Detail project plan and deliverable schedule

Date	Project Milestones	Project Deliverable
11/15/2000	1st chip design, synthesis, verification, & fab submition	
12/5/2000	9 weeks	
12/26/2000	↓	
1/17/2001	1st chip fabrication	
2/7/2001	9 weeks	
2/28/2001	↓	
3/19/2001	1st chip testing and parameter extraction	
4/9/2001	9 weeks	
4/30/2001	↓	Mid-project report & 1st chip samples
5/20/2001	2nd chip design, synthesis, verification, & fab submition	
6/13/2001	9 weeks	
7/3/2001	↓	
7/24/2001	2nd chip fabrication	
8/15/2001	9 weeks	
9/5/2001	↓	
9/26/2001	2nd chip testing and parameter extraction	
10/17/2001	7 weeks	Final project report & 2nd chip samples
11/7/2001 11/14/2001	↓	Project presentation

Table 2. List of the work component

Chip design
1st prototype chip — 6 bit ADC; 2nd prototype chip — 8 bit ADC
Comparator section (TIQ): Circuit design, Layout design, Simulation, Verification, Synthesis
Thermometer to binary encoder: Circuit design, Layout design, Simulation, Verification, Synthesis
Floorplan, place, route, and padframe: Simulation, Verification, Synthesis
Fab submision preparation
Fab submision
Chip testing: Test design, Test setup and program, Measuring and data collection, Test data analysis, Evaluation, Parameter extraction
Report writting
Project presentation and demonstration

INVESTIGATOR BIOGRAPHICAL INFORMATION

Kyusun Choi (www.cse.psu.edu/~kyusun) is an Assistant Professor in the Department of Computer Science and Engineering at The Pennsylvania State University, where he taught for 7 years and received a best teacher award from the department. He received his B.S. from Lehigh University, M.S. and Ph.D. from The Pennsylvania State University. His current research and teaching interests include mixed-signal VLSI circuit design, RF ASICs, and DSP architecture for RF signal. He is the inventor of the three PSU invention disclosures: No. 98-1967, a parallel ADC circuit different from the TIQ based ADC, US patent pending; No. 99-2135, a fast DAC circuit, US patent pending; No. 2000-2336, an area efficient ADC circuit different from the TIQ based ADC.
