

Balaji Vaidyanathan

Principal Engineer

Technology Reliability Physics Dept., R&D
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EDUCATION

PhD in Computer Science and Engineering 2010
Pennsylvania State University CGPA: 3.78/4.00
B.E in Computer Science and Engineering 2003
University of Madras, India First Class with distinction

WORK EXPERIENCE

Principal Engineer, Technology Reliability Physics Dept., R&D, TSMC, Taiwan 2009-Present
Mentor: A. S. Oates
Research Engineer, Technology Reliability Physics Dept., R&D, TSMC, Taiwan 2007-2009
Mentor: A. S. Oates
- *Logic, Analog/RF, SRAM, eDRAM reliability modeling and analysis considering*
- *NBTI, PBTI, HCI, and Soft-Errors*
Summer Intern, Technology Reliability Physics Dept., R&D, TSMC, Taiwan Summer 2007
Advisors: J. -C. Lin , A. S. Oates
- *Soft Error Rate (SER) Modeling and Analysis for SRAM and eDRAM*
Research Assistant, Department of CSE Spring 2007
Research Assistant, Department of CSE Fall 2006
Advisors: Y. Xie, N. Vijaykrishnan, M. J. Irwin
- *Analysis of Aging in AMBA bus architecture due to NBTI and HCI*
Research Assistant, Department of CSE Summer 2006
Advisors: Y. Xie, N. Vijaykrishnan, M. J. Irwin
- *NBTI-aware CAD flow design*
Teaching Assistant, Department of CSE Spring 2006
- *Computer Design and Organization (CSE 331)*
Research Assistant, Department of CSE Fall'04-Fall'05
Advisors: Y. Xie, N. Vijaykrishnan, M. J. Irwin
- *Leakage optimized decap placement for power grid* Fall 2005
- *Soft Error analysis of asynchronous circuits* Summer 2005
- *Crosstalk aware bus power optimization in Codecompressed H/W* Spring 2005
- *3D Stacked implementation of Arithmetic units* Fall 2004

SKILL SET

Languages : C, C++, SQL, ForTran, COBOL, PASCAL, Visual Basic, Perl
Simulation Tools : Synopsis Design Compiler, PrimeTime Analyzer, Tsuprem, & Medici, Cadence Silicon
: Ensemble & SoC Encounter, VERILOG, VHDL, SiS, HSPICE, SimpleScalar, MatLab
Hardware Tools : eTest and Bench Measurement

RESEARCH INTEREST

Statistical System-on-Chip reliability modeling

PUBLICATIONS

- **B. Vaidyanathan, S. Bai, A. S. Oates,** "The Relationship Between Transistor-Based and Circuit-Based Reliability Assessment for Digital Circuits", *IEEE Intl. Reliability Physics Symposium (IRPS) 2011.*

- **B. Vaidyanathan, Y. Xie**, "Aging and Process Variation Aware Reliability Analysis and Optimization for Nanoscale System-On-Chip Design", *ACM/IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2010 (Best Student Forum Poster Award)*
- **B. Vaidyanathan, A. S. Oates, Y. Xie**, "Intrinsic NBTI-Variability Aware Statistical Pipeline Performance Assessment and Tuning", *IEEE/ACM Intl. Conference on Computer Aided Design (ICCAD) 2009*
- **B. Vaidyanathan, Y. Wang, Y. Xie**, "Cost-Aware Lifetime Yield Analysis of Heterogeneous 3D On-Chip Cache", *IEEE Intl. Workshop On Memory Technology, Design, and Testing (MTDT) 2009*.
- **Y. -P. Fang, B. Vaidyanathan, A. S. Oates**, "Soft Error Rate Cross-Technology Prediction on Embedded DRAM", *IEEE Intl. Reliability Physics Symposium (IRPS) 2009*.
- **B. Vaidyanathan, A. S. Oates, Y. Xie, Y. Wang**, "NBTI-Aware Statistical Circuit Delay Assessment", *IEEE Intl. Symposium on Quality Electronic Design (ISQED) 2009*.
- **B. Vaidyanathan, W. -L. Hung, F. Wang, Y. Xie, V. Narayanan, M. J. Irwin**, "Architecting Microprocessor Components in 3D Design Space", *Intl. Conference on VLSI Design (VLSID) 2007*.
- **B. Vaidyanathan, Y. Xie, V. Narayanan, R. Luo**, "Leakage Optimized DECAP Design for FPGAs", *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) 2006*.
- **B. Vaidyanathan, Y. Xie**, "Crosstalk-Aware Energy Efficient Encoding for Instruction Bus through Code Compression", *IEEE System-On-Chip Conference (SOCC) 2006*.
- **B. Vaidyanathan, Y. Xie, V. Narayanan, H. Zheng**, "Soft Error Analysis and Optimizations of C-elements in Asynchronous Circuits", *The Second Workshop on System Effects of Logic Soft Errors (SELSE), 2006*.

RESEARCH THESIS

Doctoral Dissertation: "Reliability Analysis and Optimization for Nano-scale System-on-Chip Design"

Undergraduate Thesis: "Multi GHz Deep Sub Micron Test issues and towards their Solution" (**State-Level Best Undergraduate Thesis Award**). Accessible from Naren Group at <http://www.warftindia.org/>)

COURSES TAKEN

VLSI Digital Circuits (CSE 477)	Network on Chip Architecture (CSE 598B)
Fault Tolerant Systems (CSE 536)	VLSI CAD Tools (CSE 578)
Topics in Computer Architecture (CSE 539)	Computer Networks (CSE 514)
Nano Architecture (CSE 598B)	Multi Processor Architecture (CSE 532)
Digital Design Using Field Programmable Devices (CSE 478)	Algorithm Design and Analysis (CSE 565)
Computer Arithmetic/Advanced VLSI System Design (CSE 575/577)	Computer & Network Security (CSE 497C)

PROFESSIONAL ACTIVITIES

Program Committee Member : Circuit Reliability section of *IEEE IRPS 2011*

External Reviewer : *IEEE Tran. on VLSI (TVLSI)*, *IEEE Tran. on Elec. Devices (TED)*,
 : *ACM Tran. on Design Automation of Elec. Systems (TODAES)*, *IRPS*,
 : *DAC, ICCAD, ICCD, ISCA*

PERSONAL DETAILS

Nationality : Indian
 Current Visa Type : B1/B2, Multiple Entry, Expires Jul 2019
 Website : www.cse.psu.edu/~bvaidyan

REFERENCES

Available upon request.