

Balaji Vaidyanathan

Engineer

Technology Reliability Physics Dept., R&D
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EDUCATION

PhD in Computer Science and Engineering	Current
Pennsylvania State University	CGPA: 3.78/4.00
B.E in Computer Science and Engineering	2003
University of Madras, India	Aggregate: 77.4%

WORK EXPERIENCE

Engineer, Technology Reliability Physics Dept., R&D, TSMC, Taiwan	Current
Advisor: A. S. Oates	
- <i>Modeling and analysis of NBTI induced aging in Logic and SRAM</i>	
Summer Intern, Technology Reliability Physics Dept., R&D, TSMC, Taiwan	Summer 2007
Advisors: J. -C. Lin , A. S. Oates	
- <i>Soft Error Rate (SER) Modeling and Analysis in SRAM and E-DRAM</i>	
Research Assistant, Department of CSE	Fall 2007
Research Assistant, Department of CSE	Fall 2006
Advisors: Y. Xie, N. Vijaykrishnan, M. J. Irwin	
- <i>Analysis of Aging in AMBA bus architecture due to NBTI and HCE</i>	
Research Assistant, Department of CSE	Summer 2006
Advisors: Y. Xie, N. Vijaykrishnan, M. J. Irwin	
- <i>NBTI-aware CAD flow design</i>	
Teaching Assistant, Department of CSE	Spring 2006
- <i>Computer Design and Organization (CSE 331)</i>	
Research Assistant, Department of CSE	Fall'04-Fall'05
Advisors: Y. Xie, N. Vijaykrishnan, M. J. Irwin	
- <i>Leakage optimized decap placement for power grid</i>	Fall 2005
- <i>Soft Error analysis of asynchronous circuits</i>	Summer 2005
- <i>Crosstalk aware bus power optimization in Codecompressed H/W</i>	Spring 2005
- <i>3D Stacked implementation of Arithmetic units</i>	Fall 2004

COMPUTING SKILLS

Operating Systems : Linux, Solaris, Macintosh, Windows
Languages : C, C++, Matlab, MySQL, ForTran, COBOL, PASCAL, Visual Basic, Perl
Simulation Tools : Synopsis Design Compiler, PrimeTime Analyzer, Tsuprem, & Medici, Cadence Silicon Ensemble & SoC Encounter, VERILOG, VHDL, SiS, Hspice, Magic, SimpleScalar

RESEARCH INTEREST

Low power, Reliable design, and 3D IC architectures.

PUBLICATIONS

Conference

- **B. Vaidyanathan, A. S. Oates, Y. Xie,** "Intrinsic NBTI-Variability Aware Statistical Pipeline Performance Assessment and Tuning", *IEEE/ACM Intl. Conference on Computer Aided Design (ICCAD) 2009.*

- **B. Vaidyanathan**, Y. Wang, Y. Xie, "Cost-Aware Lifetime Yield Analysis of Heterogeneous 3D On-Chip Cache", *IEEE Intl. Workshop On Memory Technology, Design, and Testing (MTDT) 2009*.
- Y. -P. Fang, **B. Vaidyanathan**, A. S. Oates, "Soft Error Rate Cross-Technology Prediction on Embedded DRAM", *IEEE Intl. Reliability Physics Symposium (IRPS) 2009*.
- **B. Vaidyanathan**, A. S. Oates, Y. Xie, Y. Wang, "NBTI-Aware Statistical Circuit Delay Assessment", *IEEE Intl. Symposium on Quality Electronic Design (ISQED) 2009*.
- **B. Vaidyanathan**, W. -L. Hung, F. Wang, Y. Xie, V. Narayanan, M. J. Irwin, "Architecting Microprocessor Components in 3D Design Space", *Intl. Conference on VLSI Design (VLSID) 2007*.
- **B. Vaidyanathan**, Y. Xie, V. Narayanan, R. Luo, "Leakage Optimized DECAP Design for FPGAs", *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) 2006*.
- **B. Vaidyanathan**, Y. Xie, "Crosstalk-Aware Energy Efficient Encoding for Instruction Bus through Code Compression", *IEEE SOCC 2006*.
- **B. Vaidyanathan**, Y. Xie, V. Narayanan, H. Zheng, "Soft Error Analysis and Optimizations of C-elements in Asynchronous Circuits", *The Second Workshop on System Effects of Logic Soft Errors (SELSE), 2006*.
- N. Venkateswaran, **B. Vaidyanathan**, V. Mahalingam, T. L. Rajaprabhu, "BSM Fault Coverage Analysis in EDAC encoded FSM", *IEEE 12th North Atlantic Test Workshop (NATW) 2003*.
- N. Venkateswaran, **B. Vaidyanathan**, V. Mahalingam, T. L. Rajaprabhu, "An Encoding Scheme for Instruction, Data and Address in a Multi-GHz Processor for Concurrent Cross-talk Fault Detection", *IEEE 12th North Atlantic Test Workshop (NATW) 2003*.
- N. Venkateswaran, **B. Vaidyanathan**, V. Mahalingam, T. L. Rajaprabhu, "Super Scalar Architecture for billion device Combinational and Sequential Circuit Test Design", *IEEE 39th Autotestcon 2003*.
- N. Venkateswaran, **B. Vaidyanathan**, V. Mahalingam, T. L. Rajaprabhu, "Analysis of Bit Transition Count For EDAC Encoded FSM", *IEEE 9th International On-Line Testing Symposium (IOLTS) 2003*.
- N. Venkateswaran, **B. Vaidyanathan**, V. Mahalingam, T. L. Rajaprabhu, "Cross-Talk Fault Tolerant Processor Architecture - A Power Aware Design", *IEEE 2nd International Workshop on Electronic Design Test and Applications (DELTA) 2004*.

RESEARCH THESIS

I have co-authored an under graduate thesis titled "*Multi GHz Deep Sub Micron Test issues and towards their Solution*". (Available at Naren Group at <http://www.warftindia.org/>)

COURSES TAKEN

VLSI Digital Circuits (CSE 477)	Network on Chip Architecture (CSE 598B)
Fault Tolerant Systems (CSE 536)	VLSI CAD Tools (CSE 578)
Topics in Computer Architecture (CSE 539)	Computer Networks (CSE 514)
Nano Architecture (CSE 598B)	Multi Processor Architecture (CSE 532)
Digital Design Using Field Programmable Devices (CSE 478)	Algorithm Design and Analysis (CSE 565)
Computer Arithmetic/Advanced VLSI System Design (CSE 575/577)	Computer & Network Security (CSE 497C)

PERSONAL DETAILS

Nationality : Indian
 Current Visa Type : B1/B2, Multiple Entry, Expires Jul 2019
 Website : www.cse.psu.edu/~bvaidyan

REFERENCES

Available upon request.