

Temperature and Voltage Scaling Effects on Electrical Masking

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Abstract— Radiation induced soft errors in combinational logic is expected to become as important as directly induced errors on memory elements. Recent works have looked at modeling and estimating soft errors in logic circuits. Increased power consumption with very dense circuits has led to large number of hot spots in present day ICs. Voltage scaling is one of the popular techniques used for power reduction in circuits. This work presents the results from a study of effects of both increased temperature and voltage scaling on electrical masking effect in logic circuits.

Index Terms— Soft error, Thermal effects, voltage scaling.

I. INTRODUCTION

CONTINUOUS scaling of CMOS technology has resulted in very dense circuits. Consequently, power and temperature/thermal issues are playing an important role in design considerations in nanometer technologies. Voltage scaling is one of the important techniques that have been frequently used for active power reduction. Both temperature increase and voltage scaling affect the transistor delay, which will in turn affect the Soft Error Rates (SER) in logic circuits. SER in logic circuits depend on three masking effects: logical masking, electrical masking and latch window masking. Of these, electrical masking (which is a function of the gate and interconnect-delays) and latch window masking (which is a function of flip-flop set-up and hold times) vary with both temperature and voltage scaling. This study focuses on the combined effect of increased temperature and voltage scaling on the electrical masking effect.

Heat generation in chips has increased rapidly with recent scaling trends and increased transistor density. This has led to non-uniform substrate temperature profile, affecting both interconnect and transistor delays. In the case of interconnects, the rise in temperature increases the resistivity of metals thus resulting in increased delays. In devices, temperature affects both the mobility and the threshold voltage. Thus the overall delay of a logic chain changes and affects the electrical masking capability of the logic chain. The change in transistor delays also affects flip-flop characteristics like the set-up and hold times. This in turn results in a change in latch window masking capability of logic circuits. Thus, it is important to

analyze these effects in detail and so far no work has contributed to such an analysis.

Voltage scaling is one of the most popular techniques used in modern microprocessors for power reduction. The increased delay because of voltage scaling in turn will affect both the pulse mitigation property (electrical masking) of logic chains and the flip-flop set-up and hold times, thus affecting the latch window masking. Thus it will be interesting to analyze the result of both temperature and voltage variation on the two masking effects.

In this work we first look at the effect of temperature and voltage on transistor delays by analyzing the voltage transfer characteristics of an inverter in Section 2. Section 2 also presents the results of device analysis on current generation. After the initial analysis, the experimental set-up is presented in Section 3. Finally, results of SER variation with temperature and voltage scaling in three different circuits are compared in Section 4.

II. THEORY AND INITIAL ANALYSIS

The electrical masking effect is a strong function of the cell delays. The cell delay determines the amount of pulse mitigation across the cell and hence the electrical masking effect. Here, we present the theory and an initial analysis on the effects of temperature and voltage variation on the delay.

The charge collection and current generation in the devices are responsible for the current spike and hence the glitches in circuits. The amount of charge collection and the current generation will also vary with temperature. We study these effects using device simulators and have presented the analysis in this section.

A. Temperature and voltage effects on logic cell delay

Rise in substrate temperature reduces the mobility of MOSFETs because of increased scattering at higher temperature [3]. The threshold voltage also decreases with increase in temperature because of the change in fermi potential (ϕ_f) [4]. But it has been found that the effect on threshold voltage is much lesser than that of on the mobility [3]. Thus, the overall effect of temperature on the delay of circuits is to increase the delay. The delay of interconnects also increases with temperature due to reduced mobility in the metals.

Now, we study the voltage transfer characteristics (VTC) of a single inverter stage. The inverter was laid out in 1V, 70nm technology and extracted using BSIM3 [5] models for transistors. The HSPICE simulation results are shown in

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Figure 1. The VTC was measured at 25°C (room temperature), 40°C, 70°C and 100°C. Thus clearly from Figure 1, the overall gain (slope) of the inverter reduces which is due to the decrease in the delay. The effect of reduced threshold voltage at higher voltages can also be noticed in Figure 1 as the dotted and dashed lines (corresponding to higher temperatures) move away from supply and ground at an earlier voltage. Here the effect of temperature on both the device and interconnects in an inverter, although the effect on interconnect delays will be more pronounced at the system level. Similar results were also observed at lower voltages of 0.8V and 0.6V (not shown here).

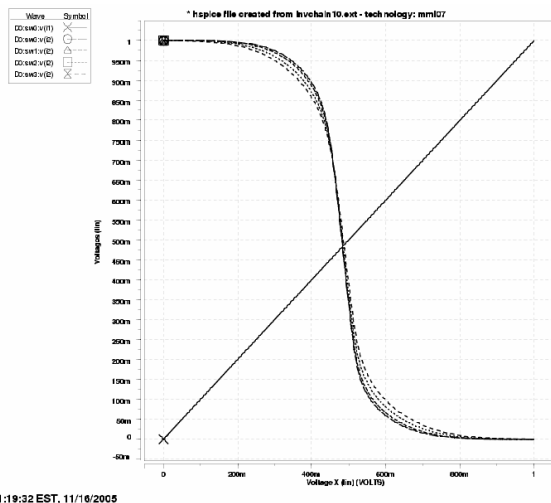


Figure 1. VTC for an inverter

B. Device Simulation

We performed experiments at the device level to observe the temperature and voltage effects on the generation and collection of charges in a single device. To examine these effects on the transient current pulse, we used the Synopsys TCAD Davinci device simulator. Davinci uses physical model and equation interface (PMEI) to perform simulations that incorporate user-defined physical models and equations. The inputs to the 3D device simulator are the device structure, device parameters, device level equations and the charge generation rate.

The device simulator was setup to include the physical models that combine the drift-diffusion laws and classical physical models. These models include carrier-carrier scattering mobility model (CCSMOB), to account for the large carrier concentrations present in the charge column. It also includes the effects of doping and temperature in mobility. Field - dependent mobility model (FLDMOB), to account for reverse biased junction and high electric fields in the depletion region is also modeled. Shockley-Read-Hall and Auger recombination (SRH) are also modeled to account for recombination of the carriers. Band-gap-narrowing (BGN) model is used to model the pn junction as a bipolar device. The device is also attached to a lumped resistance and capacitance models to ensure realistic conditions.

The electron-hole pairs are introduced in the simulation as a charge column [1]. The charge column is assumed to have a Gaussian profile and is generated over a period of about 6

picoseconds using a Gaussian waveform. The structure was set up to solve time-dependent solution. The output from the 3D simulation is used to generate the transient current pulses at various temperatures. The current is integrated over time to calculate the charge collected by the hit. We attribute the cause of the drift current to the drift processes: funneling and alpha-particle source-drain penetration effect (ALPEN) [2].

We used a 130 nm PMOS and NMOS transistor as a test design to the device simulator. The details of the process parameters of the transistors are given in Table 1. The device structure was simulated to operate at various temperatures between 273 K (0 °C) and 375 K (102 °C) and the corresponding current transients were observed. Figure 2 shows the drift current due to the collected charges for the first 100 picoseconds for an NMOS. Based on the current profile, it is observed that at lower temperatures, the contribution of the drift current to the collected charge is higher than that at higher temperatures. However the change in the current peak is very minimal as seen in Figure 2. The difference in the current is of the order of few microamperes. We attribute this decrease to the increase in resistance in the substrate and S/D of the transistor due to the increase in the lattice temperature of the device.

Similar experiments were conducted to study the variation of generated current with voltage scaling. Figure 3 presents the results for these experiments. Clearly, as the voltage decreases, the peak value of the generated current decreases as seen. The width of the current pulses remains the same with little variation as seen.

TABLE 1
Process Parameters

Parameters	NMOS	PMOS
Epitaxial layer doping/ cm^3	$3e^{+15}$	$3e^{+17}$
Substrate doping/ cm^3	$5e^{+17}$	$3e^{+19}$
Channel junction depth/ μm	0.05	0.05
Channel peak S/D Doping/ cm^3	$2e^{+20}$	$2e^{+20}$
Power supply voltage/ V	1	1

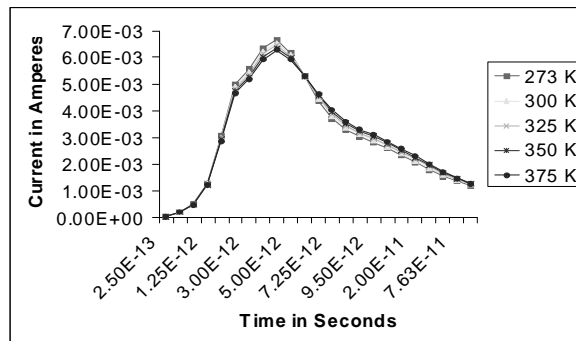


Figure 2 NMOS Current transient pulse due to the collected charge when operated under different temperatures

III. EXPERIMENTAL SET-UP

Here, we describe the various experimental analyses done on the effects of temperature and voltage scaling on the various factors that affect SER. To study these effects, layouts of an inverter chain, a logic chain, and c17 (an ISCAS

benchmark, See Figure 4) were built using Micro-magic, a layout tool in 1V, 70nm technology. SPICE Net-lists were then extracted for these designs and simulations were run using HSPICE with BSIM3 models [5] for modeling the transistors.

In each of the circuits, exponential current pulses (as in Figure 2) of same magnitude were injected at different nodes. The resulting voltage pulses at different nodes in the path were studied at different temperature and voltages to analyze the electrical masking effects. Results for various experiments are described in the next section.

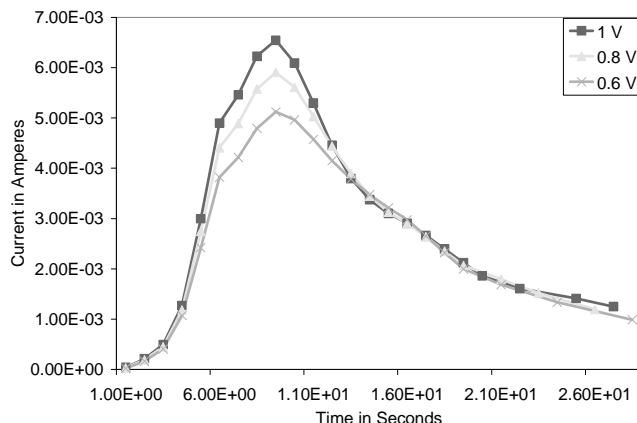


Figure 3 NMOS Current transient pulse due to the collected charge when operated under different voltages

IV. RESULT SUMMARY

Now, we present the results of temperature on the electrical masking effects for different circuits simulated with HSPICE. We also present the results of temperature effects at different supply voltages. Simulations were performed by injecting current pulses resembling the ones in Figure 2 at different nodes in three different circuits.

A. Temperature effects

To study the effect of electrical masking, the variation of pulse characteristics (amplitude and width) at different nodes at which the current is injected (IP), at the output of the gate to which the node IP is the input (OP), and at the output of the path (Path_OP) were analyzed.

At the injected node IP, when the same current pulse was injected at all temperatures, there was a very slight increase in pulse width with temperature. The variation occurs due to the change in current to voltage characteristics of the transistors in a gate. The magnitude of the variation was very small. The results were similar to the variation seen for current generation (Figure 2). The amplitude of the voltage pulse reduced with temperature similar to the current amplitude reduction in Figure 2. The pulse amplitude at the output node OP decreases with increase in temperature for all the nodes considered. The pulse width at this node also decreases with temperature. In these cases, the effect of change in the VTC results in variation in pulse width and amplitude. As the pulse passes through different gates and reaches the output node of the path (Path_OP), the electrical masking effects of all cells gets added up. Thus the over-all effect of these cells can be

compared. In most paths, increase in temperature results in decrease in both amplitude and pulse width.

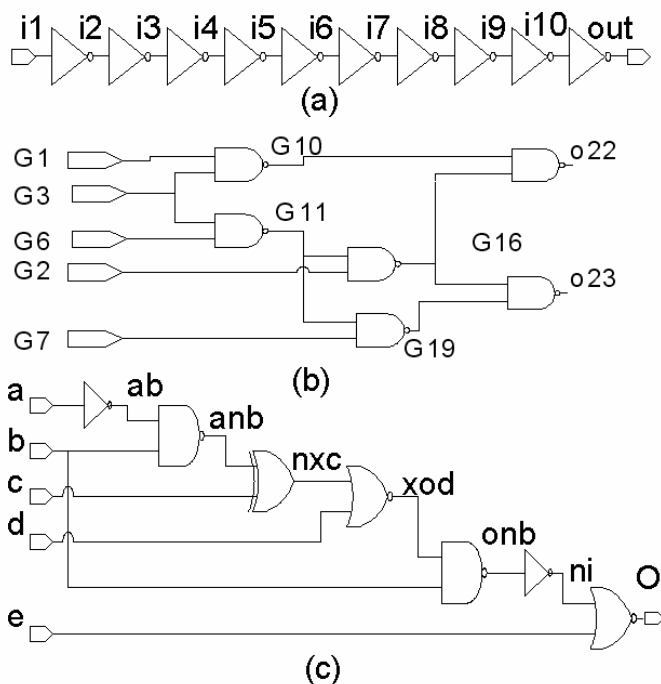


Figure 4 Circuit Schematics (a) inverter chain (b) C17 (c) Logic chain

To illustrate these effects, Figure 5 shows the effect of temperature on electrical masking for an inverter chain. A current pulse was injected at the input of third inverter ‘i3’. The pulses at the node ‘i7’ (input of the seventh inverter) and at the node ‘out’ (output of the last inverter) are shown for four different temperatures (25, 40, 70 and 100 °C). The pulse width measured for the node out is also shown. The topmost set of outputs in Figure 5 was for the lowest temperature and the bottommost was for the highest temperature. It is clear from the figure that the electrical masking effect increases with rise in temperature. Thus the pulse width at the output is smaller for higher temperature. Similar results were obtained for c17 and logic chain as well. The results are not shown here due to space constraints.

B. Voltage scaling effects

An analysis similar to the one in the previous section was done at lower voltages (0.8V and 0.6V). The pulse width at the injected node at lower voltages decreases with temperature unlike the increase in pulse-width at 1V. This is not intuitive although it is definitely due to the reduction in voltage which would definitely change the current to voltage transfer characteristics. The effect of electrical masking although remains the same and in fact increases as the reduction of pulse-width and amplitude at OP and Path_OP is more at lower voltages.

Figure 6 and 7 illustrates these effects of electrical masking at the lower voltages for an inverter chain. Similar to Figure 5, the pulse width reduces with increase in temperature. However, it is to be noted that lower the voltage, the bigger the

pulse width at each node for a similar current pulse. Also, the reduction in pulse width at lower voltages is also higher as seen in Figures 6 and 7. The results from C17 and logic chains also showed similar trends.

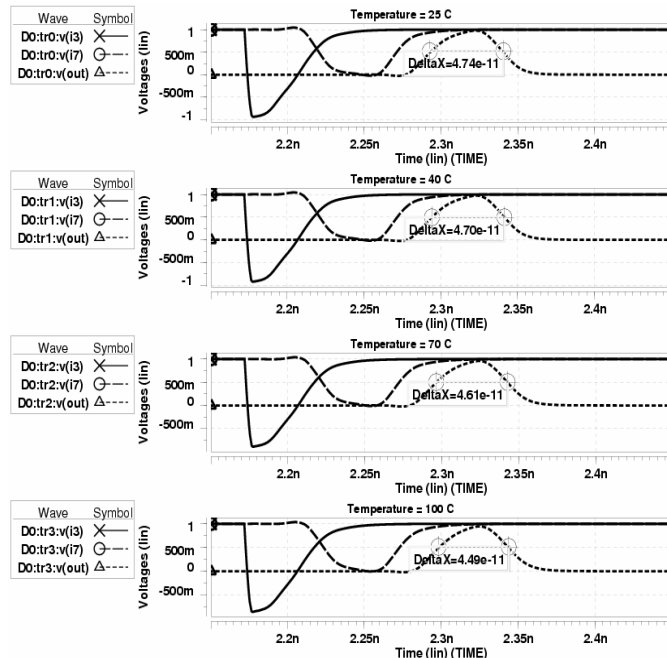


Figure 5 Temperature effect on electrical masking for an inverter chain

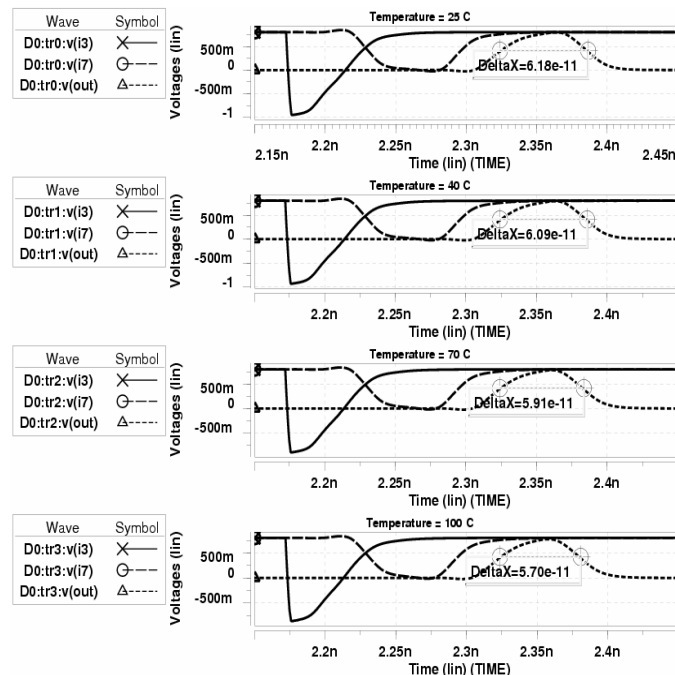


Figure 6 Temperature effect at 0.8V

V. CONCLUSIONS AND FUTURE WORK

This work studies the effect of both temperature and voltage scaling on electrical masking in logic circuits. These variations mainly affect the delay of circuits and which in turn affect electrical masking. Thus we have studied the effect of

such variations on VTC of an inverter. We have also presented our results on the variation of the pulse characteristics at different nodes in different circuits and analyzed the results. The results show that increase in temperature helps the electrical masking capability of circuits and hence will result in the reduction in soft error rates. At lower voltages, the masking capability due to increase in temperature is magnified even more, even though the pulses are much larger at lower voltages.

Apart from affecting the electrical masking, which is a function of cell delays, temperature and voltage variation also changes the latch window masking effects. The latch window masking is a strong function of the flip-flop set-up and hold times and their variation with temperature and voltage will be an interesting study for future work.

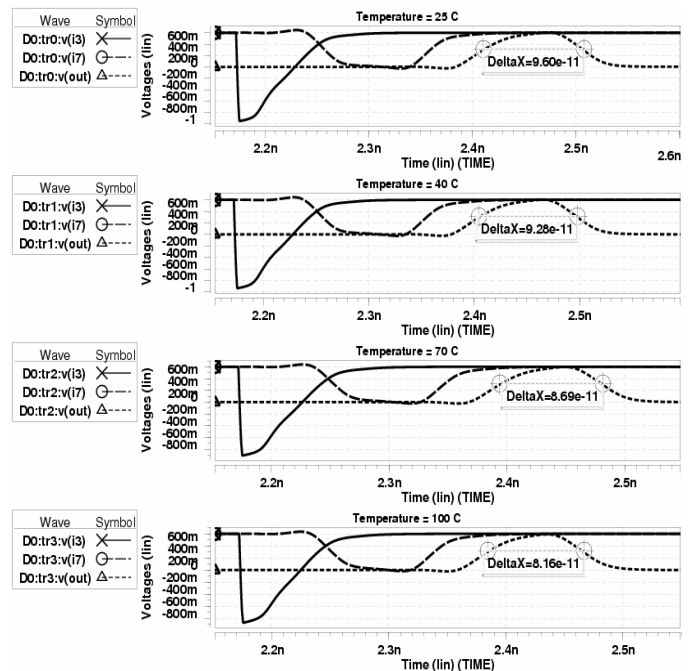


Figure 7 Temperature effect at 0.6V

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