

# A Crosstalk Aware Interconnect with Variable Cycle Transmission

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# Outline

- **Motivation**
- **Related work**
- **Crosstalk model**
- **Crosstalk analysis**
- **Crosstalk aware interconnect**
  - **Crosstalk analyzer**
  - **Variable cycle transmission**
- **Experimental results**
- **Conclusion**

# Motivation

- **Dramatic scaling in VLSI feature size.**
  - Propagation delay vs. gate delay.
  - Increased capacitive coupling.
- **Crosstalk noise between signals.**
  - Affect the timing of signals.
  - Increase cycle time.
  - Lead to performance degradation and functional failures.
- **High performance system design.**
  - Alleviating the impact of crosstalk.

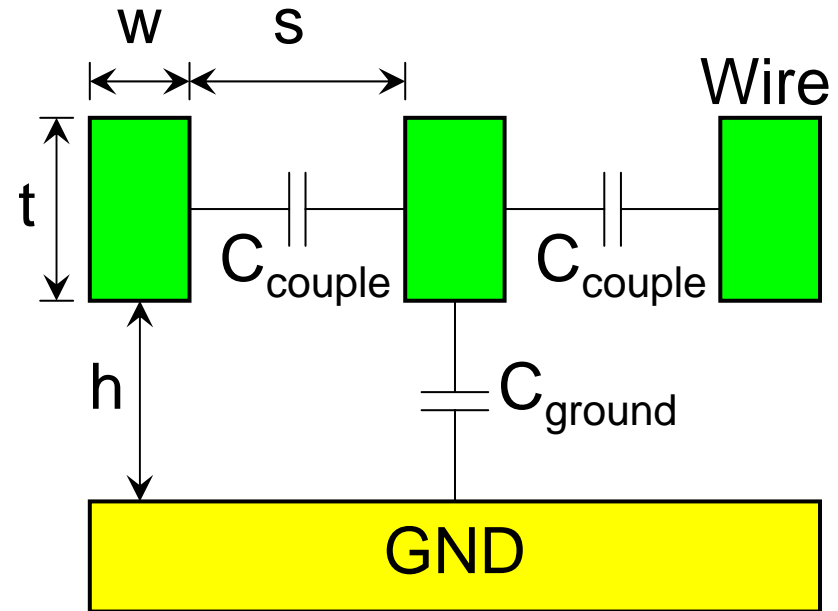
# Related Work

- **Net ordering and buffer insertion in physical design.**
- **Shielding and spacing schemes.**
- **Bus encoding to prevent crosstalk delay.**

# Crosstalk Model

- **$C_{\text{couple}}$  is decided by:**

- Technology parameters:  $w$ ,  $t$ ,  $s$ , and  $h$ .
- Transition directions of adjacent lines.

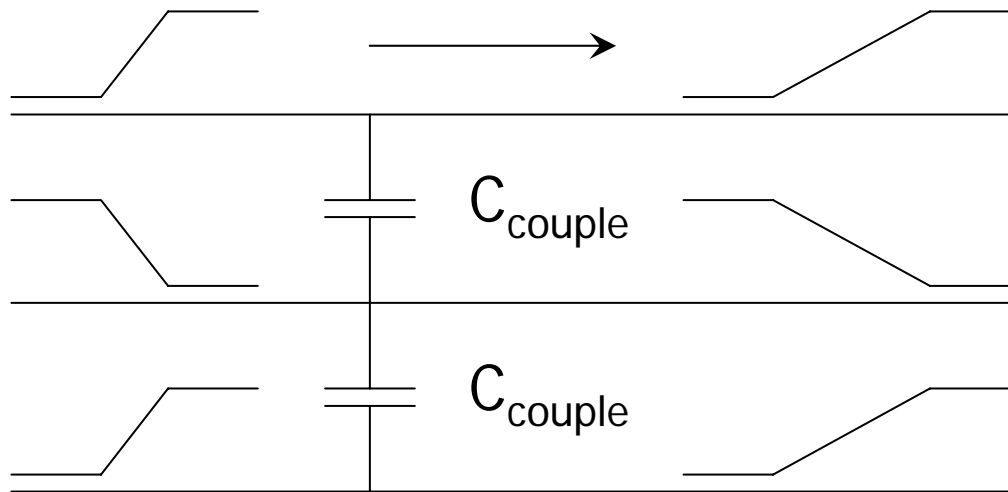


- **$C_{\text{couple}} \propto (h/s)$**

- With technology scaling, wire spacing is shrinking faster than wire height.
- $C_{\text{couple}}$  contributes to a larger portion of the total capacitance.

# Propagation Delay

$$T_{delay} \propto R_{total} * C_{total} = R_{total} * (C_{ground} + n * C_{couple})$$



- **$n$  depended on the transition of adjacent signals.**
- **Delay is longest when transitions of adjacent signals in opposite directions:**  
 $C_{total} = C_{ground} + 4 * C_{couple}$

# Crosstalk Analysis

- Different transmission patterns have different  $C_{total}$ , and then have different delay (concerning line k-1, k, k+1).

↑ : 0 → 1

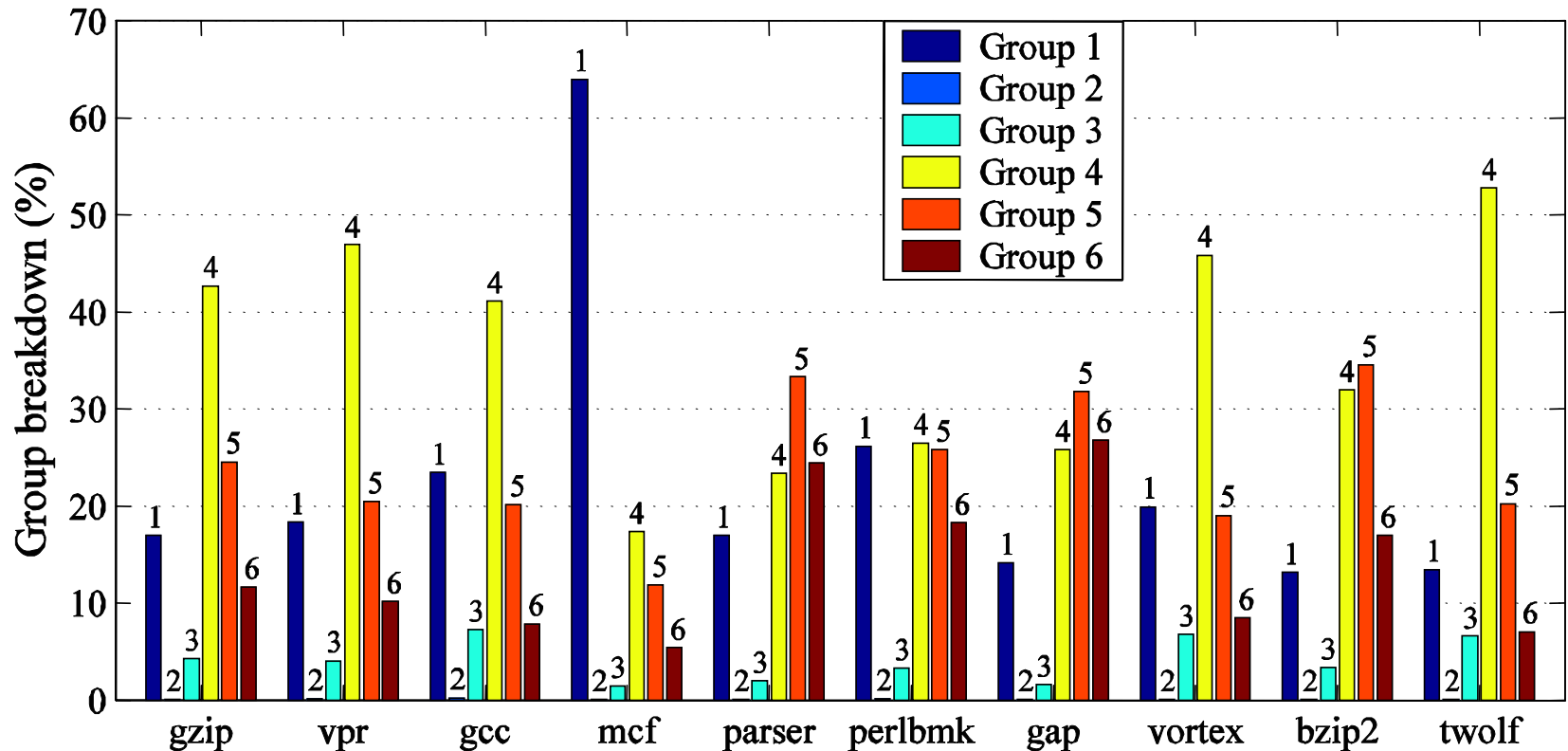
↓ : 1 → 0

— : not change

Group	$C_{total}$ of line k	Patterns			
1	0	— — — —			
		— — ↑	— — ↓	↑ — —	↓ — —
		↑ —	↑ —	↓ —	↓ —
2	$C_{ground}$	↑ ↑ ↑	↓ ↓ ↓	↑	↓
3	$C_{couple} + C_{ground}$	— ↑	— ↓	↑ ↑	↓ ↓
4	$2 * C_{couple} + C_{ground}$	— ↑ —	— ↓ —	—	—
		↑ ↑	↑ ↓	↓ ↑	↓ ↓
5	$3 * C_{couple} + C_{ground}$	— ↓ ↑	— ↓ ↓	↑ ↑ ↓	↓ ↑ ↑
6	$4 * C_{couple} + C_{ground}$	↑ ↓ ↓	↓ ↑ ↑	—	—

Ref: “Reducing bus delay in submicron technology using coding”,  
P. Sotiriadis and A. Chandrakasan, ASP-DAC’01.

# Crosstalk Analysis (Cont.)

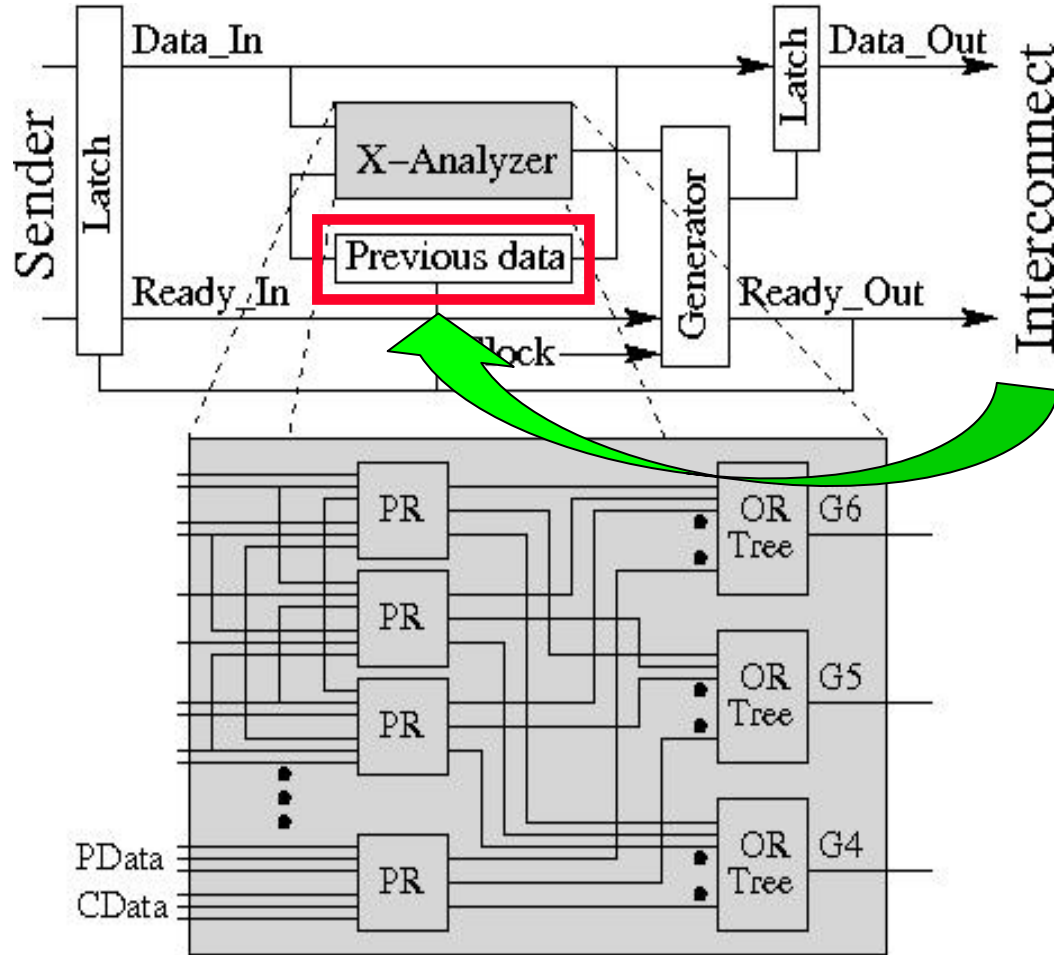


- Average distributions are 22.64%, 0.05%, 4.06%, 35.4%, 24.2%, and 13.7% for Group 1 to 6.
- The worst case (Group 6) is not the dominant case.
- Group 2 includes only two transmission pattern:  
 ↑ ↑ ↑ ... ↑ ↑ ↑ and ↓ ↓ ↓ ... ↓ ↓ ↓ .

# Observation

- **Original interconnect**
  - **Bus clock cycle is designed for the worst-case scenario of crosstalk.**
  - **Many transmissions may incur a shorter delay than that of the worst case.**
- **Proposed interconnect**
  - **Use multiple short clock cycles instead of the original long clock cycle.**
  - **The number of clock cycles is determined based on the delay group.**

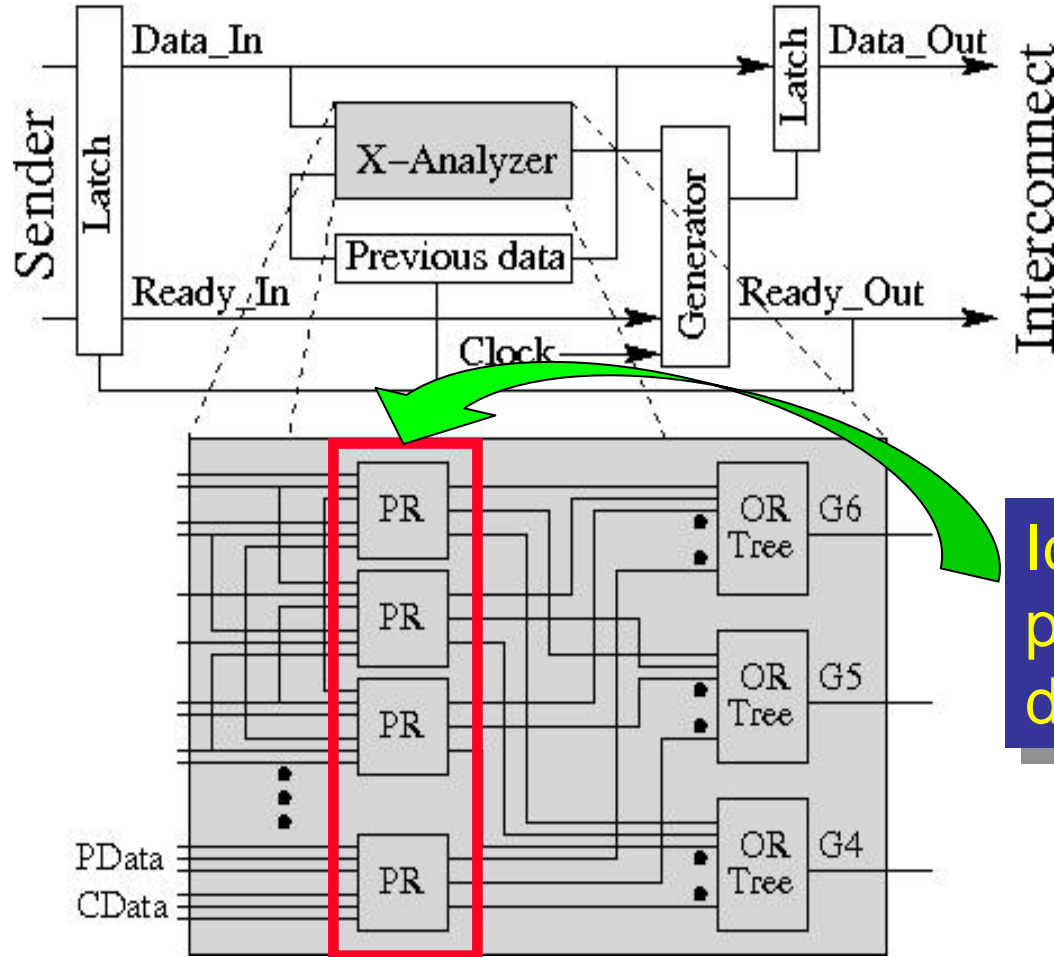
# Crosstalk Analyzer



Delay determined by the transition between data transmitted in the previous and current cycles.

Using a register to store the previous data.

# Crosstalk Analyzer

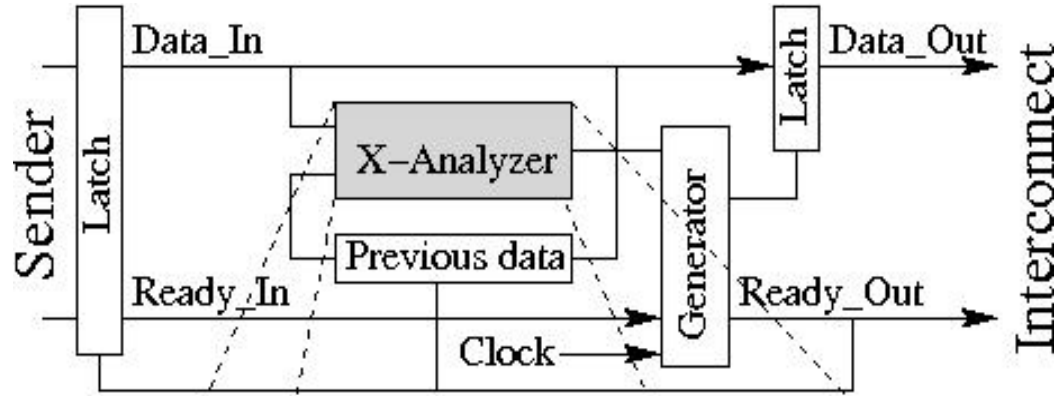


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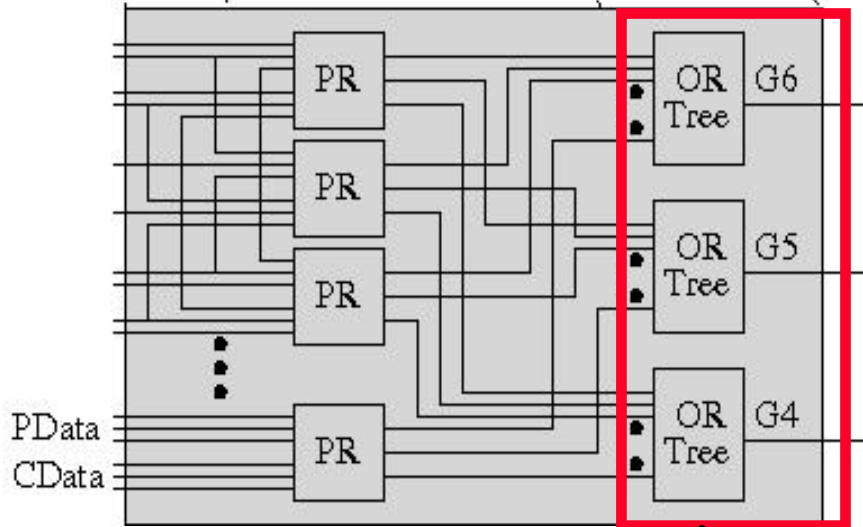
Identifies the transition pattern and determines the delay group.

# Crosstalk Analyzer



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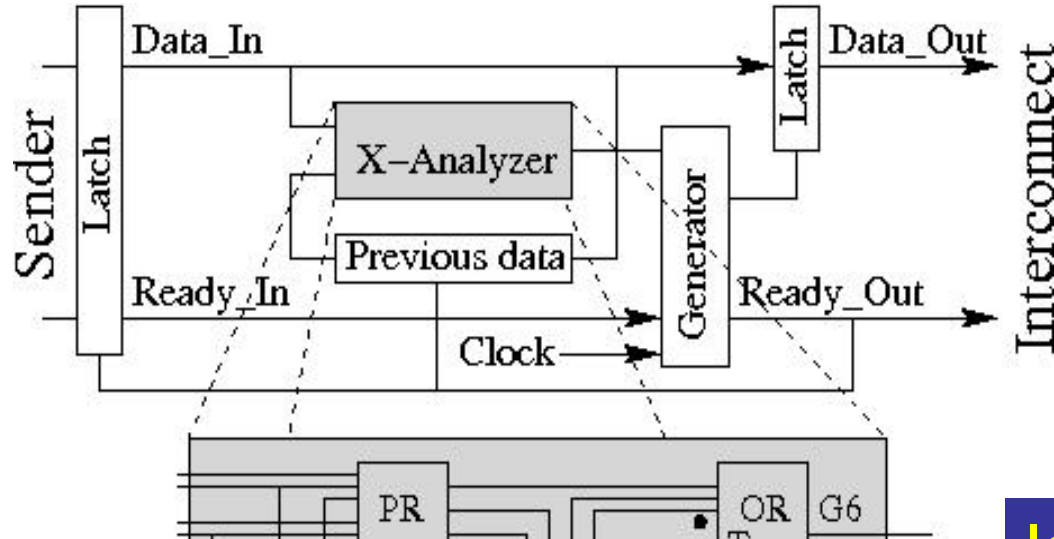
Using a register to store the previous data.



Identifies the transition pattern and determines the delay group.

The wire that belongs to the largest group determines the delay of the entire 32-bit bus.

# Crosstalk Analyzer



The impact of crosstalk is captured by the sender before the transmission begins.

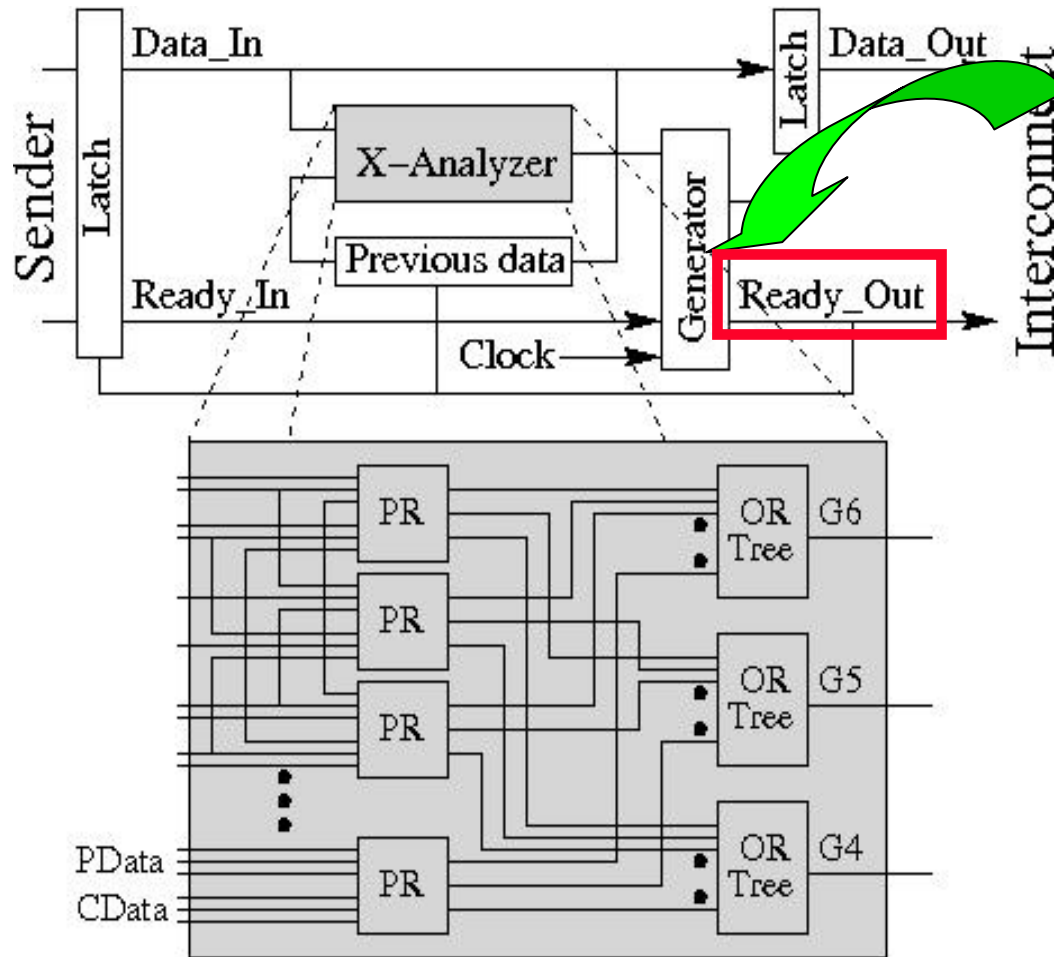
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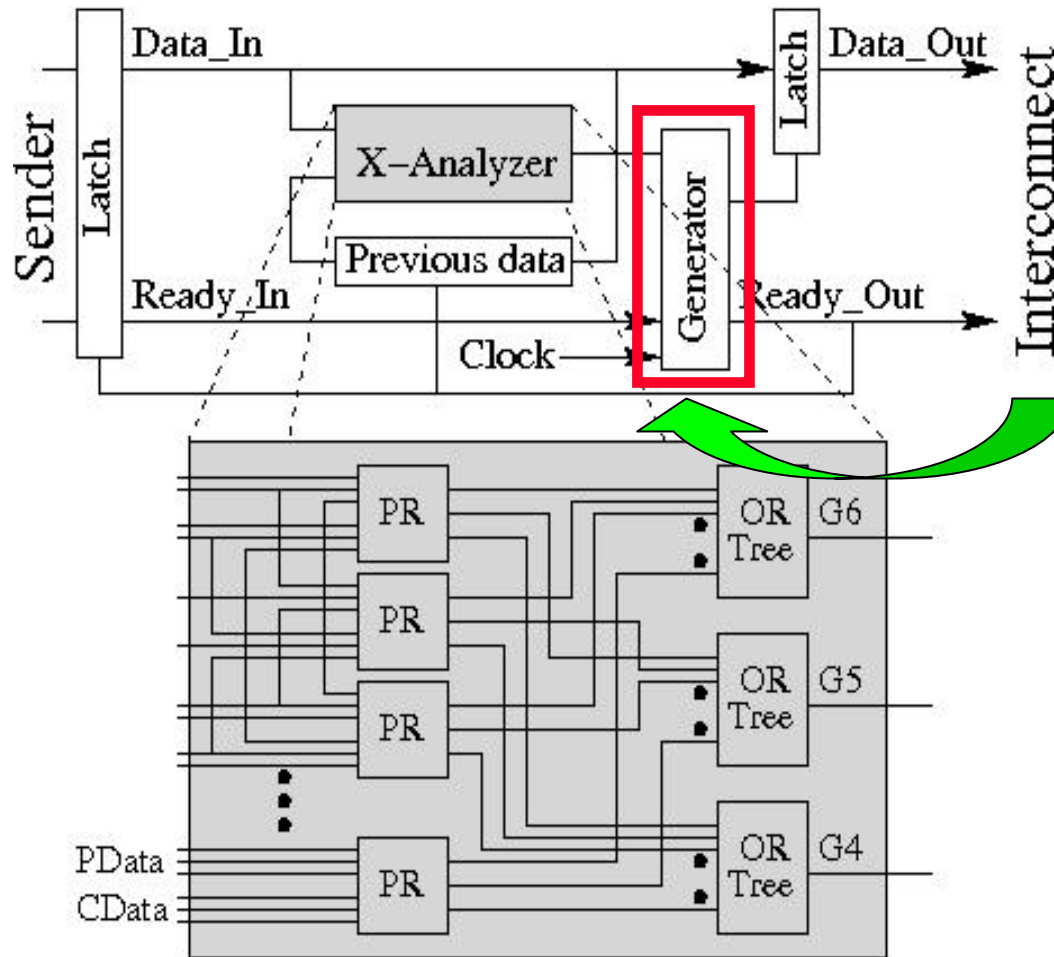
The wire that belongs to the largest group determines the delay of the entire 32-bit bus.

# Crosstalk Aware Interconnect



Control signal informs receiver whether data is ready.

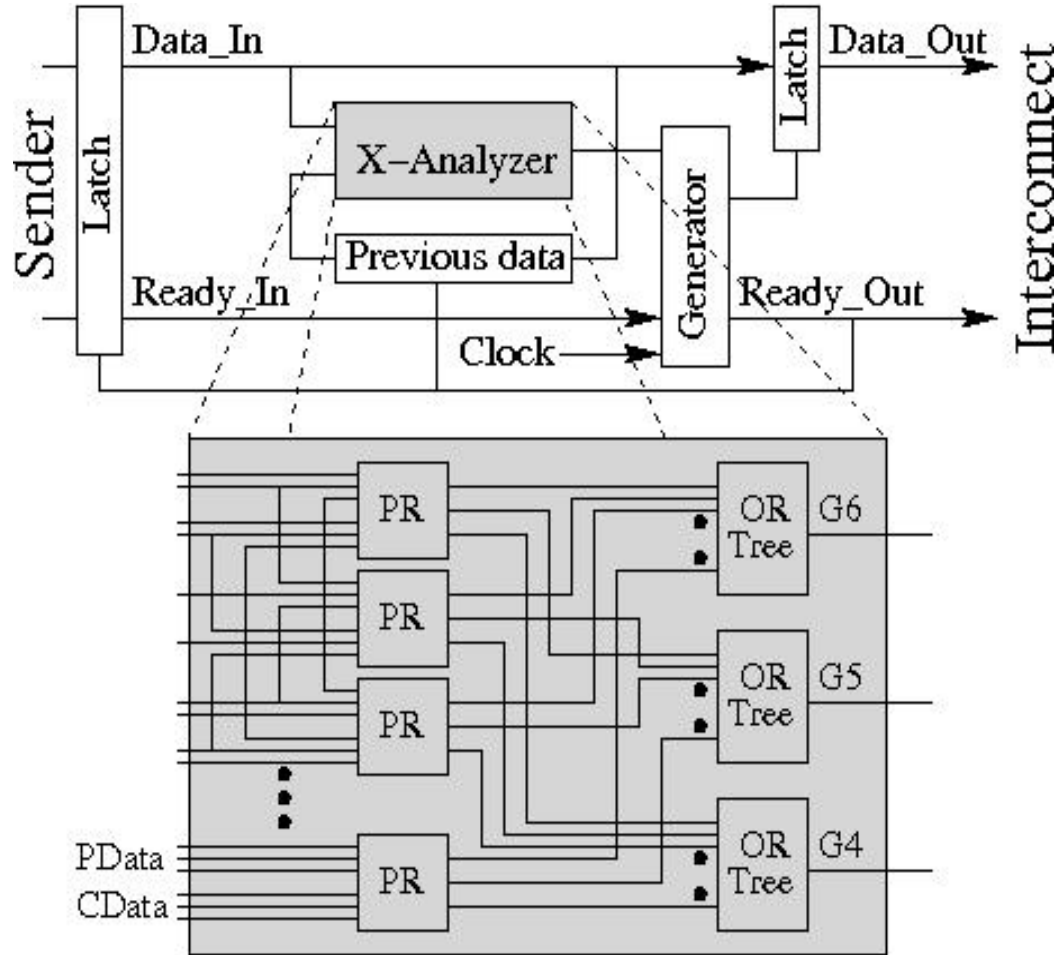
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Control signal informs receiver whether data is ready.

Dynamically change the cycles used to transmit data based on the output of X-analyzer.

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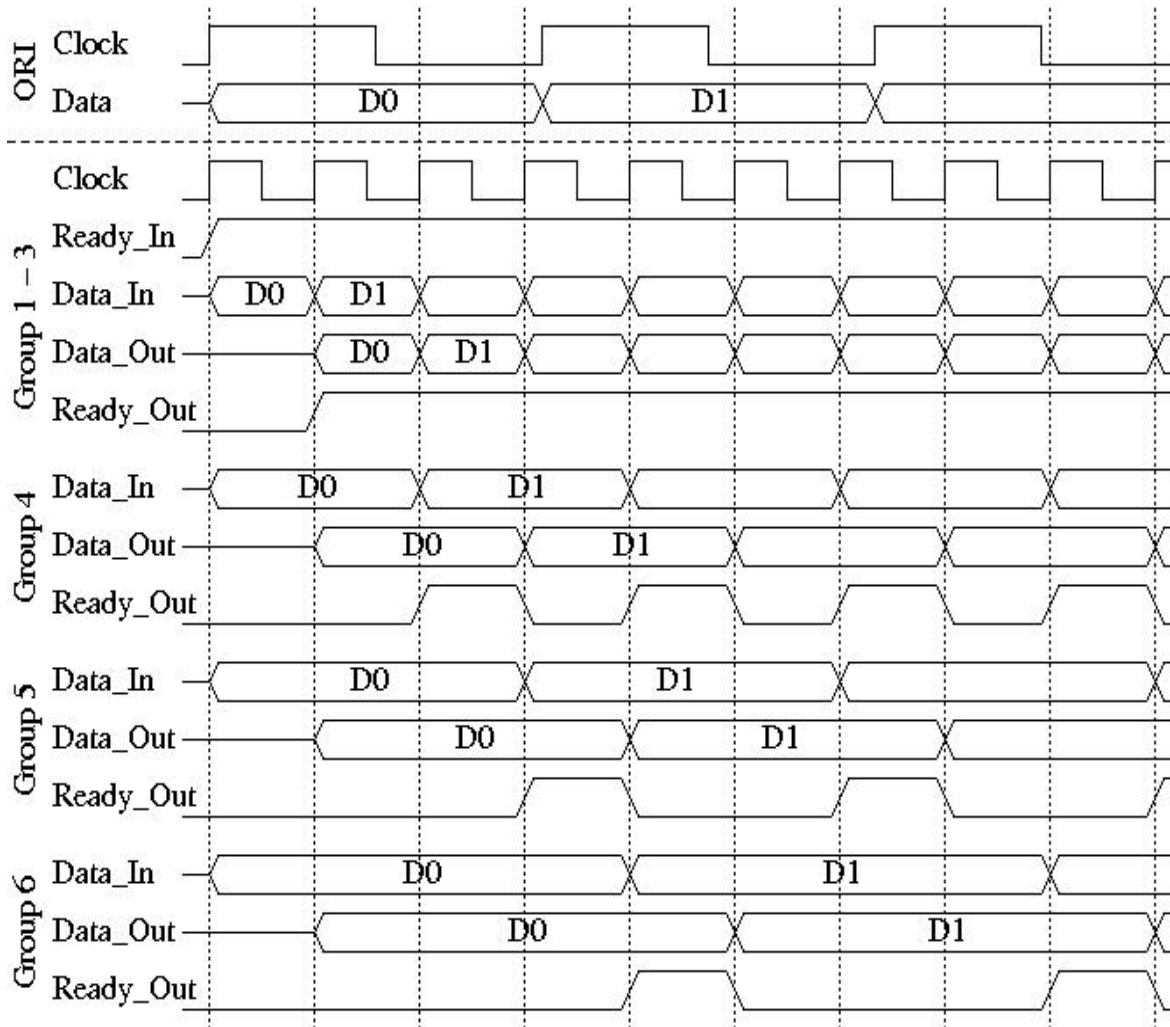


Control signal informs receiver whether data is ready.

Dynamically change the cycles used to transmit data based on the output of X-analyzer.

X-analyzer incurs one cycle latency, but it can be overlapped by fetching next data.

# Variable Cycle Transmission

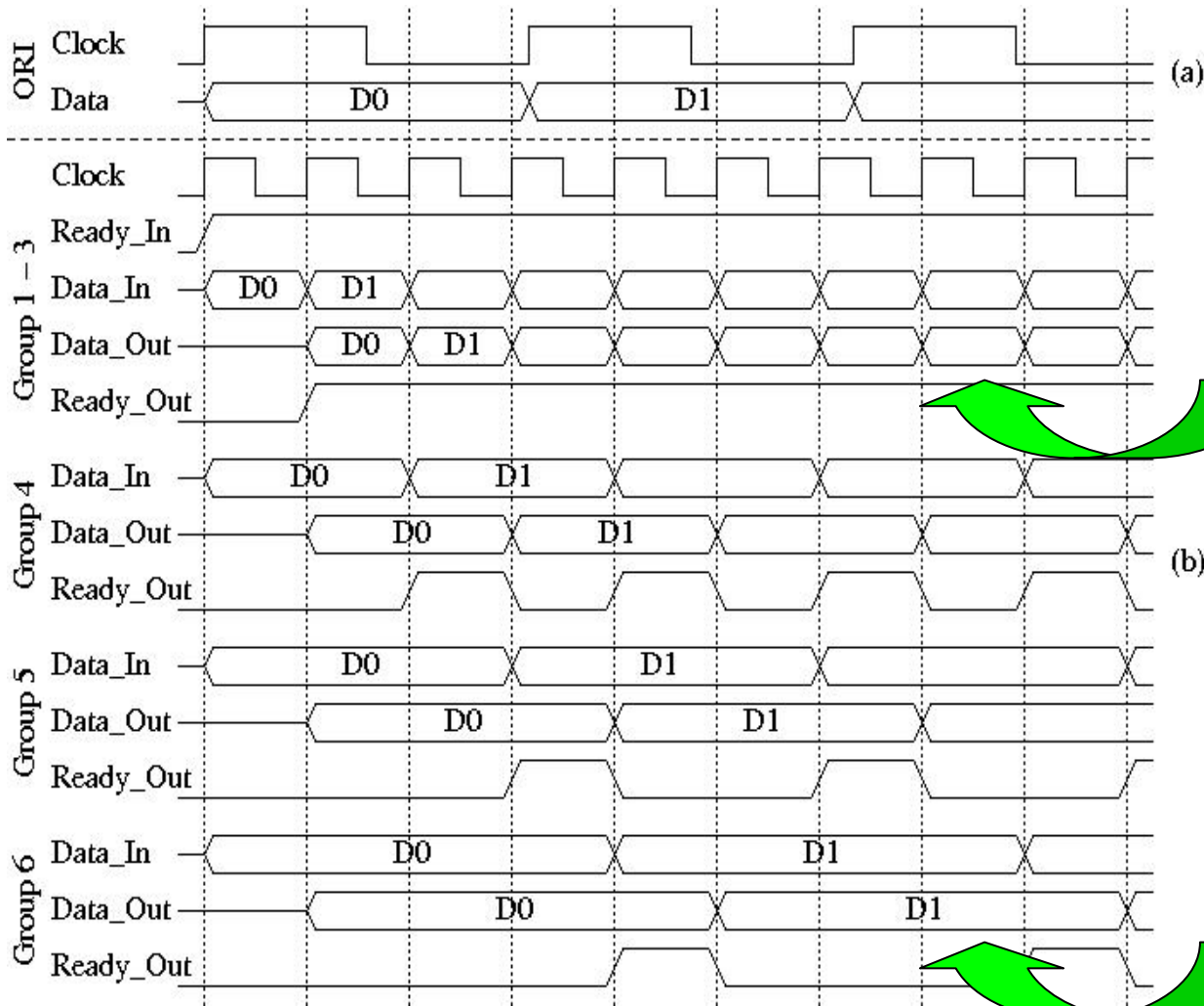


Original (ORI):  
Long clock cycle for  
all transmissions.

$$\frac{T_{clk-dyn}}{T_{clk-ori}} = \frac{C_{ground} + C_{couple}}{C_{ground} + 4 * C_{couple}}$$

Proposed (DYN):  
Different # of short  
clock cycles for  
different groups.

# Variable Cycle Transmission



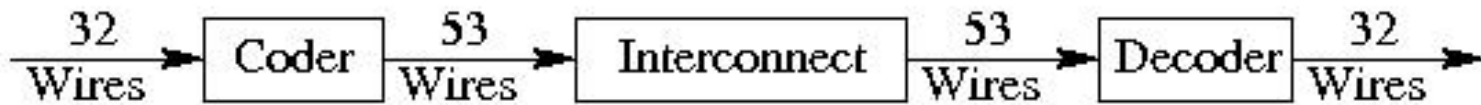
One cycle per transmission for group 1-3.

Four cycles per transmission for group 6.

# Schemes for Comparison

Crosstalk  
Prevention Coding

CPC



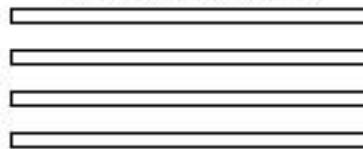
Interconnect



ORI

Original  
Interconnect

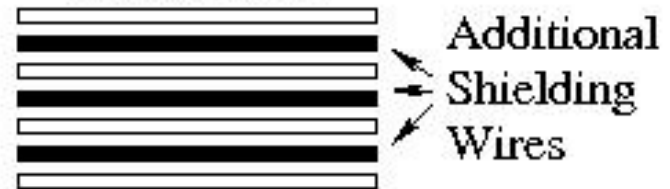
Interconnect



DBS

Double  
Spacing

Interconnect



SHD

Shielding

# Characteristics of Schemes

	$C_{\text{ground}}$ (fF/mm)	$C_{\text{couple}}$ (fF/mm)	# of wires	Normalize cycle time
ORI	36.3	115.1	32	3.28
CPC	36.3	115.1	53	2.76
<b>DYN</b>	<b>36.3</b>	<b>115.1</b>	<b>33</b>	<b>1.00</b>
DBS	53.1	60.4	32	1.95
SHD	36.3	115.1	63	1.76

Different  $C_{\text{ground}}$  and  $C_{\text{couple}}$  due to different space between wires.

Coupling capacitance contributes to a large portion of the total capacitance.

	Normalized Area			Extra Energy
	2mm	5mm	10mm	
ORI	100	100	100	
CPC	174	170	168	12.6mW
<b>DYN</b>	<b>132</b>	<b>113</b>	<b>106</b>	<b>32.1mW</b>
DBS	149	149	149	
SHD	198	198	198	

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Large overhead of extra wires for CPC and SHD.

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Normalized to the cycle time of DYN.

Reflect the worst case crosstalk in ORI, CPC, DBS, and SHD.

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2mm: short interconnect.

5mm: medium interconnect.

10mm: long interconnect.

Areas are normalized to the size of ORI with different length.

	Normalized Area			Extra Energy
	2mm	5mm	10mm	
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DYN has the smallest area overhead, while SHD has the largest area overhead.

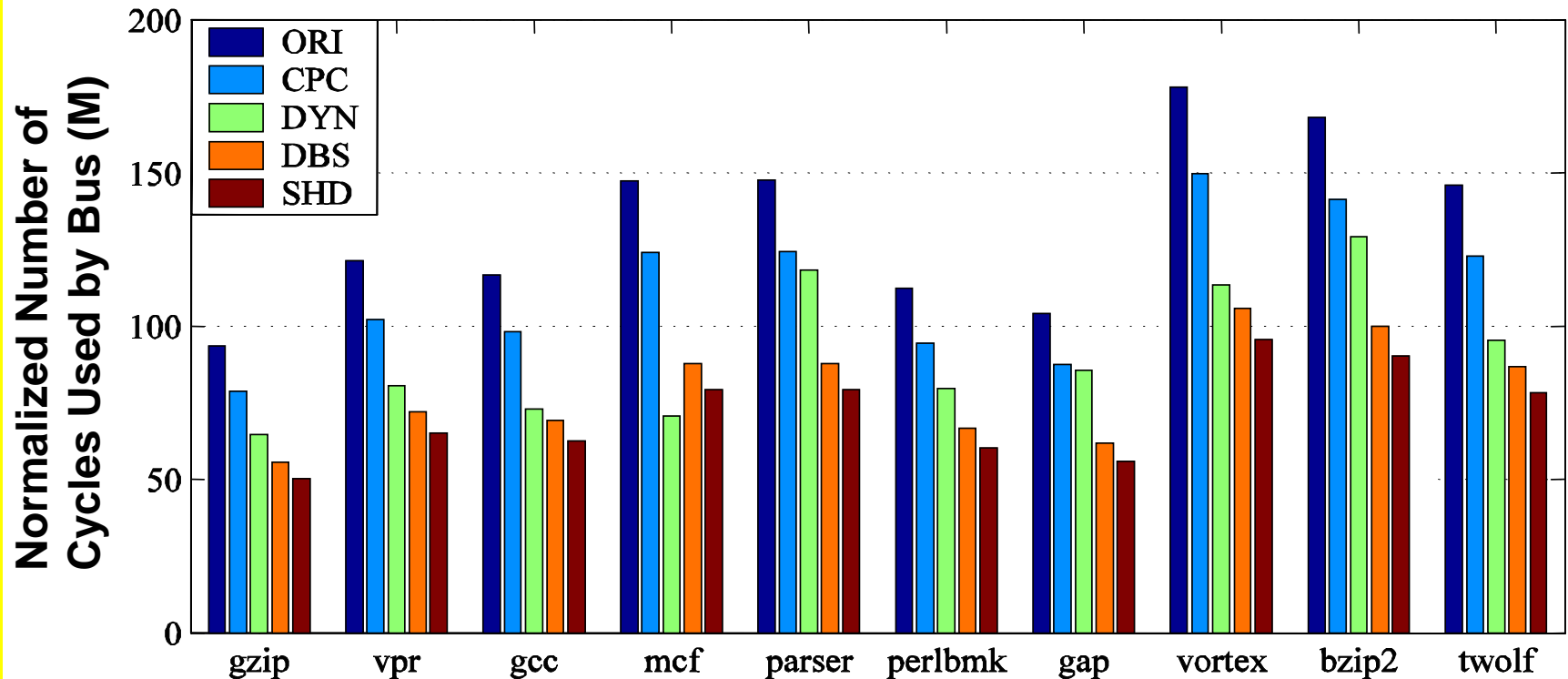
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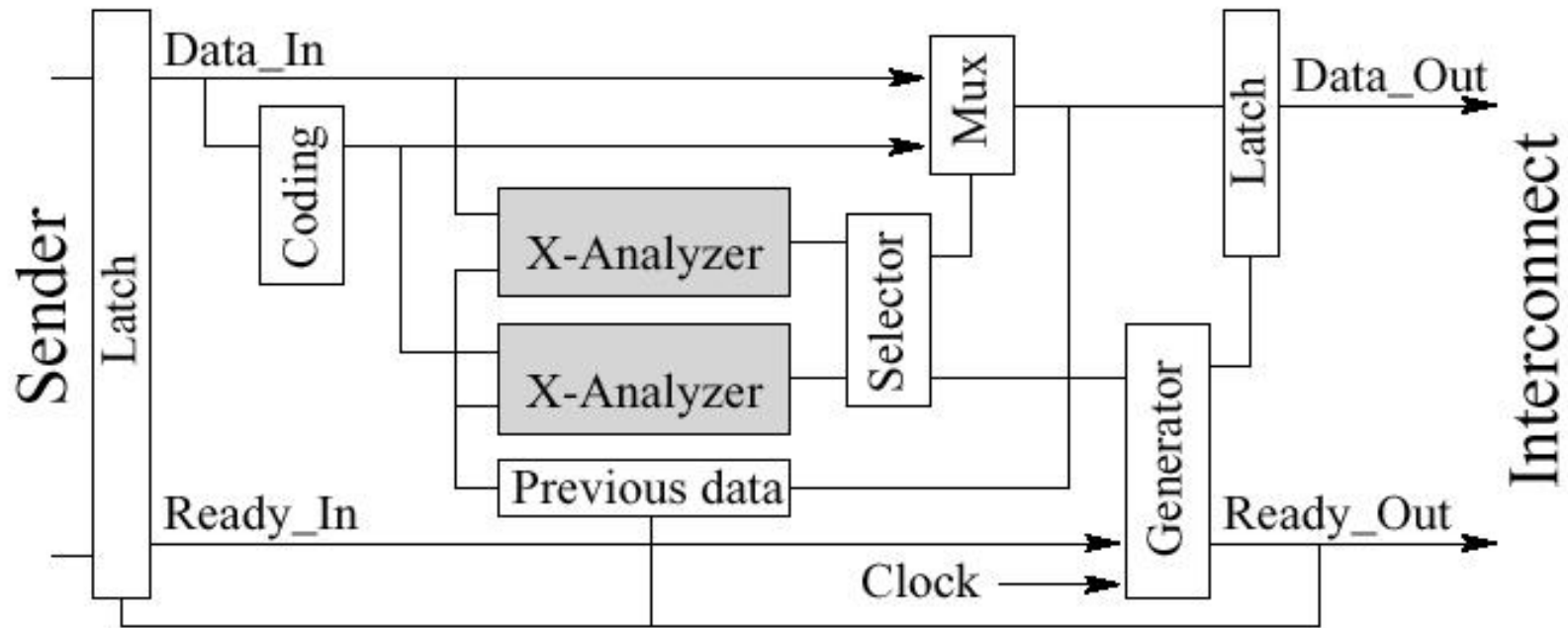
Extra energy consumed by coder and decoder.

# Performance Result



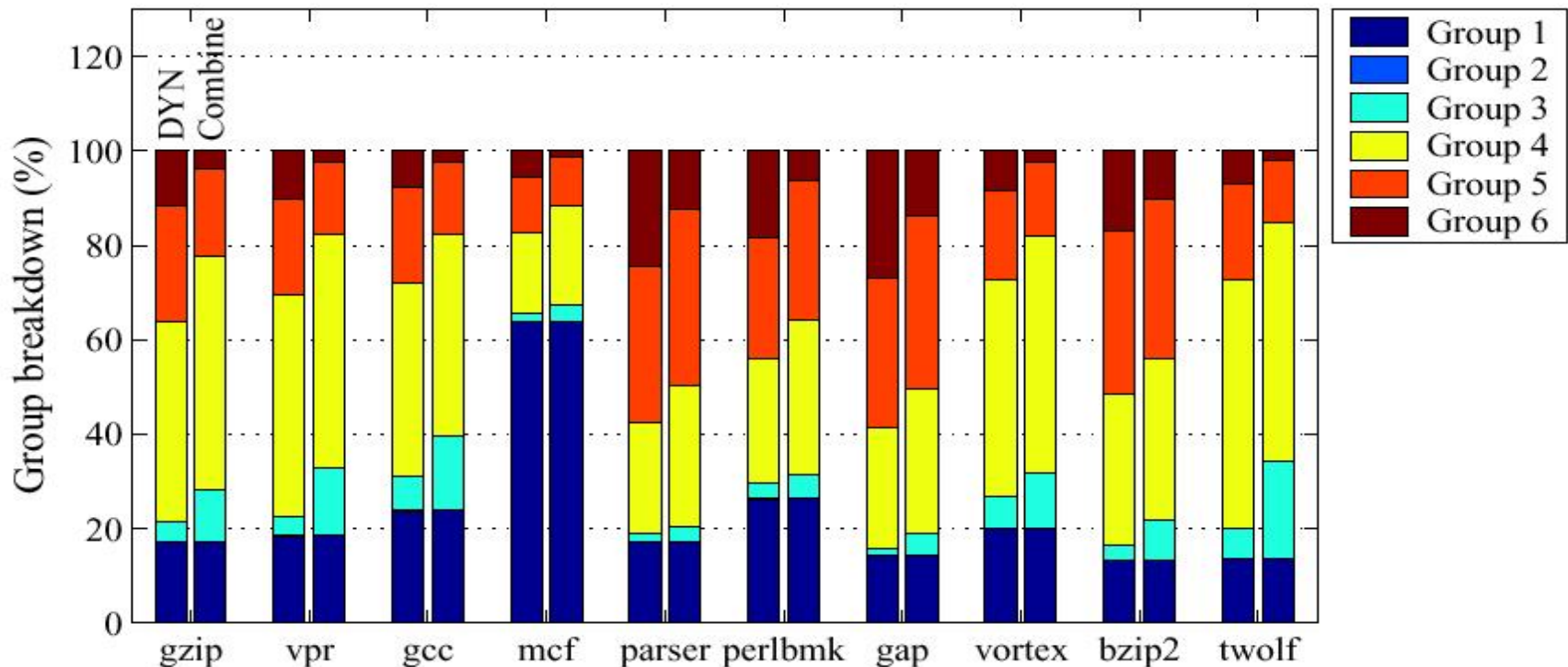
- **Dynamic approach provides an average of 31.5% performance improvement over the original scheme.**
- **It is a tradeoff between performance and area overhead.**

# Combining with Bus-Invert



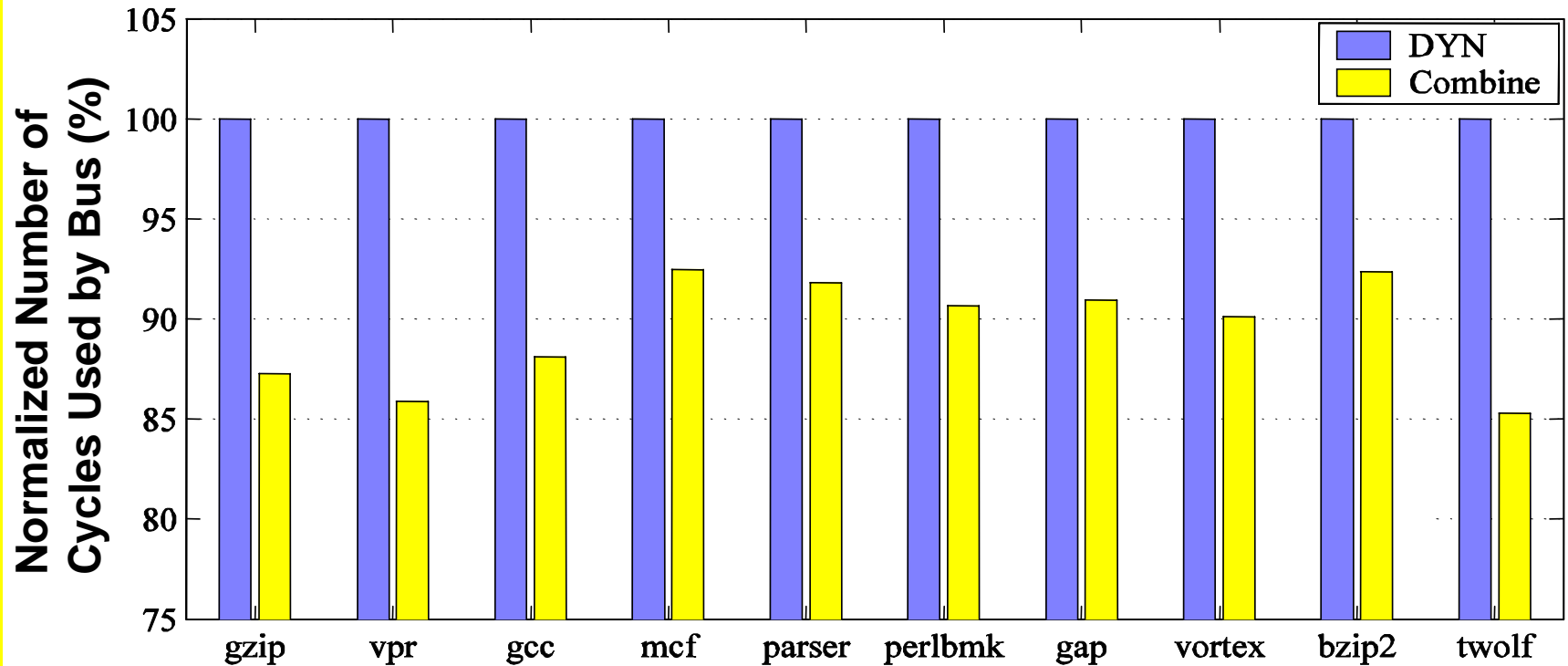
- Using Bus-Invert to get more transitions in Groups 1 to 3.
- Using two crosstalk analyzers.

# Distribution of Patterns



- Increase transmissions in Groups 1, 3, and 4 by 0.06%, 5.9%, and 3.8%, respectively.
- Reduce transmissions in Groups 5 and 6 by 1.6% and 8.0%, respectively.
- Group 2 is very hard to distinguish in the figure due to very small value.

# Performance Result



**The combined method has 10.5% of performance improvement over DYN.**

# Conclusion

- **Crosstalk induced delays are transition dependent.**
- **Designing bus cycle times based on worst-case crosstalk is overly pessimistic.**
- **We design a crosstalk aware interconnect**
  - **Use a faster clock.**
  - **Estimate the delay of the data pattern to be transmitted.**
  - **Dynamically control the number of cycles required for transmission.**

Thanks !

Questions?