

The Effect of Threshold Voltages on the Soft Error Rate

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Outline

- Introduction
 - Soft Errors
- High Threshold (V_{+})
 - Charge Creation
 - Logic Attenuation
- Methodology
 - Flip-Flops, SRAM
 - Logic chain- Inverter & Nands
- Results
 - Flip-flops
 - SRAMs
 - Combinational logic

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Soft Errors

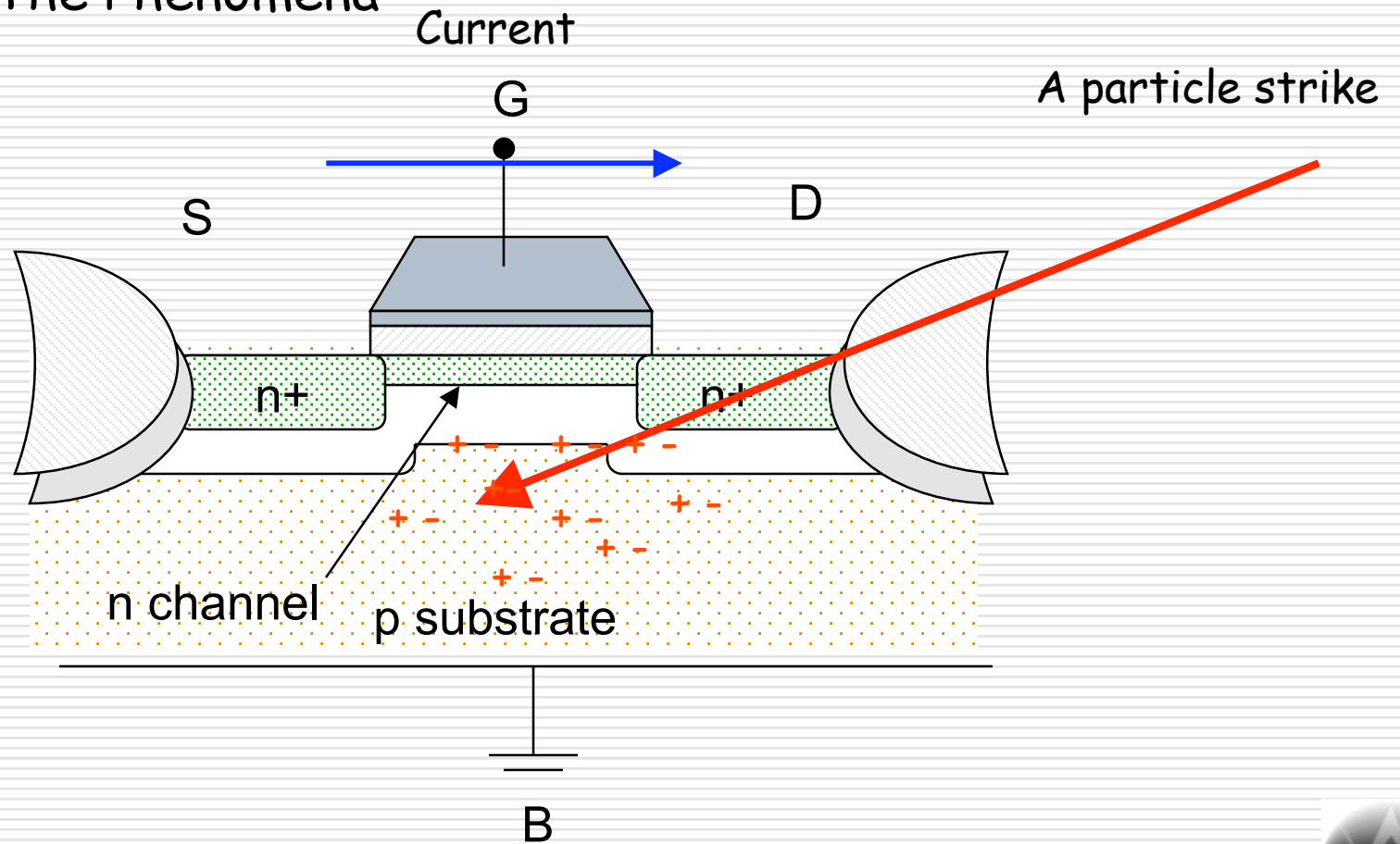
- ❑ Soft errors or transient errors are circuit errors caused due to excess charge carriers induced primarily by external radiations
- ❑ These errors cause an upset event but the circuit it self is not damaged.

Soft Errors: Sources

- At ground level, there are three major contributors to Soft errors.
 - **Alpha particles** emitted by decaying radioactive impurities in packaging and interconnect materials.
 - **Cosmic Ray induced neutrons** cause errors due to the charge induced due to Silicon Recoil
 - **Neutron induced ^{10}B fission** which releases a Alpha particle and ^7Li

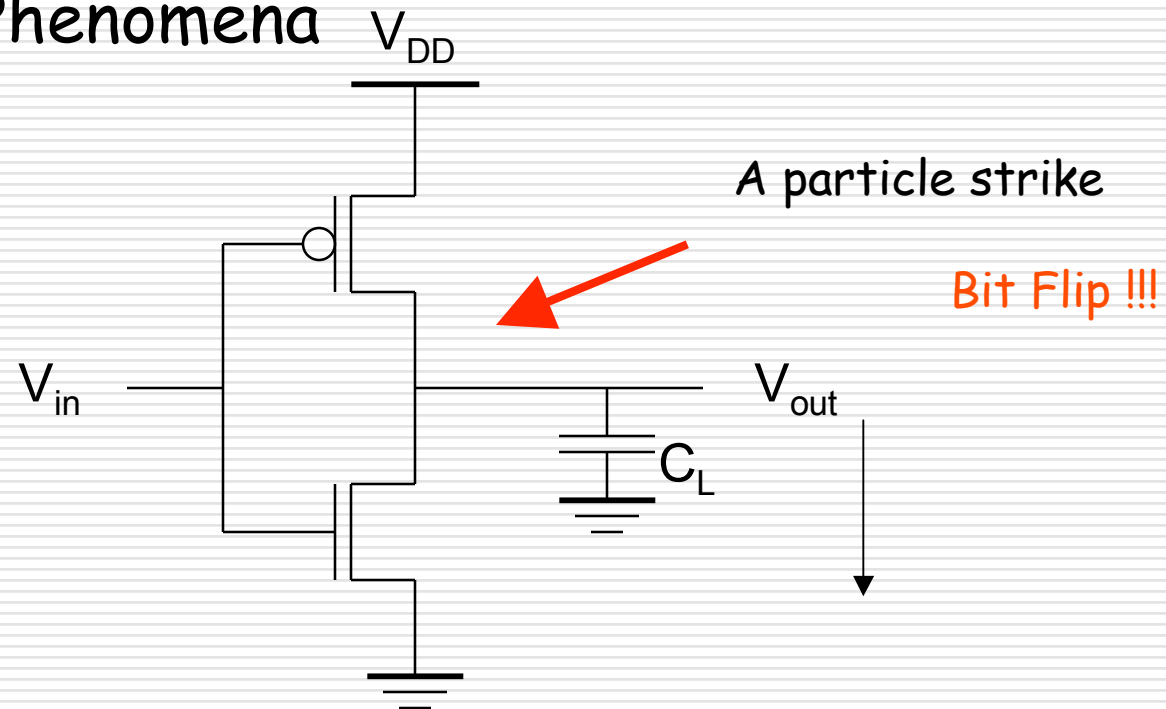
Soft Errors

- The Phenomena



Soft Errors

■ The Phenomena



Soft Errors

- ❑ For a soft error to occur at a specific node in a circuit, the collected charge Q at that particular node should be more than Q_{critical}
- ❑ As CMOS device sizes *decrease*, the charge stored at each node *decreases* (due to lower nodal capacitance and lower supply voltages).
- ❑ This potentially leads to a much *higher* rate of soft errors

Soft Errors

- Soft Errors can cause problems in 3 different ways
 - Affects the memory like **Caches** and **Memory**
 - Affects the **data path** if the error propagates to the **pipeline registers**.
 - Change the character of a SRAM-Based FPGA circuit.(Firm Error)

Is it important?

agere^{systems}

SER vs. Applications

Application	Embedded SRAM (Mbits)	System			SER Critical
		# of Chips	FITs ^{1,2}	%/yr. Fail ¹	
Storage Area Network Inline Circuit Extender	10	2	2E4	17.5	Yes
Network Processors	50	64	32E5	100	Yes
Cell Phone - Base Station	14	12	17E4	100	Yes
Cell Phone - Terminal	20	1	2E4	17.5	No
Disk Drive SOC ASIC - High End Drives	5	1	5E3	4.4	Yes
Disk Drive SOC ASIC - PC Drives	1	1	1E3	0.9	No

¹ at 1000 FITs/Mbit

² Customer request as low as 50 to 2000 FITs SER per chip

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Charge creation

- $V_t = V_{fb} + V_b + V_{ox}$

where, V_t is the threshold voltage, V_{fb} is the flat band voltage, V_b is the voltage drop across the depletion region at inversion, V_{ox} stands for potential drop across the gate oxide

- By increasing the threshold voltage, we increase the energy required to push the electrons up the valence band

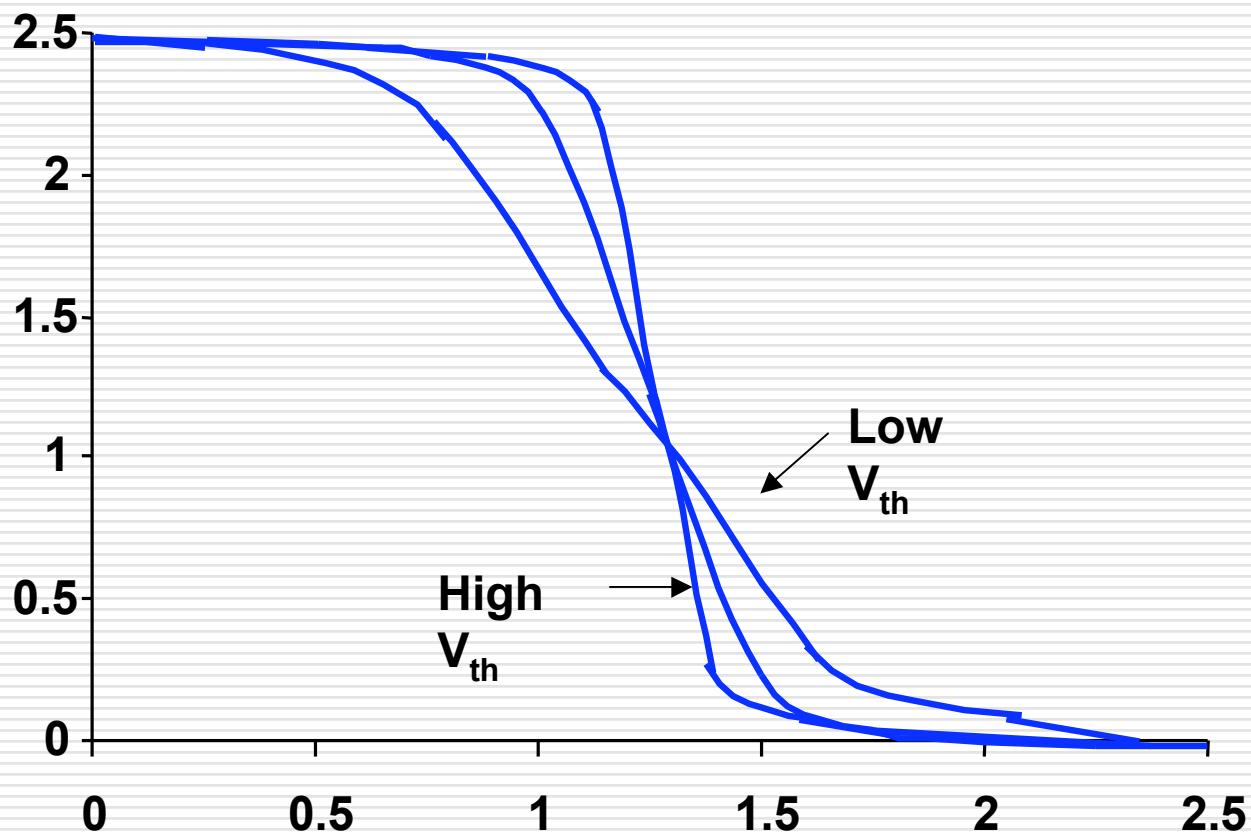
Logic attenuation under high V_T

- Gain G is given by

$$G = \frac{(1+r)}{(V_M - V_T - V_{DSat}/2)(\lambda_n - \lambda_p)}$$

Where, r is switching threshold, V_m is half of supply voltage, V_{dsat} is drain saturation current, and λ_n , λ_p are channel length modulation factors for n-channel and p-channel

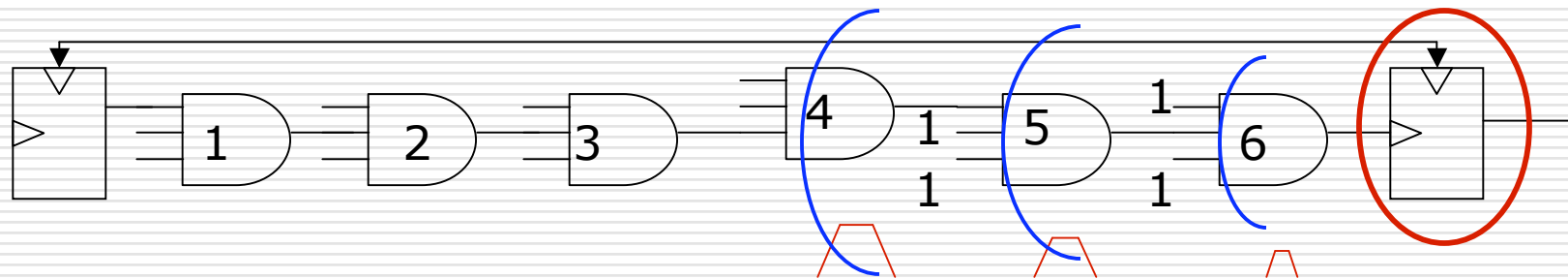
Logic attenuation under high V_t



Logic attenuation under high V_{\dagger}

- higher gain, hence a transient pulse will propagate in a system for a longer time and travels more logic stages.
- but the circuit will be slower!

Logic attenuation- 'Hazard Bubble'



Clock

**Flip flop/
Latch**

Gate 6

Gate 5

Gate 4

Setup Hold

**Window of
Vulnerability**

Error Masking

- ❑ **Logical masking** : A particle strikes a portion of the combinational logic that doesn't determine output.
- ❑ **Electrical masking** : The pulse resulting from a particle strike is attenuated by subsequent logic gates.
- ❑ **Latching-window masking** : The pulse resulting from a particle strike reaches a latch, but not at the clock transition.

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Test Circuits and Methodology

- ❑ Used Flip-flops -TGFF, C2MOS, SRAMS, 6inverter chain, FO4 Nand chains with FFs to latch errors.
- ❑ Layout in 70 nm BPT models, simulated in Hspice
- ❑ Transient Pulse modeled as current pulse with a sharp rise and slow decay
- ❑ Pulse only at nodes which produce change in output (No logic masking)
- ❑ Measuring metric: $Q_{critical}$

Soft Errors

□ $SER = N_{flux} * CS * \exp(Q_{critical} / Q_s)$ [Hazucha, 2000]

■ N_{flux} - Neutron Flux

■ CS - Cross Sectional area

■ $Q_{critical}$ - Critical charge necessary for a Bit Flip

■ Q_s - Charge Collection Efficiency

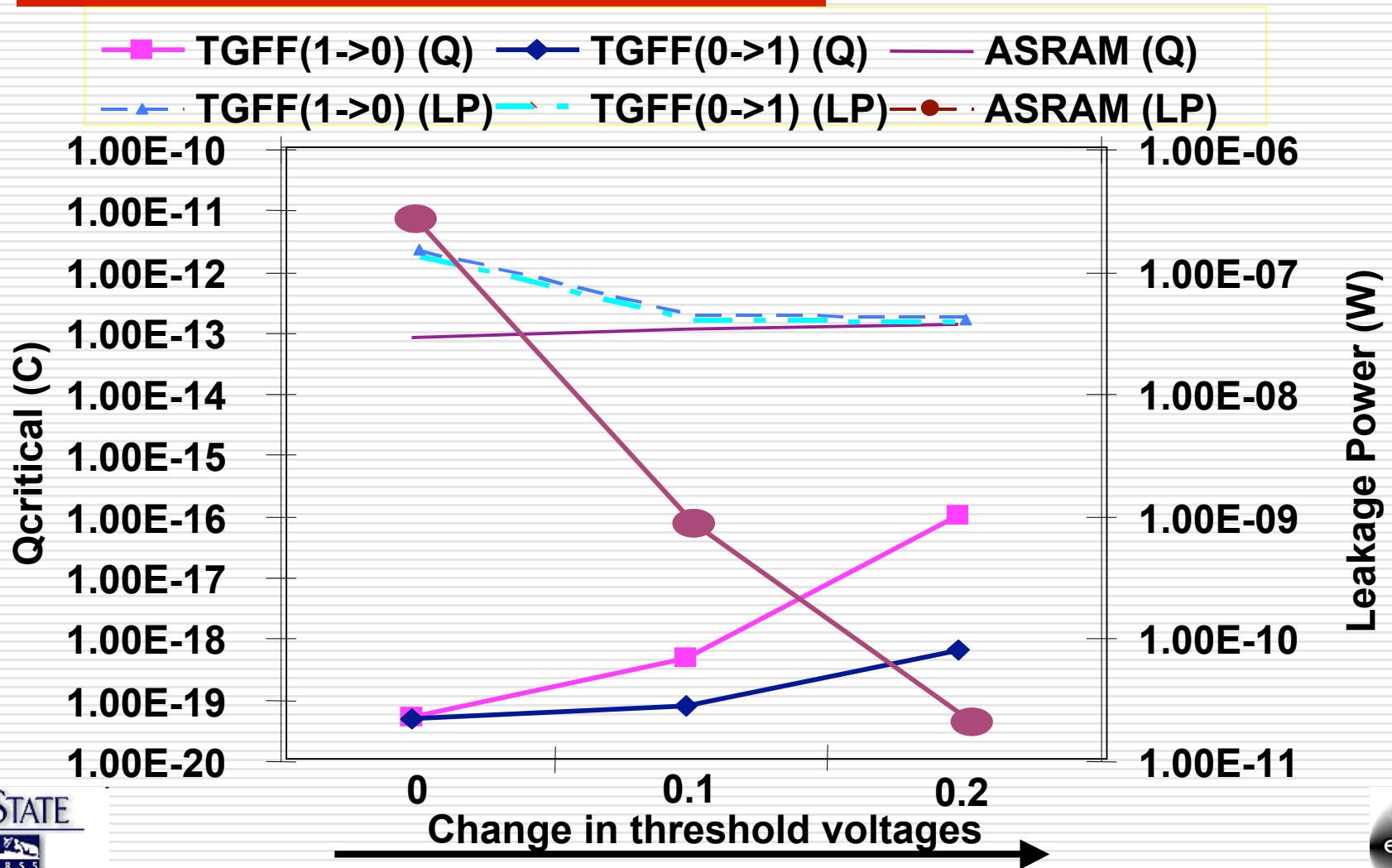
□ $Q_{critical} = \int_0^{I_f} I_d dt,$

■ I_d = Drain Current

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Results



Results

- Generally for Flip Flops & SRAMs
 - Q_{critical} increase with higher V_{t}
 - Q_{critical} for 0- \rightarrow 1 higher than 1- \rightarrow 0
 - Leakage decreases with higher V_{t}

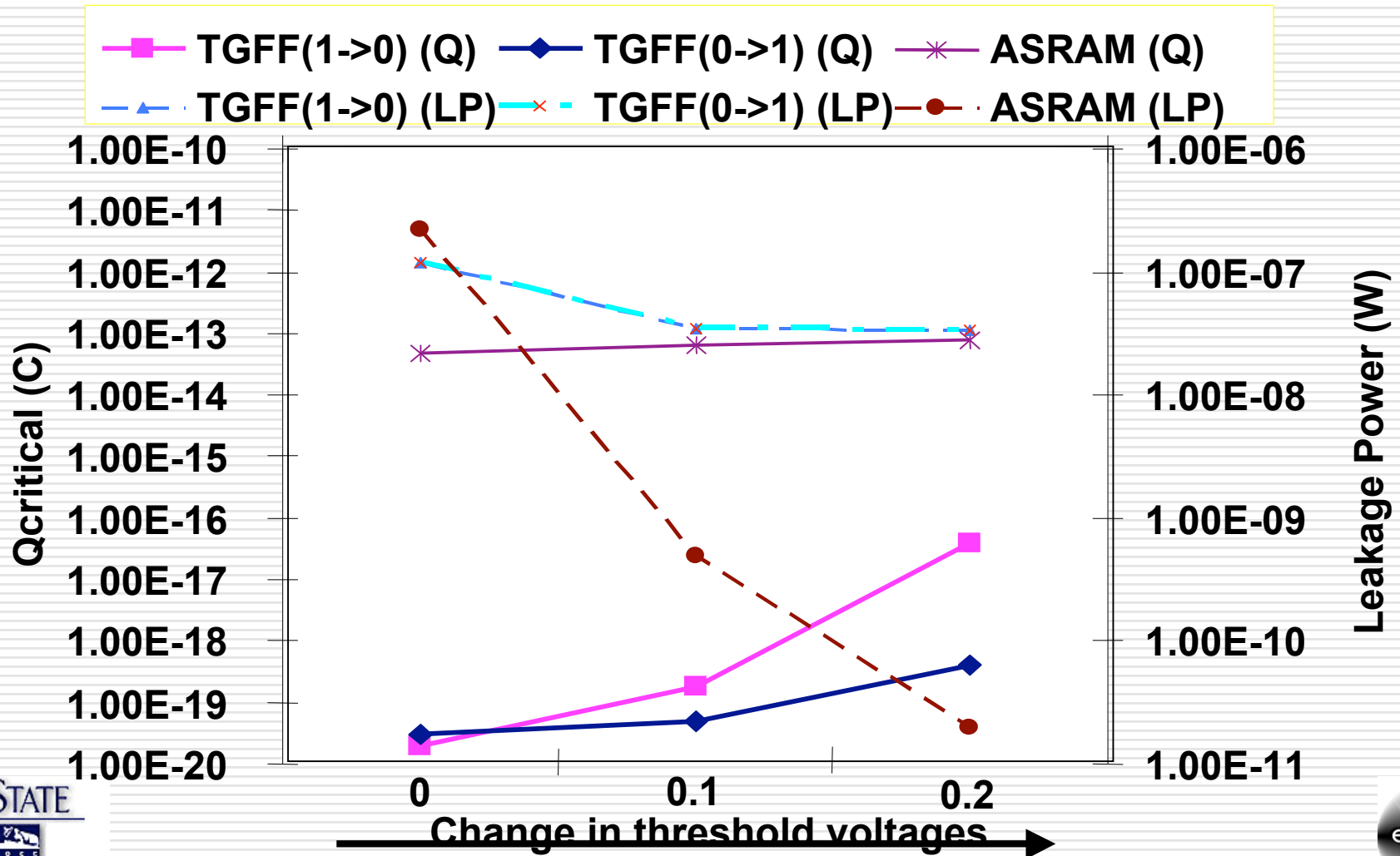
Results- $Q_{critical}$

	$-V_{th}$	$Q_{critical}/C$		$-V_{th}$	$Q_{critical}/C$
TGFF(1 → 0)	0	1.99E-20	ASRAM	0	4.75E-14
	0.1	1.77E-19		0.1	6.58E-14
	0.2	3.87E-17		0.2	7.58E-14
TGFF(0 → 1)	0	3.04E-20	Inverters	0	1.28E-20
	0.1	5.03E-20		0.1	2.3E-20
	0.2	4.18E-19		0.2	4.73E-20
Adder-1Bit(1 → 0)	0	4.60E-20	Nand	0	2.23E-18
	0.1	1.35E-19		0.1	2.23E-18
	0.2	5.87E-17		0.2	5.24E-18
Adder-1Bit(0 → 1)	0	3.67E-17	SRAM	0	4.75E-14
	0.1	4.29E-17		0.1	4.04E-14
	0.2	7.13E-17		0.2	3.82E-14

Results- Leakage Power

	$-V_{th}$	Leakage Power in W		$-V_{th}$	Leakage Power in W
TGFF(1->0)	0	1.18E-07	SRAM	0	2.20E-07
	0.1	3.42E-08		0.1	9.10E-09
	0.2	3.40E-08		0.2	3.42E-10
TGFF(0->1)	0	1.20E-07	ASRAM	0	2.20E-07
	0.1	3.42E-08		0.1	4.90E-10
	0.2	3.40E-08		0.2	1.99E-11
Adder-1Bit(1->0)	0	3.61E-05	Inverters	0	2.56E-07
	0.1	3.49E-05		0.1	9.92E-09
	0.2	3.46E-05		0.2	4.90E-10
Adder-1Bit(0->1)	0	3.61E-05	Nand	0	2.40E-07
	0.1	3.49E-05		0.1	9.66E-09
	0.2	4.59E-06		0.2	9.46E-10

Results at a glance



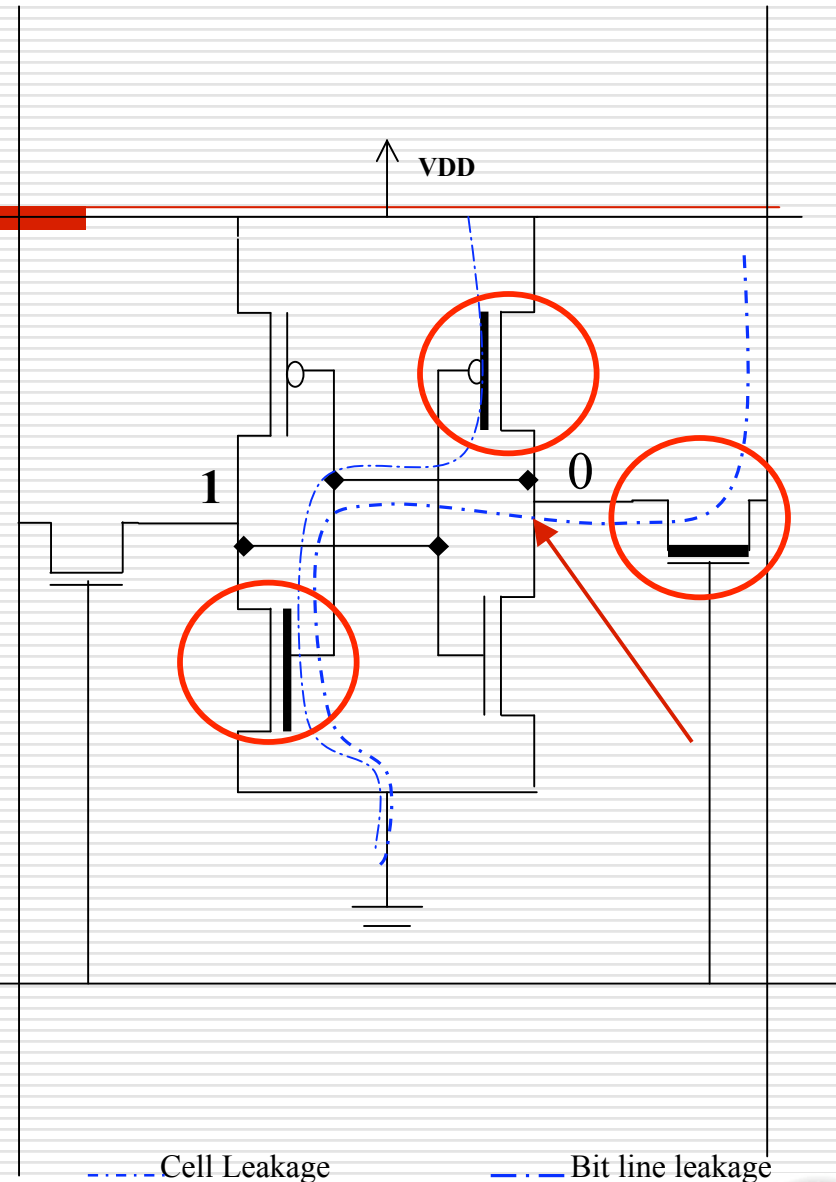
SRAMs

- Qcritical of 6-t SRAM changes a little
 - Because of the regenerative nature the back to back inverters
- ASRAM, the Qcritical increases for the preferred state
 - Due the difference in the driving strength of the PMOS or NMOS

Asymmetric SRAM

(Optimized for Leakage of "0")

- ❑ The lower current drive of the high threshold voltage transistors make this design vulnerable to a stored value of 1 (its non favorable state for leakage reduction).
- ❑ Similarly for the cell optimized for 1.



Flip Flops

- Flip flops evaluated for
 - Most susceptible node
 - Ability to latch the transient pulse
- Two factors
 - gain of the inverter- should decrease $Q_{critical}$
 - Transmission gate present at the slave - should increase $Q_{critical}$

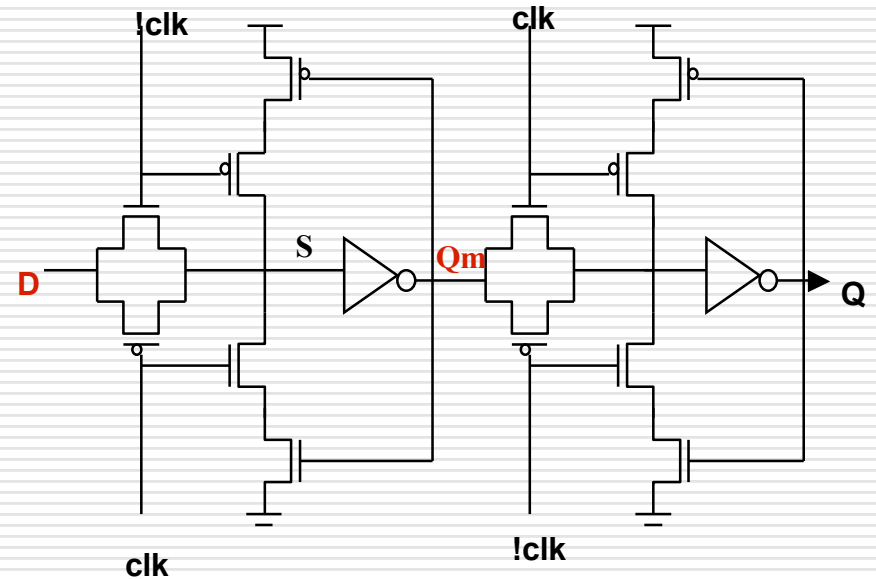
Flip Flops

	$_V_{th}$	$Q_{critical}$ at input/C	$Q_{critical}$ at most susceptible node/C
SDFF	0	6.06E-21	1.24E-20
	0.1	5.08E-21	1.33E-20
	0.2	-	-
C ² MOSFF	0	3.69E-20	7.12E-21
	0.1	5.64E-20	7.17E-21
	0.2	1.68E-19	
TGFF	0	1.99E-20	7.36E-21
	0.1	1.77E-19	7.36E-21
	0.2	3.87E-17	7.36E-21

Flip Flops

□ TGFF

- Both factors cancel out, hence $Q_{critical}$ almost same at most susceptible node
- At the input **D**, the presence of the transmission gate results in a large increase in $Q_{critical}$

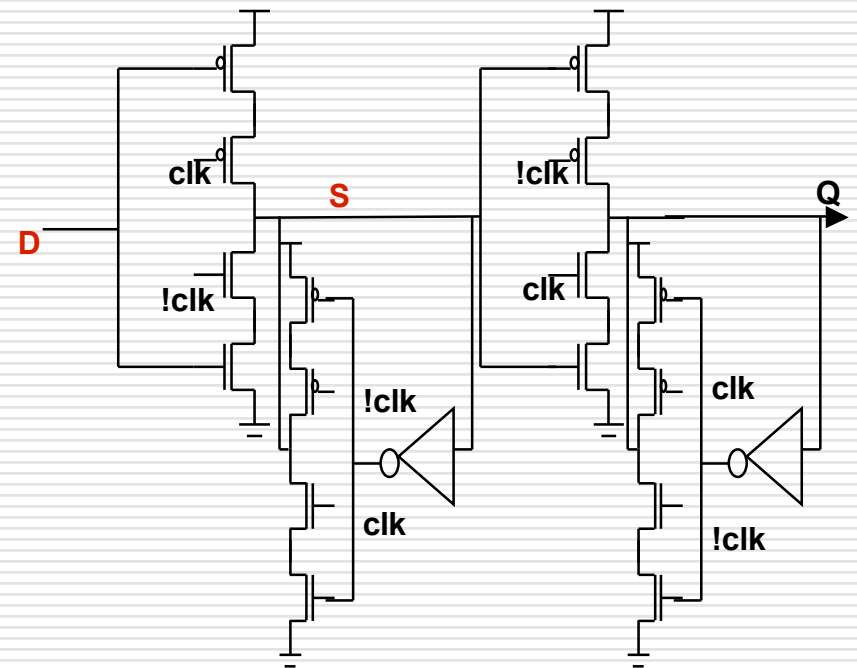


TGFF

Flip Flops

□ C²MOS

- no inverter in the path to the output
- Q_{critical} increases for both the nodes **S** and **D**

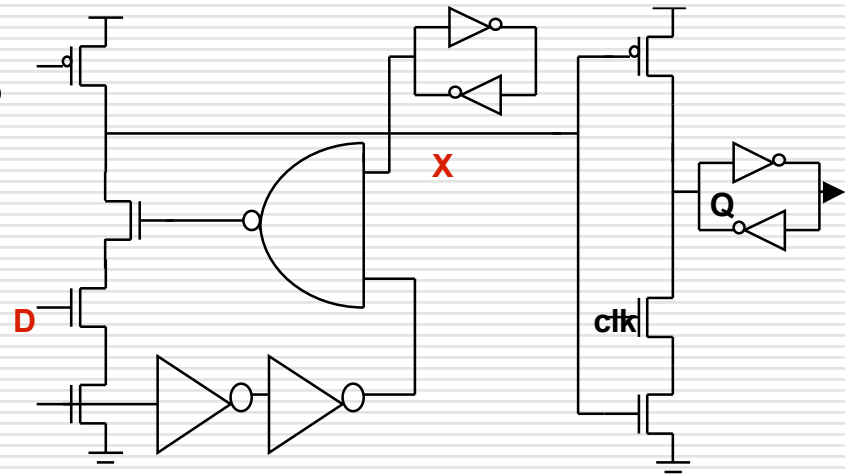


B. C²MOS-FF

Flip Flops

□ SDFF

- few sized devices resulting in a much higher $Q_{critical}$ for node X
- With high V_t , at input the greater overlap time is actually going to help pull down the value X more and hence reduces the $Q_{critical}$



B. SDFF

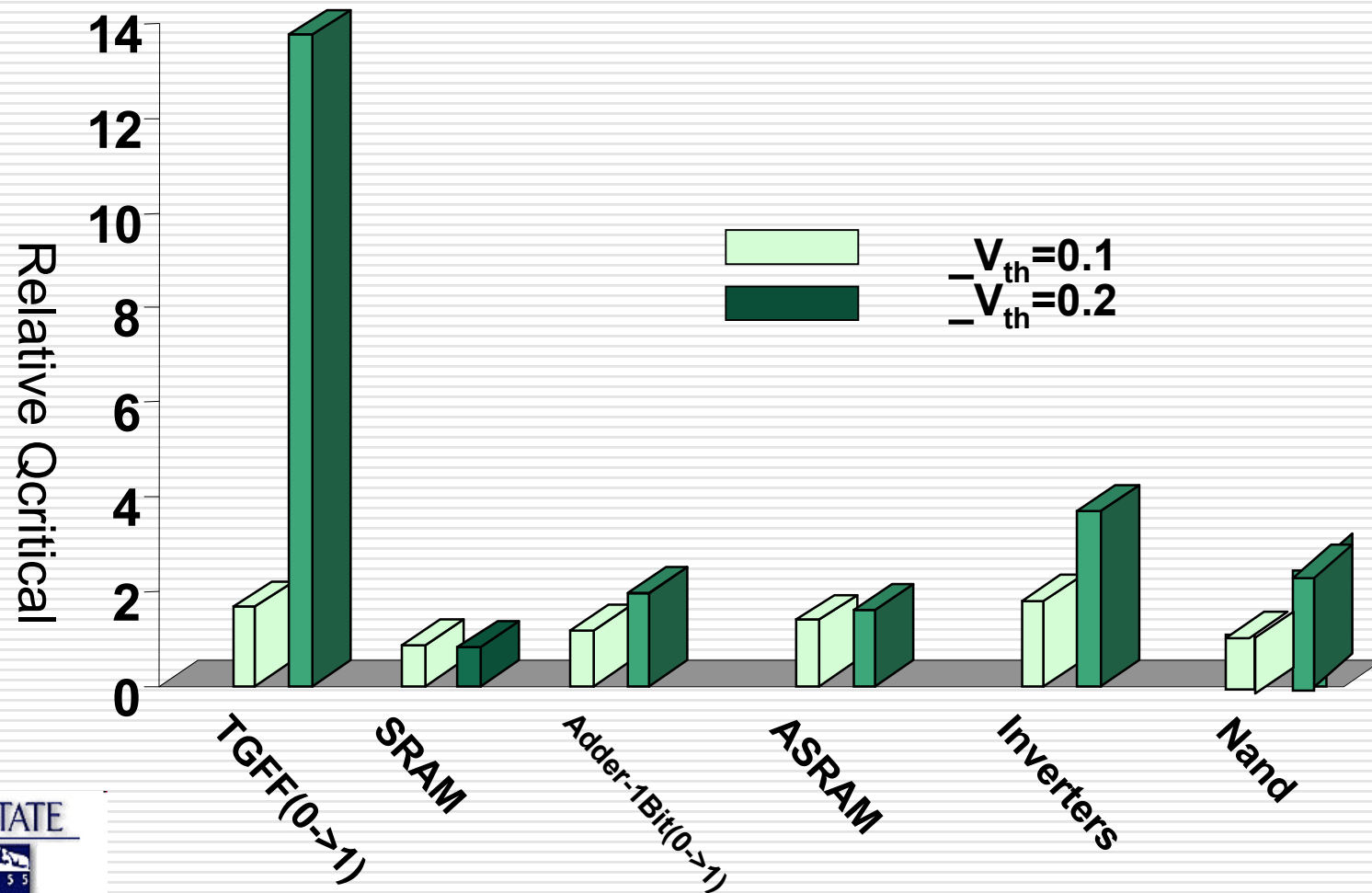
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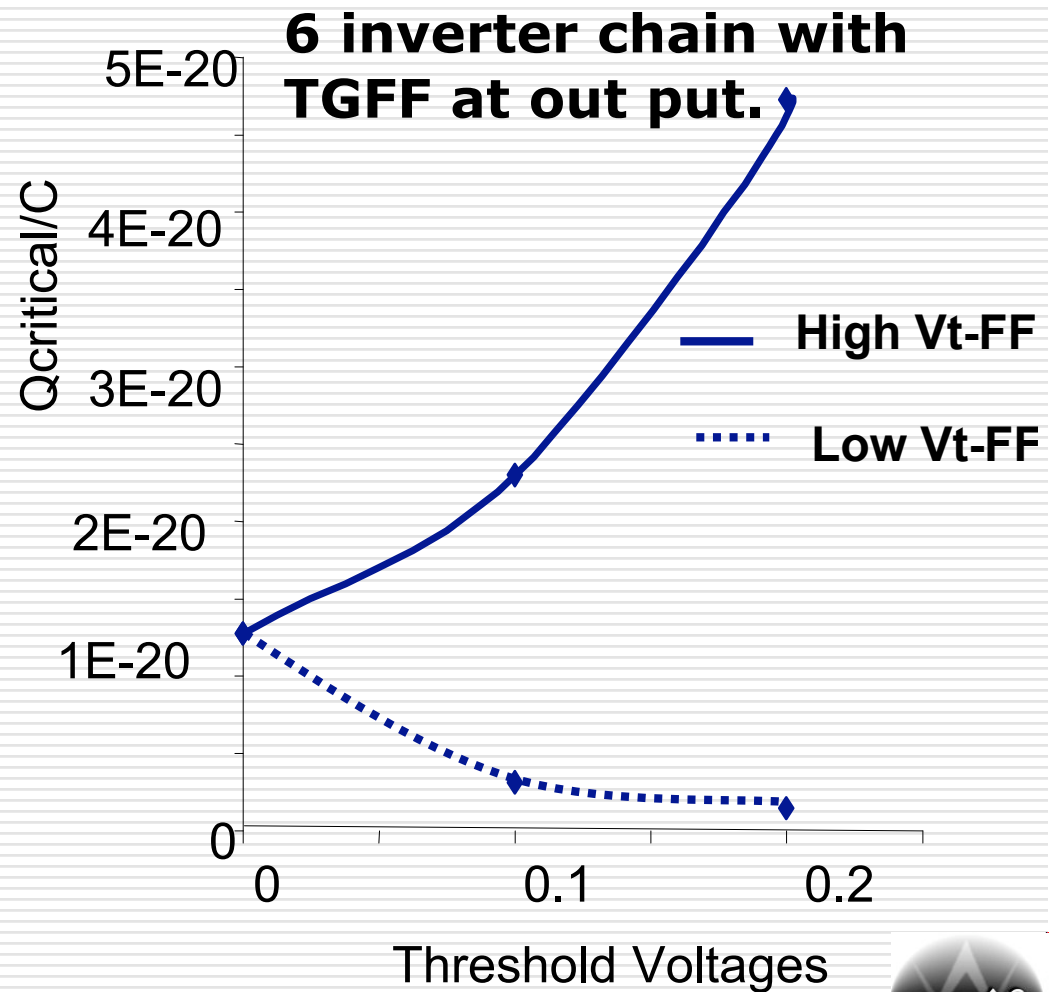
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Results- $Q_{critical}$



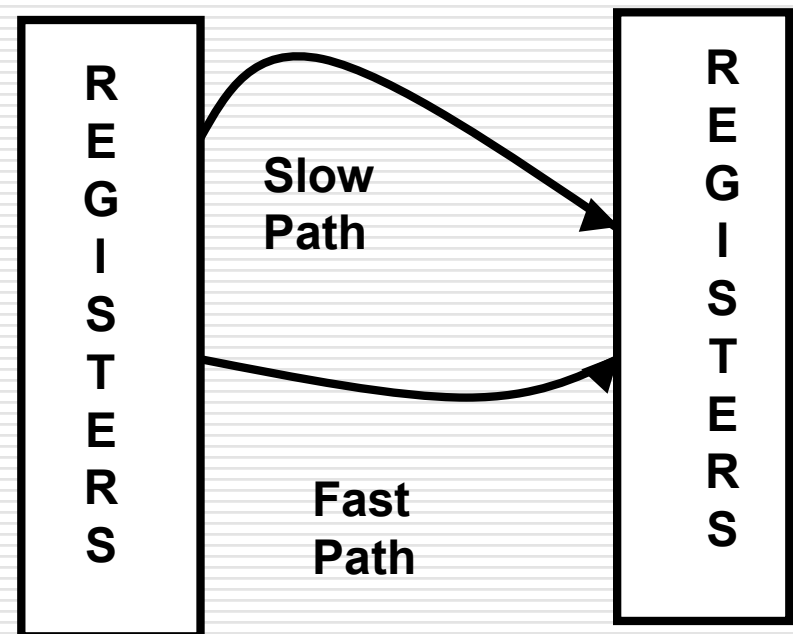
Logic Chains

- Q_{critical} depends on the output flips flop
 - High V_{+FF} , Q_{critical} increases
 - Low V_{+FF} , Q_{critical} decreases



Delay Balancing

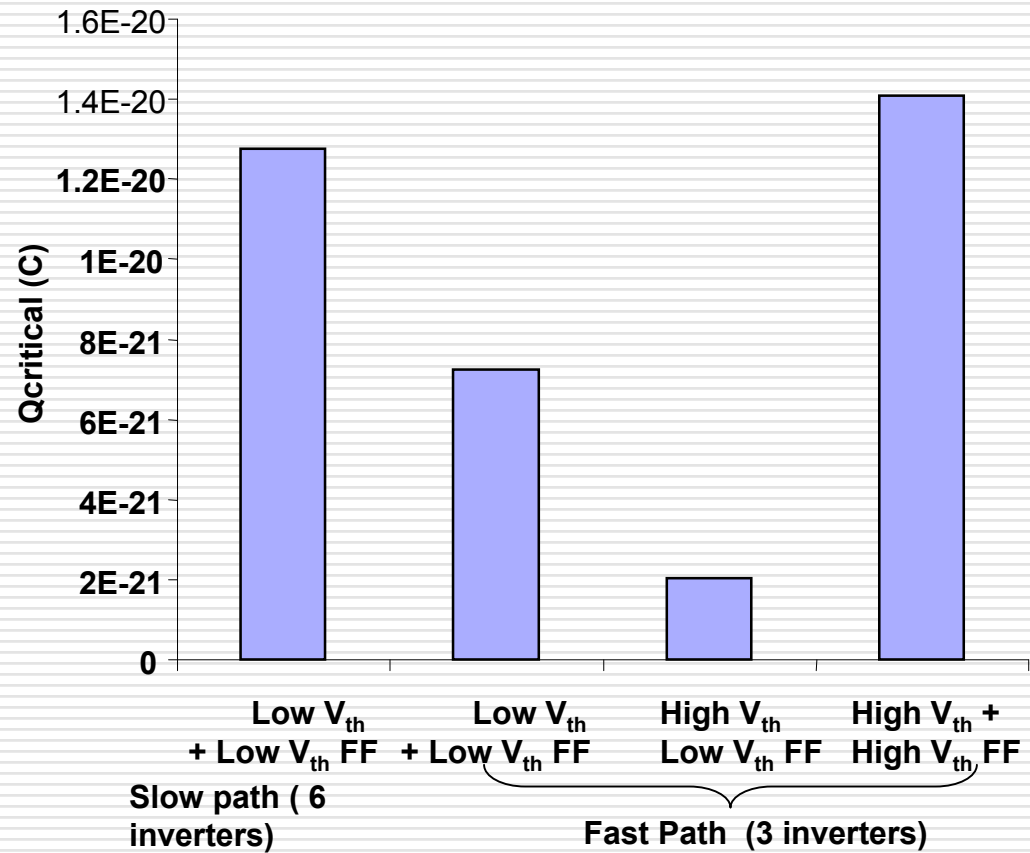
- Practice to use high V_+ on fast path to do delay balance
- Effects the hazard bubble
- Use 6/3 invert chains for slow/fast logic



Delay Balancing

□ Qcritical of fast paths reduces

□ Use High V_{th} flip flops



Conclusion

- ❑ Certain designs (like TGFF) have higher Q_{critical} for high V_{t} , others (like static logic chains) have lower Q_{critical} .
- ❑ ASRAM has lower leakage and higher Q_{critical}
- ❑ Delay balancing can potentially increase SER, can use high- V_{t} TGFF to buy back the Q_{critical} .
- ❑ Analysis of leakage reduction strategies on SER is critical