On-chip Bus Thermal Analysis and Optimization

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Outline

- Motivation
- Bus Energy & Thermal model
- Thermal impact of system bus with technology scaling
- Theoretical analysis of bus thermal optimization
- Thermal spreading encoding method
- Experimental results
- Conclusions

Motivation

- On-chip bus power consumption: an important part of the overall system power consumption
- The interconnect temperature can be as high as 90˚C [Shang]
- High temperature has a negative impact on interconnect performance and reliability
- The on-chip bus has not gained enough attention

Energy Model

- Heat generated on the interconnects regardless the current direction
- The energy drawn from power [Sotiadis]
  - Energy stored in the capacitance
  - Energy dissipated as heat (E_{heat0})
- Energy generated when bus line discharged
  - Energy stored in the capacitance
  - Energy dissipated as heat (E_{heat1})

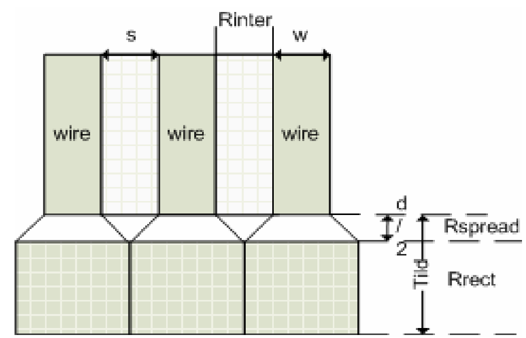
Energy Model

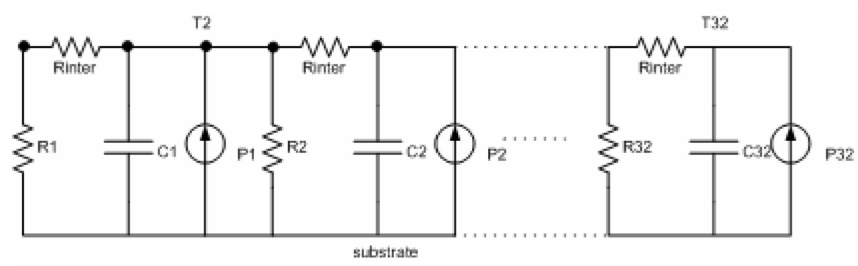
- Heat dissipated in the interconnects and drivers or receivers (Eheat0+Eheat1)
- Optimal length of the wire segment (S_{opt})
- Optimal size of the gate (L_{opt})
- Heat dissipated in the interconnects

$$\frac{l_{opt} r (E_{heat1} + E_{heat0})}{(l_{opt} r + \frac{r_0}{s_{opt}})T}$$

Chiang's Thermal Model

- Assumptions:
- Heat dissipated through the underlying layer
- Ignore thermal conductivity variation along the length
- Via effects diminished beyond critical length





Chiang's Thermal Model

- For edge wires

$$P_1 = C_1 \times \frac{\partial T_1}{\partial t} + \frac{T_1 - T_0}{R_1} + \frac{T_1 - T_2}{R_{inter}}$$

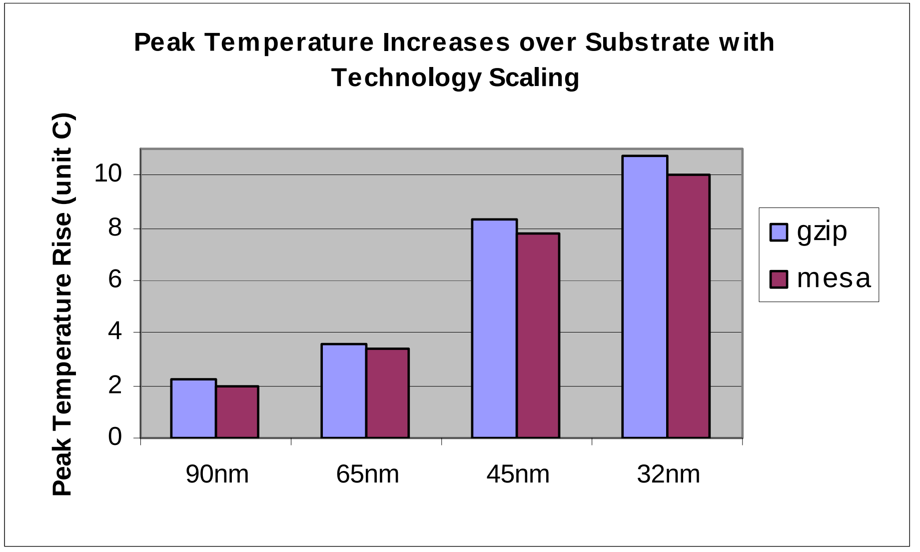
$$P_{32} = C_{32} \times \frac{\partial T_{32}}{\partial t} + \frac{T_{32} - T_0}{R_{32}} + \frac{T_{32} - T_{31}}{R_{inter}}$$

- For the wires in the middle

$$P_i = C_i \times \frac{\partial T_i}{\partial t} + \frac{T_i - T_0}{R_i} + \frac{(2T_i - T_{i-1} - T_{i+1})}{R_{inter}}$$

Technology Scaling

- Not worst case analysis
- Technology Parameters [ITRS 2004 edition]
- Thermal conductivity of low k materials, clock, interconnect pitch, Number of interconnects layer



Theoretical analysis

- ***Problem formulation:***
  - Given that the total power consumption across the system bus *P(t)*
  - Find an optimal distribution of the power consumption among the bus wires
- Optimal power consumption distribution:

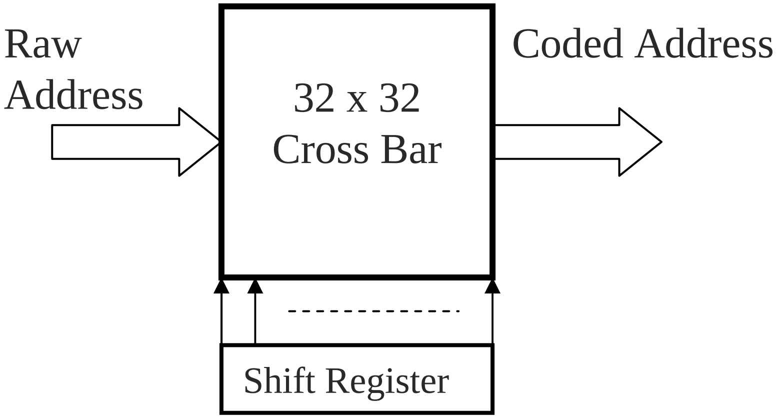
$$P_i = \frac{P_{total}}{Buswidth}$$

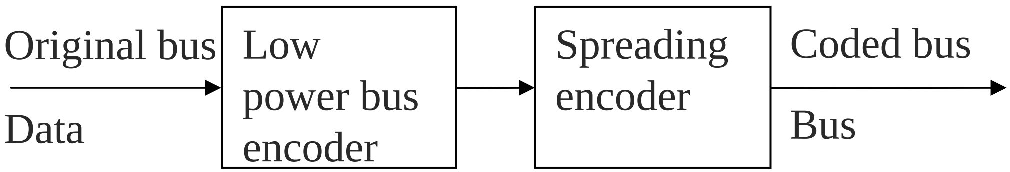
Thermal Spreading Encoding

- Distribute the switching activities among the bus line evenly
- Rotating the bus line position at a certain period
- More effective combined with the simple low power coding scheme

Spreading coding

- Advantages:
  - Low area overhead
  - Low power overhead
  - Low complexity

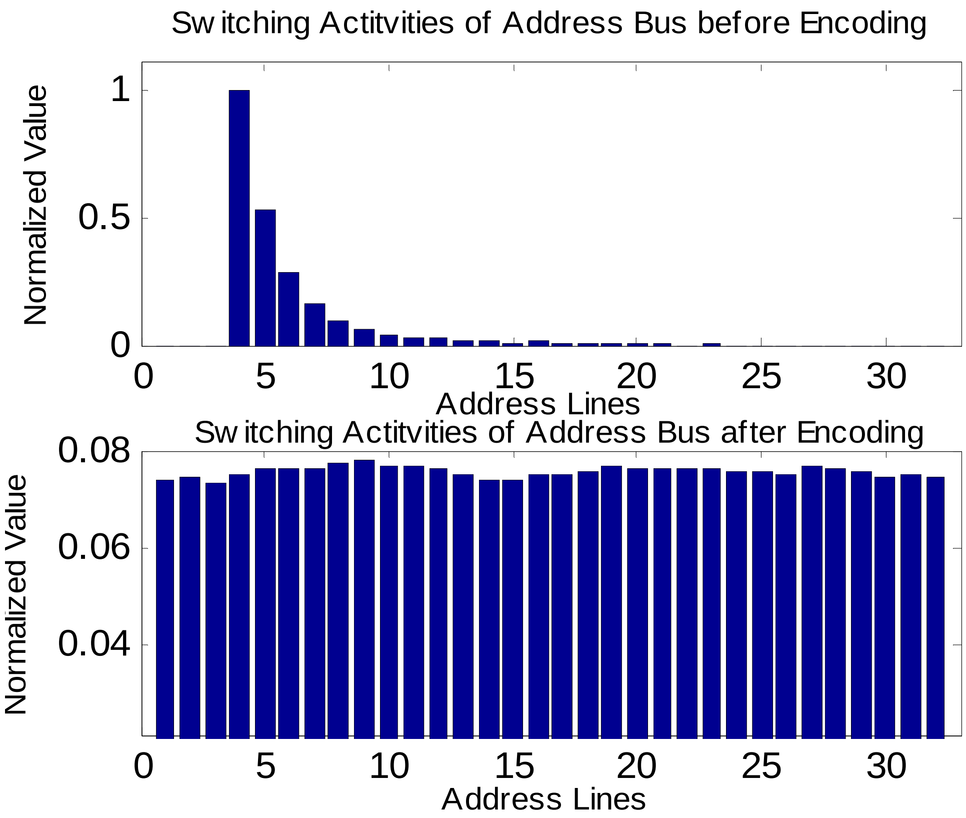




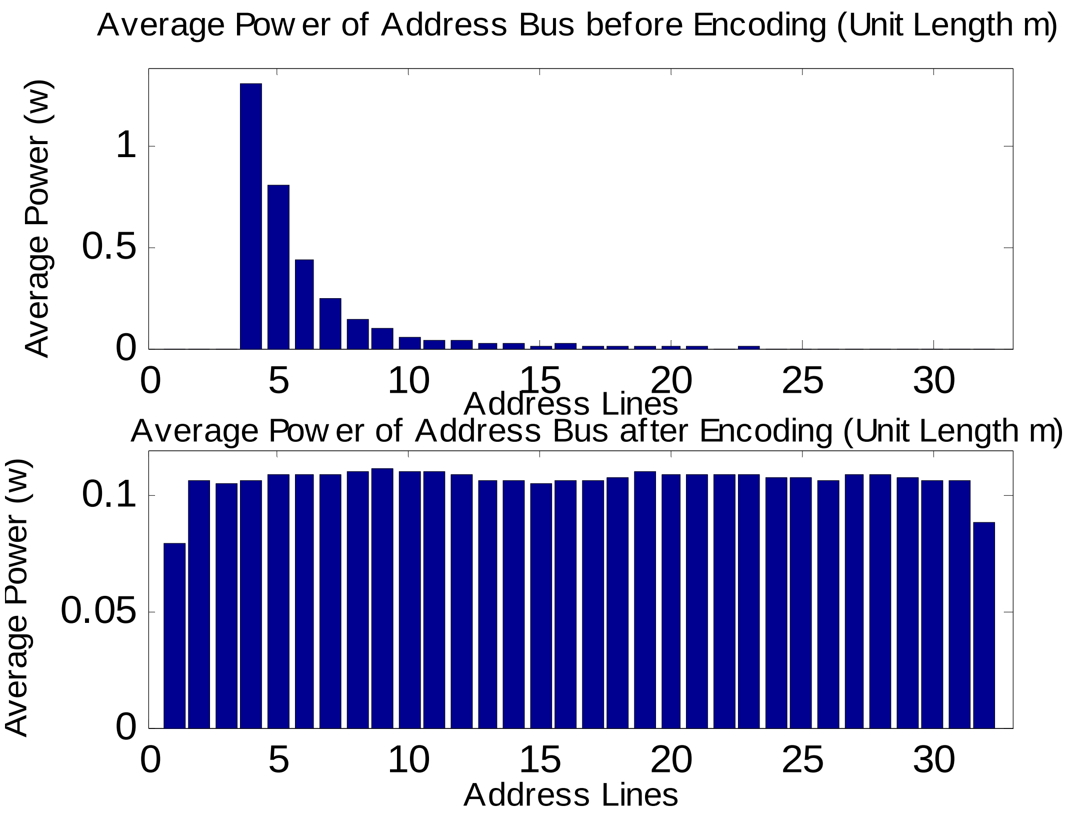
Experiment results

- Instruction Address Bus:
  - large power consumption
  - Regular switching patterns
- Switching activities distribution
- Power distribution
- Temperature reduction

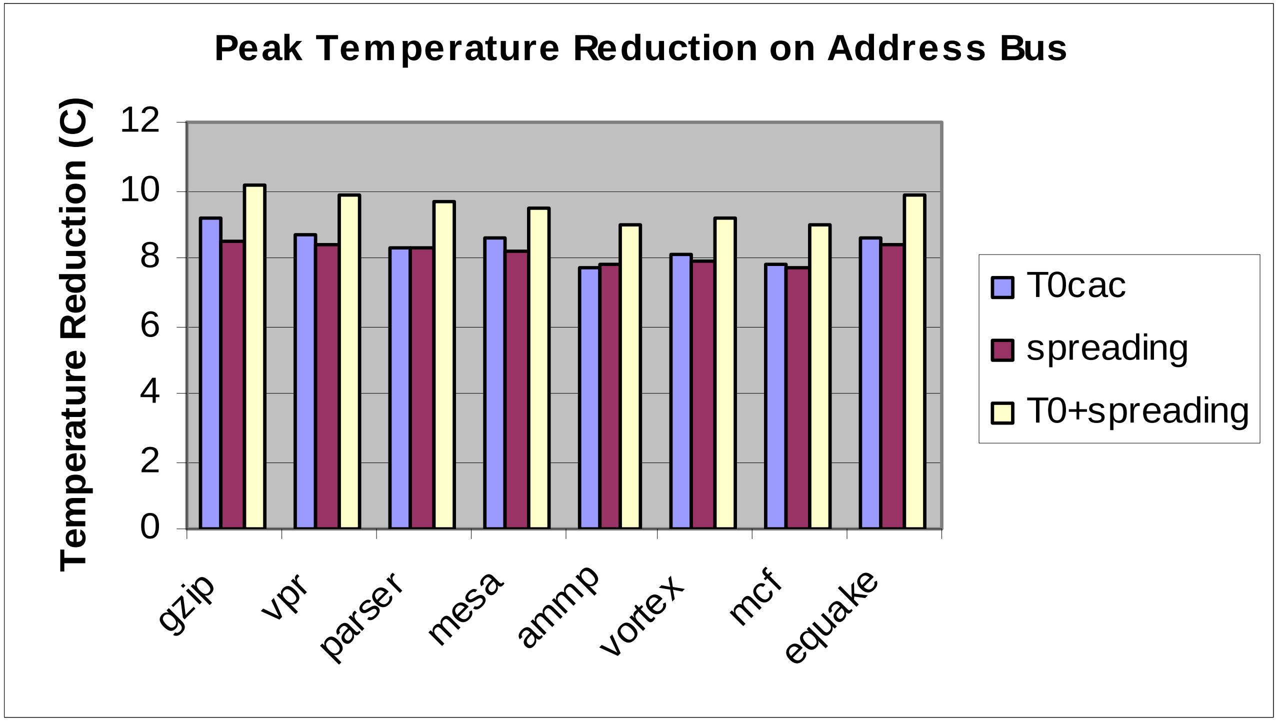
Instruction Address Bus



Instruction Address Bus



Instruction Address Bus



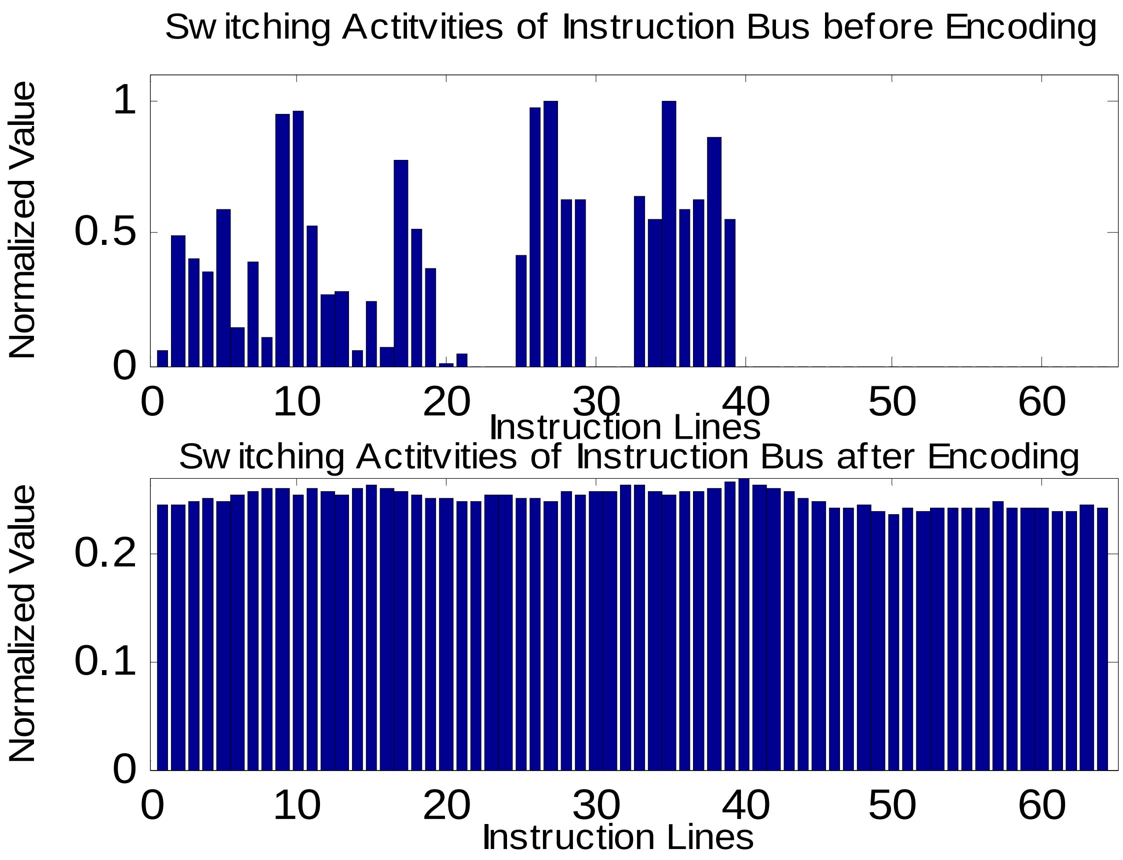
Instruction Address Bus

- Compared to T0CAC-- a very effective low power encoding
- Spreading + *T0* coding better than T0CAC
  - Simple
  - Lower power overhead
  - More effective in temperature reduction

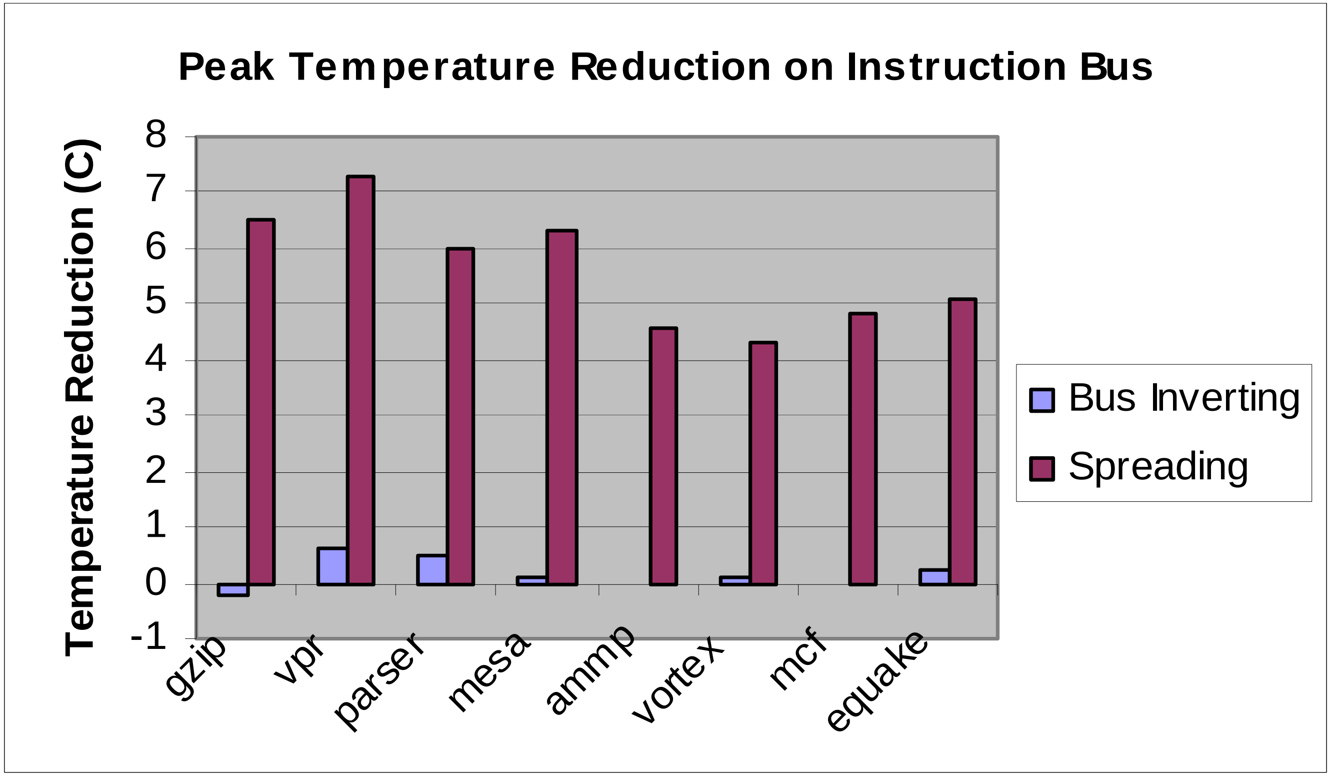
Instruction Bus

- Instruction data bus
  - Large power consumption
  - Irregular switching patterns
- T0CAC can not be used
- Much better than Bus Inverting

Instruction Bus



Instruction Bus



Conclusion

- Characterize the thermal impact on on-chip bus
- Improved bus energy and thermal models
- Optimal power distribution for temperature reduction
- Spreading+T0 encoding better than T0CAC
- Effective for both instruction address and instruction bus