Curriculum Vitae

MARY JANE IRWIN
Evan Pugh Professor
A. Robert Noll Chair in Engineering

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Education

1977	Ph.D. Computer Science, University of Illinois at Urbana-Champaign (UIUC)
1975	M.S. Computer Science, UIUC
1971	B.S. Mathematics, Memphis State University (magna cum laude)

Employment

7/06-	Evan Pugh Professor, Computer Science and Engineering, PSU
7/03-	A. Robert Noll Chair in Engineering, Computer Science and Engineering, PSU
1/99-7/03	Distinguished Professor, Computer Science and Engineering, PSU
7/89-1/99	Professor, Computer Science and Engineering, PSU
7/91-6/93	Department Head, Computer Science, PSU
1/86-7/86	Research Staff, Supercomputing Research Center, Institute for Defense Analysis, Bowie, MD
8/77-7/89	Associate Professor, Assistant Professor, Computer Science, PSU
1/72-8/77	Graduate Research and Graduate Teaching Assistant, Computer Science, UIUC

Research Interests

Computer architecture (resource constrained, application specific, chip multiprocessors) and computer arithmetic; Energy aware systems design; Reliable systems design; VLSI systems design and emerging technologies

Awards and Honors

Outstanding Teacher Award, PSU Computer Science Club (1981); ACM/SIGDA Leadership Award (1993); IEEE Fellow (1994); PSU/PSES Outstanding Research Award (1995); ACM Fellow (1996); CIC Academic Leadership Program Fellow (1996-97); Honorary Doctorate, Chalmers University, Sweden (1997); PSU/PSES Premier Research Award (2001); Elected to the National Academy of Engineering (2003); IEEE/CAS VLSI Transactions Best Paper of the Year Award (2003); DAC Marie R. Pistilli Women in EDA Award (2004); ACM/SIGDA Distinguished Service Award (2005 and 2007); ACM Distinguished Service Award (2005); CRA Distinguished Service Award (2006); PSU Howard B. Palmer Faculty Mentoring Award (2006); IEEE ICPADS Best Paper Award (2006); Anita Borg Technical Leadership Award (2007); IPDPS Best Paper Award (2008); Elected to the American Academy of Arts and Sciences (2009); ACM Athena Lecturer Award (2010)

Selected Keynote/Feature/Plenary Talks and Distinguished Lectures

SiPS'99 Feature Talk, Taipei, TAIWAN, 1999; KAIST Distinguished Lecturer, Korea, 2000; PATMOS Feature Talk, Göttingen, Germany, 2000; Dortmund Summer School Lecturer, Dortmund, GERMANY, 2000; COLP'00 Workshop Keynote, Philadelphia, PA, 2000; NSF/CISE Molecular Architectures Workshop Invited Talk, Notre Dame, 2001; Eli Lilly Distinguished Lecturer, Univ. of Pittsburgh, 2002; ISVLSI Invited Talk, Tampa, FL, 2003; IBM ACEED'03 Invited Talk, Austin, TX, 2003; MPSoC Summer School Lecturer, Chamonix, France, 2003 and Provence, France, 2004; Smith Distinguished Lecturer, UCIrvine, 2005; Distinguished Lecturer, Univ. of Virginia, 2005; Distinguished Lecturer, University of Minnesota, 2007; CCSCNE-07 Conference Plenary, Rochester, NY, 2007; CRA-W Distinguished Lecturer, University of South Florida, 2007; Distinguished

Lecturer, Georgia Institute of Technology, 2008; HiPEAC Workshop on Design for Reliability Keynote, Cyprus, 2009; ISCA 2010 Plenary, St. Malo, France, 2010

Selected Association/Society Memberships and Professional Activities

Memberships: Association for Computing Machinery (ACM), SIGARCH, SIGDA, SIGBED; Institute for Electrical and Electronics Engineers (IEEE) Computer Society, IEEE SP Society, IEEE CAS Society, IEEE SSC Society; International Federation for Information Processing (IFIP) Sections 10.2 and 10.3

5/85-	Program Committee Member and Publicity Chair, 7th Symp. on Computer Arithmetic (ARITH7), 1985; Program Chair, ARITH8, 1987; Program Committee Member, ARITH9, 1989 and ARITH10, 1991; Program Co-Chair, ARITH11, 1993; Program Committee Member, ARITH12, 1995 and ARITH13, 1997; Steering Committee Member, ARITH14 - present
7/85-6/91	Secretary/Treasurer (elected), ACM SIGARCH
11/86-12/91	Advisory Committee Member, MIPS Division, CISE Directorate, NSF
1/88-12/01	Editorial Board Member, *Journal of VLSI Signal Processin*g, Kluwer Academic Publisher
1/89-12/91	Subject Area Editor, *Journal of Parallel and Distributed Computin*g, Academic Press
1/89-12/91	Member, Eckert Mauchley Award Committee (Chair in 1991), ACM and IEEE Computer Society
2/89-8/04	Member, Board of Directors, ACM/SIGDA
7/90-7/01	Member, Design Automation Conference (DAC) Executive Committee; Pub. Chair, DAC'91; Tutorials Chair, DAC'92; ACM Rep., DAC'93, DAC'94 and DAC'95; Finance Chair, DAC'96 and DAC'97; Vice Chair, DAC'98; General Chair, DAC'99; Past Chair, DAC'00; Tutorials Chair, DAC'01
5/91- 4/93	Program Chair, ACM/SIGDA Physical Design Workshop (PDW), PDW'91; Proc. Chair, PDW'93
1/91-6/95	Member, Editorial Board, *IEEE Transactions on Computers*
7/91-6/03	Member (elected), Computer Research Association (CRA) Board of Directors, Vice Chair in 7/95-6/97
1/92-12/95	Member, Publication Board (Pubs/Press Planning Committee Chair in 92-93), IEEE Computer Society
1/93-12/95	Member (elected), IEEE Computer Society Board of Governors
7/93-6/03	Member (elected), Board of Directors, ACM/SIGARCH
7/94-6/97	Member (elected), ACM Council
6/96	General Chair, Federated Research Computing Conference (FCRC), Philadelphia, PA
7/96-6/98	Vice President (elected), ACM
8/97-	Finance Chair and Program Committee Member, Inter. Symp. on Low Power Electronics and Design (ISLPED), ISLPED'97, ISLPED'98, ISLPED'99, and ISLPED'00; Technical Program Co-Chair, ISLPED'01; General Co-Chair, ISLPED'02; Steering Committee Member, ISLPED'03 - present
12/97	US Program Chair, Inter. Conf. on High Performance Computing (HiPC), Bangalore, India
1/98-12/09	Member, ACM/SIGARCH Wilkes Award Committee (1/98-12/00 & 1/07-12/09), Chair in 2000 & 2008
1/98-6/03	Member, NSF CISE Directorate Advisory Committee, Chair in 1/02-6/03
7/98	General Co-Chair, The CRA Conference at Snowbird, Snowbird, UT
10/98-8/04	Editor-in-Chief, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*
4/00	General Co-Chair, IEEE VLSI Workshop, Orlando, FL
5/00-8/04	Member, Army Research Lab Technical Advisory Board (ARLTAB), Chair of ARL/DCS Panel
12/00	Co-Chair, MICRO-33 Kool Chips Workshop, Monterey, CA
11/01-10/04	Program Committee Member, Compilers, Architectures and Synthesis for Embedded Systems (CASES) Conference, CASES'01 and CASES'02; General Co-Chair, CASES'04
5/02-6/08	Member, ACM Publications Board (Co-Chair, 1/05-6/07)
10/02-	Program Committee Member, Languages, Compiler and Tools for Embedded Systems (LCTES) Conference, LCTES'03 and LCTES'04; General Chair, LCTES'06; Steering Committee Member, LCTES'07 - present
3/03-12/05	Member, NRC Committee on the Future of Supercomputing
1/04-12/06	Member, NAE Section 5 Peer Committee, Chair in 2006
1/07-12/08	NAE Section 5 Search Executive
3/04-12/06	Co Editor-in-Chief, *ACM Journal on Emerging Technology in Computing Systems (JETC)*
1/05-	Member, IDA/Center for Computer Science (CCS) Program Review Committee
6/06-7/09	Member, NAE Russ Prize Committee, Chair in 2008, Past Chair in 2010
1/07-	Member, Board on Army Science and Technology (BAST)
7/06-	Member, Microsoft Research (MSR) External Research Advisory Board
9/08-8/13	Member, ACM Fellow Selection Committee

2/09-1/12 Member, NAE Committee on Membership (CoM), Vice Chair Class of 2011, Chair Class of 2012
3/09 Program Chair, Inter. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS)

Recent Program Committee Memberships: Conference on Computer Architectures for Machine Perception (CAMP), CAMP'97 and CAMP'00; Signal and Image Processing Systems (SIPS) Symposium, SIPS'01 through SIPS'05; Inter. Symposium on High Performance Computer Architecture (HPCA), HPCA'05; Inter. Parallel and Distributed Processing Symposium (IPDPS), IPDPS'06 and IPDPS'11; ACM/IEEE Microarchitecture Conference (MICRO), MICRO'06, MICRO'09, MICRO'10; ACM/IEEE Inter. Symposium on Computer Architecture (ISCA), ISCA'08; Inter. Conf. on High Performance Embedded Architectures and Compilers (HIPEAC), HIPEAC'09 and HIPEAC'10; Inter. Conf. on Parallel Architectures and Compilation Techniques (PACT), PACT'10

Recent External Department Review Committees: Electrical and Computer Engr, Purdue (2006), Computer Science, Syracuse (2008), Electrical and Computer Engr., UIUC (2008), Computer Science, Yale (2010)

Selected Educational Activities

Conference and University Tutorials: Low Power Design for SoCs at ASIC, Washington, DC, 9/99 (half-day, sole presenter); Low Power Design: From Soup to Nuts at ISCA'00, Vancouver, BC, 06/00 (full-day, two presenters); Low Power Design Methodologies: Hardware and Software Issues at PACT'00, Philadelphia, PA, 10/00 (full-day, two presenters); Power-Efficient Design at ISCA'01, Goteborg, Sweden, 7/01 (full-day, four presenters); Low Power Design: From Circuits to Software, Tianan, Taiwan, 10/02 (half-day, sole presenter)

PSU Undergraduate Courses: Computer Programming for Engineers (201); Introduction to Digital Systems (271); Computer Organization and Design (331); Introduction to Systems Programming; Computer Systems Architecture (431); Operating Systems; VLSI Digital Circuits (477, now 411)

PSU Graduate Courses: Fundamentals of Computer Architectures (530); Architecture of Arithmetic Processors (575); VLSI Systems Design (577); Special Topics (598): Embedded Systems, Low Power Design, Emerging Computing Technologies, Reliable Low Power Systems Design

Most recent seven years of Student Rating of Teaching Effectiveness (SRTEs)

Course/Num. Section	Enroll-ment	Elective %	Semester/ Year	Number of Respondents (%)	Overall Quality Of Course (out of 7.00)	Overall Quality Of Instruction (out of 7.00)
CSE 477.1	37	48%	Fa03	27 (73%)	5.92	6.38
CSE 598C.1*	19	38%	Fa03	16 (84%)	5.93	6.13
			Sp04**			
CSE 431.1	27	11%	Fa04	19 (70%)	5.00	5.63
CSE 431.2	70	2%	Fa04	53 (76%)	4.94	5.32
CSE 575.1	12	42%	Sp05	12 (100%)	5.83	6.50
CSE 431.1	18	31%	Fa05	16 (89%)	5.75	6.06
CSE 431.2	40	0%	Fa05	27 (68%)	4.96	5.59
			Sp06***			
CSE 331.1****	39	13%	Fa06	23 (59%)	5.43	5.70
			Sp07***			
CSE 331.1****	37	8%	Fa07	24(65%)	4.92	5.17
			Sp08***			
CMPEN 431.1	57	24%	Fa08	37 (65%)	5.32	5.73
CSE 575.1	15	60%	Fa08	10 (67%)	6.20	6.60
			Sp09***			
CSE 331.1****	53	38%	Fa09	24 (45%)	5.63	5.71
			Sp10***			

The normal teaching load for "research active" faculty in CSE is three courses a year.
* With Narayanan and Kandemir ** On sabbatical Leave *** Course Buy Out
**** Section 331.2 taught by Graduate Teaching Intern under my direct supervision

Graduated more than twenty Ph.D. students and eighty M.S. students during the period 1978 to 2009 (see *Research Contributions* section for detailed listing of Ph.D. students)

Selected Outreach Activities

6/91-	Member, Steering Committee of the Computing Research Association's Committee on the Status of Women in Computing Research (CRA-W), Co-Chair in 6/93-7/96, CRA-W Awards Chair, 1996-2009, CAPP Project Co-Chair, 2004-2008, Grad Cohort Co-Chair, 2005-2008, frequent presenter at CRA-W Career Mentoring Workshops, CRA-W Grad Cohort, and CRA-W CAPP
7/94-6/96	Chair, PSU Women in Science and Engineering (WISE) Network Executive Committee (Interim Director in 1/95-8/95)
7/96-6/01	Member, PSU Commission For Women (CFW); Member, CFW Executive Committee, Chair of the Faculty/Student Issues and Policies Committee, 7/97-6/98; Chair Elect, CFW, Member, CFW Executive Committee, Member, Faculty Issues and Policies Committee, Chair, CFW Banquet Committee, 7/98-6/99; Chair, 7/99-6/00; Past Chair, 7/00-6/01
7/97-	Ex-Officio Member, Women in Engineering Program Advisory Committee
1/05-	Member, College of Engineering, Women in Engineering Leadership Team
10/09	Panelist, Speaker, AAAS PAESMEM Workshop for Women: Building Science, Engineering, and Technology Leaders, Washington, D.C.

Funding:

5/89-590	ACM/SIGDA, DAC Graduate Academic Scholarships; $22,000
7/94-6/97	NSF/CDA, 9416785, CRA Committee on the Status of Women in CSE (with F. Berman, UCSD); $132,433
7/95-12/95	Sloan, Assessing Retention Data, Perceptions, Climate, and Mentoring for Women in Science and Engineering at Penn State (with L. Schiebinger); $29,899
1/05-1/09	Microsoft and Google, CRA-W Grad Cohort Program (with M.L. Soffa, UVA); $125,000 Microsoft and $125,000 Google per year (2005, 2006, 2007, and 2008)
1/06-12/09	NSF/ADVANCE Leadership, 0545229, CRA-W CAPP-R and CAPP-E Program (with M.L. Soffa, UVA); $268,602

Selected Other Penn State University Academic and Administrative Activities

9/79-8/80	Member, Provost's Committee for Administrative Review of the Office of the Dean, College of Science
9/79-6/82	Member, Computer Science Headship Search Committee
9/79-5/83	Chair, Computer Science Computing Facilities Committee
9/80-6/91	Advisor, Univ. Scholars Program
9/83-8/84	Graduate Officer, Computer Science
9/83-9/89	Member, Univ. Faculty Advisory Committee on Academic Computing
9/83-7/91	Member, Computer Science Promotion and Tenure Committee (9/83-7/85 and 8/88-7/91)
1/87-6/89	Member, College of Science Dean's Search Committee
6/88-6/89	Member, Center for Academic Computing Director's Search Committee
9/89-8/90	Member, College of Science Promotion and Tenure Committee
12/90-5/91	Chair, Computer Science Headship Search Committee
6/91-5/92	Member, College of Engineering Dean's Search Committee
6/92-10/92	Member, CmpSc/CmpEngr Future Committee
9/93-	Member, Computer Science and Engineering (CSE) Promotion and Tenure Committee (9/93-7/97, 8/99-7/01, 8/02-7/04 and 8/06-8/10), Chair in 9/93-8/94, 8/99-7/00, 8/02-7/04, 8/06-7/07
8/94-6/99	Member (elected), College of Engineering (CoE) Promotion and Tenure Committee (8/94-9/96 & 7/97-6/99), Chair in 1997/98
8/94-6/98	Chair, CSE Climate Committee
9/95-3/96	Chair, Committee to Review the Office of The Department Head of Electrical Engineering
9/96-7/97	Chair, CSE Department Head Search Committee
9/96-8/98	Member, University Standing Joint Committee on Tenure
7/96-6/00	Member (elected), Graduate Council, Chair, Fellowships and Awards Committee in 7/97-8/00
8/97-10/97	Member, CoE Search Committee for the Associate Dean for Graduate Studies and Research
9/97-8/99	Member, University Information Science and Technology Programs Strategic Planning Group and Implementation Committee
8/98-7/99	Chair, CSE Curriculum Committee
7/98-7/02	Member, PA Pittsburgh Digital Greenhouse (PDG) Technical Advisory Board

9/99-3/00 Chair, Senior Associate Dean of the Graduate School Search Committee
9/00-6/01 Member, Eberly College of Science Promotion and Tenure Committee
10/00-5/00 Member, CSE Department Head Search Committee
9/01-6/02 Member, CSE Faculty Recruiting Committee
9/02-2/03 Chair, PSU RA10 Committee
2/05- Chair, CSE Teaching Committee and CSE Space Committee
1/06-12/08 Member, PSES Premier Research Award Selection Committee
1/06-12/08 Member, PSU Faculty Scholar Medal Selection Panel
9/07-8/08 Member, CoE Distinguished Professor Selection Committee
1/10- Member, PSU RA10 Investigatory Committee of Dr. Michael Mann

*Research Contributions (External Funding, PhD Students, Publications (journal publications in **bold**))*

*Influenced by her thesis advisor, Dr. James Robertson (the "R" in SRT division made (in)famous by Intel with their Pentium divider bug) and with support from NSF, Dr. Irwin's early work expanded on her dissertation research in **computer arithmetic**. Her professional service in the area includes continuing involvement in the bi-annual IEEE Computer Arithmetic Conference series, serving as program chair in 1987, program co-chair in 1993, and on the Steering Committee since 1999.*

Funding:
7/78-6/79 PSU ACOR Research Initiation Grant, Algorithms for On-Line Arithmetic; $4,562
7/78-6/80 NSF/MCS Grant, 7809126, On-Line Algorithms for Computer Arithmetic; $43,454
7/80-6/82 NSF/MCS Grant, 7809126A01, VLSI Architectures/Algorithms for Recursive Computations (with D. Heller); $125,820
6/82 NSF/MCS Gant, 8203793, Computer Research Equipment (with D. Heller, R. M. Owens); $55,653

Ph.D. Students:
Robert M. Owens, Ph.D. 8/80, Digit On-Line Algorithms for Pipeline Architectures, Professor, PSU (deceased)

Publications:
M. J. Irwin, A Pipelined Processing Unit for On-Line Division, *Proc. of the 5th Annual Symp. on Computer Architecture (ISCA)*, pp. 24-30, April 1978. Also published in Computer Architecture News, 6:7, April 1978.
M. J. Irwin, Reconfigurable Pipeline Systems, *Proc. of ACM '78*, pp. 86-92, Dec. 1978.
R. M. Owens, M. J. Irwin, On-Line Algorithms for the Design of Pipeline Architectures, *Proc. of the 6th ISCA*, pp. 12-19, April 1979. Also published in *Computer Architecture News*, 7:6, April 1979.
M. J. Irwin, D. Heller, On-Line Pipeline Systems for Recursive Numeric Computations, *Proc. of the 7th ISCA*, pp. 292-299, May 1980. Also published in *Computer Architecture News*, 8:3, May 1980.
M. J. Irwin, D. Smith, A Rational Arithmetic Processor, *Proc. of the 5th Symp. on Computer Arithmetic (ARITH)*, pp. 241-244, May 1981.
B. Mackay, M. J. Irwin, A Simulator for Digit Online Arithmetic, *Proc. of the Inter. Conf. on Parallel Processing (ICPP*), pp. 304-306, Aug. 1982.
M. J. Irwin, R. M. Owens, Fully Digit Online Networks, *IEEE Trans. on Computers*, C-32(4):402-406, April 1983. Also appeared in *Computer Arithmetic, II,* Ed. E. Swartzlander, IEEE Press, 1990.
R. M. Owens, M. J. Irwin, Numerical Limitations on the Design of Digit On-Line Networks, *Proc. of the ARITH*-6, pp. 156-161, June 1983.
C. Zhang, M. J. Irwin, A Mesh-Connected VLSI Design for Binary Addition, *Proc. of the 1st Inter. Conf. on Computers and Applications*, June 1984.
T-F Ngai, M. J. Irwin, Regular, Area-Time Efficient Carry-Lookahead Adders, *Proc. of the ARITH-7*, pp. 9-15, June 1985.
T-F Ngai, M. J. Irwin, S. Rawat, Regular, Area-Time Efficient Carry-Lookahead Adders, *Journal of Parallel and Distributed Computing,* 3(1):92-105, Academic Press, March 1986.

*In the fall of 1981, Dr. Irwin began an almost two decade long research collaboration with Robert M. Owens, her first PhD student who had joined the faculty at PSU, until his untimely death in 1997. Their research focused in **application specific architectures** supported by ONR, ARO, NSF, and industry. This work included the design, implementation, and field-testing of three very different board level designs - the Arithmetic Cube, the MGAP (two generations of boards), and SPARTA. The first two, that involved the design and fabrication of custom CMOS parts, were targeted at applications in the signal and image processing domain. They combined new algorithms and*

architectures for digital signal processing with novel computer arithmetic techniques to achieve high-speed processing in single board configurations. They also required the development of extensive system software. The Arithmetic Cube and both generations of the MGAP were demoed at the Supercomputing Conferences. The MGAP-2 was also demoed at the CNSF exhibit in Washington, DC before members of congress and their staff. The SPARTA board, based on FPGAs, was designed to do near real-time simulation of physical modeling transformations on deformable objects. Work in application specific architecture design, both custom and mapping to FPGAs continues with her colleague, N. Vijaykrishnan, and their students. Her professional service in the area includes being on the editorial board of the Journal of VLSI Signal Processing from 1988 to 2001 and on the SiPS program committee from 2001 to 2005.

Funding:

7/82-10/88	ONR Contract, N00014-80-C-0517, Fundamental Research Initiatives, Signal Processing (with J. Barlow, R. M. Owens, G. Schnitger, J. Simon); $212,270
8/83-2/87	ARO Contract, DAAG29-83-K-0126, Digit Online Architectures (with R. M. Owens); $349,206
1/85-12/85	HRB Singer Contract, A VLSI Video Processor (with R. M. Owens, J. Simon); $37,500
6/85	NSF/DCR Grant, 8504847, Computer Research Equipment (with T. Maida, R. M. Owens, J. Simon); $100,000
9/87-9/91	ARO Contract, DAAL03-87-K-0118, Signal Processing Algorithms for Heterogeneous Architectures (with R. M. Owens); $456,287
5/89-4/92	NSF/MIP Grant, 8902636, The Arithmetic Cube System Prototype (with R. M. Owens); $676,778
7/91-6/94	NSF/MIP Grant, 9102500, High Performance, Fine Grained, Application Specific, VLSI Architectures (with R. M. Owens); $253,078
7/94-6/97	NSF/MIP Grant, 9408921, Architecture, Algorithms, and Software Issues in the Design of a Massively Parallel Fine-Grain Processor (with R. M. Owens); $620,355
3/97-12/99	NSF/CDA Grant, 9617308, Prototyping Equipment for Application Specific Architectures (with R. M. Owens); $80,770
1/00-9/00	PA/PDG Grant, SPARTA: Simulation of Physics on a Real Time Architecture (with B. Bishop); $50,309

Ph.D. Students:

Poras Balsara, Ph.D. 8/89, A VLSI-Based Architecture for Computer Vision, Professor, Univ. of Texas at Dallas

Tom Kelliher, Ph.D. 12/92, High Performance Memory Architectures, Associate Professor, Goucher College, PA

Paul Keltcher, Ph.D. 5/96, Performance Evaluation of Parallel Computers with Consideration to Large Design Spaces (co-advised with R.M. Owens), AMD, Foxborough, MA [American Indian]

Heung-Nam Kim, Ph.D. 8/96, Motion Estimation Algorithms and Architectures, Head, Embedded Software Technology Center, Electronics and Telecommunications Research Institute (ETRI), KOREA

Kevin Acken, Ph.D. 8/97, Low Power Architectural Optimizations for 3D Graphics Subsystems (co-advised with R.M. Owens), NVIDIA, San Jose, CA

Ben Bishop, Ph.D. 12/00, Issues in High Performance Multimedia, Associate Professor, University of Scranton

Theo Theocharides, Ph.D. 5/06, Embedded Hardware Face Detection (co-advised with N. Vijaykrishnan), Lecturer, University of Cyprus

Joo-Heung Lee, Ph.D. (EE) 08/06, VLSI Architectures for Video Applications (co-advised with N. Vijaykrishnan), Assistant Professor, University of Central Florida

Publications:

S. Rawat, P.T. Balsara, M. J. Irwin, T. Mackowiak, Design and Implementation of a Real Time Video Processor, *Proc. of Inter. Conf. on Accoustics, Speech, and Signal Processing (ICASSP)*, pp. 2215-2218, April 1986.

S. Adams, M. J. Irwin, R. M. Owens, A Parallel, General Purpose CAM Architecture, *Proc. of the 4th MIT Conf. on Advanced Research in VLSI*, pp. 51-71, April 1986.

R. M. Owens, M. J. Irwin, The Arithmetic Cube and Its Associated Algorithms, *Proc. of the Workshop on Future Directions in Computer Architecture and Software*, pp. 38-47, May 1986.

R. M. Owens, M. J. Irwin, An Area Efficient VLSI FIR Filter, in *VLSI Signal Processing, II*, Ed. S-Y Kung, R.E. Owen, J.G. Nash, pp. 188-199, IEEE Press, 1986.

T. Mackowiak, R. M. Owens, M. J. Irwin, The Arithmetic Cube Digital Signal Processor, *GOMAC-86 Digest*, pp. 395-398, Nov. 1986.

P. Balsara, S. Rawat, M. J. Irwin, Design of Fast Pipelined Arithmetic Units in VLSI, *Proc. of the Platinum Jubilee Conf. on Systems and Signal Processing*, Dec. 1986. **Also appeared in *The Journal of the Indian Institute of Science*, 67:413-422, Nov. 1987.**

M. J. Irwin, R. M. Owens, Digit Pipelined Processors, *The Journal of Supercomputing*, 1(1):61-86, Jan. 1987.

R. M. Owens, M. J. Irwin, The Arithmetic Cube, *IEEE Trans. on Computers*, C-36(11):1342-1348, Nov. 1987.

R. M. Owens, M. J. Irwin, Multidimensional Algorithms for VLSI Processors, *Proc. of ICASSP-88*, pp. 749-752, April 1988.

M. J. Irwin, A Digit Pipelined Dynamic Time Warp Processor, *IEEE Trans. on ASSP*, 36(9):1412-1422, Sept. 1988.

M. J. Irwin, R. M. Owens, A Comparison of Two Digit Serial VLSI Adders, *Proc. of Inter. Conf. on Computer Design (ICCD)*, pp. 227-229, Oct. 1988.

C-M Wu, R. M. Owens, M. J. Irwin, A VLSI Space Warper, in *VLSI Signal Processing, III*, Ed. R. Brodersen, H. Moscovitz, pp. 39-49, IEEE Press, 1988.

M. J. Irwin, R. M. Owens, Design Issues in Digit Serial Signal Processors, *Proc. of Inter. Symp. on Circuits and Systems (ISCAS)*, pp. 441-444, May 1989.

R. M. Owens, M. J. Irwin, Implementing Algorithms for Convolution on an Array of Adders, *Proc. of ICASSP-89*, pp. 1127-1130, May 1989.

M. J. Irwin, R. M. Owens, Digit Serial Systolic VLSI Architectures, *Proc. of the Inter. Conf. on Systolic Arrays*, pp. 215- 224, June 1989.

P. Balsara, M. J. Irwin, Parallel Algorithms for Region Labeling on a Memory Array Architecture, *Proc. of the 1989 Conf. on Image Processing*, pp. 384-388, Sept. 1989.

R. M. Owens, M. J. Irwin, The Arithmetic Cube: A Highly Parallel VLSI DSP Architecture, *Proc. of IFIP Workshop on Parallel Architectures on Silicon*, pp. 212-226, Dec. 1989.

C-M Wu, R. M. Owens, M. J. Irwin, Distortion Processing in Image Matching Problems, *Proc. of ICASSP-90*, pp. 2181-2184, April 1990.

M. J. Irwin, R. M. Owens, A Two-Dimensional Distributed Logic Processor for Vision Processing Algorithms, *Proc. of ICASSP-90*, pp. 945-948, April 1990.

M. J. Irwin, R. M. Owens, A Case for Digit Serial VLSI Signal Processors, *The Journal of VLSI Signal Processing*, 1(4):321-334, Kluwer, April 1990.

R. M. Owens, M. J. Irwin, Being Stingy with Multipliers, *IEEE Trans. on Computers*, 39(6):809-818, June 1990.

C-M Wu, R. M. Owens, M. J. Irwin, Mapping High-Dimension Wavefront Computations to Silicon, *Proc. of Application Specific Array Processing Conf. (ASAP)*, pp. 78-89, Sept. 1990.

R. M. Owens, M. J. Irwin, T. Kelliher, C-M Wu, The Design of the Arithmetic Cube II, in *VLSI Signal Processing, IV*, pp. 95-105, IEEE Press, Nov. 1990.

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Due to the lack of tools to support their design efforts, in 1984 Drs. Irwin and Owens began a research effort to develop a suite of ***architecture, logic, and circuit design tools*** *ranging from module layout (ARTIST and PERFLEX), to logic synthesis (LOGICIAN), to VHDL behavioral synthesis (DECOMPOSER). The tools were used to synthesize the custom CMOS parts for the Arithmetic Cube (from behavioral VHDL to layout) and portions of the MGAP architecture. The innovative approach to logic synthesis focused on minimizing communication complexity, the heuristics developed for performance driven custom module generation, and the routing algorithms developed for module generation based on an elegant Steiner routing heuristic (now referred to as the BOI algorithm) have all found their way into commercial products. Another outcome of this work was the discovery (by the communication complexity based logic synthesis program) of a new parallel prefix adder design (the ELM adder) that has superior energy-delay characteristics to other prefix adders that is reputed to be used in a number of commercial parts. Dr. Irwin's professional service in this area included membership on the Executive Committee of the annual Design Automation Conference (a conference with about 4,000 technical attendees and a large commercial exhibition) from 1990 to 2001, with Dr. Irwin serving as conference general chair in 1999. She also served for four years as the Editor-in-Chief of ACM's Transactions on the Design Automation of Electronic Systems (TODAES).*

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In late 1993, recognizing that energy consumption was fast becoming the next important design constraint, Dr. Irwin began a focused research effort in the area of ***resource constrained systems design*** *including embedded systems that have limited battery life and limited memory space and sensor network systems that have extremely limited resourses. She works with a team of researchers including Dr. Vijay Narayanan (N. Vijaykrishnan), Dr. Kandemir, and Dr. Xie. Their work has been supported by NSF, DARPA/MARCO/GSRC, PA/PDG, and industry. The uniqueness of their research is an holistic approach that spans the space from low power circuit design, to micro-architecture design, to system software design (compilers, operating systems, Java virtual machines), to application system design (databases, sparse matrix solvers) along with the design and implementation of the simulation tools necessary to support the design of resource constrained systems. Their architectural level power simulator, SimplePower, was made publicly available in November 2000 and has been distributed to over 200 sites worldwide. Dr. Irwin's professional service in the area includes continuing involvement in the annual International Low Power Symposium on Electronics and Design series, serving as program co-chair in 2001, as general co-chair in 2002, and on the*

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With the emergence of promising new "nano" technologies another new line of multidisciplinary research has emerged – that of mixed technology circuits. The initial focus is on ***nanotechnologies*** *that are used to augment CMOS circuitry such as new input/output technologies, new non-volatile memory structures, etc. Another "advanced technology" issue is that of* ***3D integrated circuits*** *– where a stack of multiple device layers with direct vertical interconnections between the layers (through silicon vias (TSVs)) are put together in the same package. As fabrication of 3D ICs becomes a reality, developing CAD tools to support their design and exploring new architectural alternatives have become an interest.*

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8/03-7/07 NSF/NIRT Grant, 0303981, Heterogeneous Integration of Nanowires for Chemical Sensor Arrays (with T. Mallouk, Chemistry, T. Mayer, EE, S. Evoy, EE, UPenn); $1,200,000 ($350,000 to CSE)

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While the original motivation for research in the design of power aware systems was in the mobile and embedded space, it has also become an issue in the server and high-performance computing space where both energy consumption and thermal (cooling) have become major constraints. Thus, the research with Dr. Vijay Narayanan (N. Vijaykrishnan), Dr. Kandemir, and Dr. Xie has expanded to cover that space with a focus on the design of high performance, power-efficient, resilient ***chip multiprocessors*** *(CMPs) and multiprocessor systems on a chip (MPSoC). A project with Dr. Raghavan - called pxp - focused on optimizing the performance and power of computational science applications on high-performance systems. This work has been supported by NSF and DARPA/MARCO/GSRC.*

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9/04-8/07 NSF/STHEC Grant, 0444345, Adaptive Software for Extreme-Scale Scientific Computing: Co-Managing Quality-Performance-Power Tradeoffs (with P. Raghavan, Norris, and McInnes); $749,755

9/06-10/09 MARCO/DARPA Focus Research Center Program (FCRP), Gigascale Systems Research Center (GSRC), Concurrent Systems Theme; $185,600 (9/06-8/07), $158,625 (9/07-8/08), $160,000 (9/08-10/09)

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9/07-8/09 NSF/CSR-AES, 0720645, REEact: A Robust Execution Environment for Fragile Multicores (with M. Kandemir), $50,000

8/08-7/11 NSF/CPA-CPL, 0811687, REEact: A Robust Execution Environment for Fragile Multicore Systems (with M. Kandemir), $599,999

Ph.D. Students:

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Aditya Yanamandra, Ph.D., 8/10, Exploring Power Reliability Tradeoffs in On-Chip Networks, (co-advised with V. Narayanan), Intel, Portland, Oregon

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