

## Curriculum Vitae

### MARY JANE IRWIN

*Evan Pugh Professor*

*A. Robert Noll Chair in Engineering*

#### *Personal*

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#### *Education*

1977 Ph.D. Computer Science, University of Illinois at Urbana-Champaign (UIUC)

1975 M.S. Computer Science, UIUC

1971 B.S. Mathematics, Memphis State University (magna cum laude)

#### *Employment*

7/06- Evan Pugh Professor, Computer Science and Engineering, PSU

7/03- A. Robert Noll Chair in Engineering, Computer Science and Engineering, PSU

1/99-7/03 Distinguished Professor, Computer Science and Engineering, PSU

7/89-1/99 Professor, Computer Science and Engineering, PSU

7/91-6/93 Department Head, Computer Science, PSU

1/86-7/86 Research Staff, Supercomputing Research Center, Institute for Defense Analysis, Bowie, MD

8/77-7/89 Associate Professor, Assistant Professor, Computer Science, PSU

1/72-8/77 Graduate Research and Graduate Teaching Assistant, Computer Science, UIUC

#### *Research Interests*

Computer architecture (resource constrained, application specific, chip multiprocessors) and computer arithmetic;

Energy aware systems design; Reliable systems design; VLSI systems design and emerging technologies

#### *Awards and Honors*

Outstanding Teacher Award, PSU Computer Science Club (1981); ACM/SIGDA Leadership Award (1993); IEEE Fellow (1994); PSU/PSES Outstanding Research Award (1995); ACM Fellow (1996); CIC Academic Leadership Program Fellow (1996-97); Honorary Doctorate, Chalmers University, Sweden (1997); PSU/PSES Premier Research Award (2001); Elected to the National Academy of Engineering (2003); IEEE/CAS VLSI Transactions Best Paper of the Year Award (2003); DAC Marie R. Pistilli Women in EDA Award (2004); ACM/SIGDA Distinguished Service Award (2005 and 2007); ACM Distinguished Service Award (2005); CRA Distinguished Service Award (2006); PSU Howard B. Palmer Faculty Mentoring Award (2006); IEEE ICPADS Best Paper Award (2006); Anita Borg Technical Leadership Award (2007); IPDPS Best Paper Award (2008); Elected to the American Academy of Arts and Sciences (2009); ACM Athena Lecturer Award (2010)

#### *Selected Keynote/Feature/Plenary Talks and Distinguished Lectures*

SiPS'99 Feature Talk, Taipei, TAIWAN, 1999; KAIST Distinguished Lecturer, Korea, 2000; PATMOS Feature Talk, Göttingen, Germany, 2000; Dortmund Summer School Lecturer, Dortmund, GERMANY, 2000; COLP'00 Workshop Keynote, Philadelphia, PA, 2000; NSF/CISE Molecular Architectures Workshop Invited Talk, Notre Dame, 2001; Eli Lilly Distinguished Lecturer, Univ. of Pittsburgh, 2002; ISVLSI Invited Talk, Tampa, FL, 2003; IBM ACEED'03 Invited Talk, Austin, TX, 2003; MPSoC Summer School Lecturer, Chamonix, France, 2003 and Provence, France, 2004; Smith Distinguished Lecturer, UC Irvine, 2005; Distinguished Lecturer, Univ. of Virginia, 2005; Distinguished Lecturer, University of Minnesota, 2007; CCSCNE-07 Conference Plenary, Rochester, NY, 2007; CRA-W Distinguished Lecturer, University of South Florida, 2007; Distinguished

Lecturer, Georgia Institute of Technology, 2008; HiPEAC Workshop on Design for Reliability Keynote, Cyprus, 2009; ISCA 2010 Plenary, St. Malo, France, 2010

*Selected Association/Society Memberships and Professional Activities*

Memberships: Association for Computing Machinery (ACM), SIGARCH, SIGDA, SIGBED; Institute for Electrical and Electronics Engineers (IEEE) Computer Society, IEEE SP Society, IEEE CAS Society, IEEE SSC Society; International Federation for Information Processing (IFIP) Sections 10.2 and 10.3

- 5/85- Program Committee Member and Publicity Chair, 7th Symp. on Computer Arithmetic (ARITH7), 1985; Program Chair, ARITH8, 1987; Program Committee Member, ARITH9, 1989 and ARITH10, 1991; Program Co-Chair, ARITH11, 1993; Program Committee Member, ARITH12, 1995 and ARITH13, 1997; Steering Committee Member, ARITH14 - present
- 7/85-6/91 Secretary/Treasurer (elected), ACM SIGARCH
- 11/86-12/91 Advisory Committee Member, MIPS Division, CISE Directorate, NSF
- 1/88-12/01 Editorial Board Member, *Journal of VLSI Signal Processing*, Kluwer Academic Publisher
- 1/89-12/91 Subject Area Editor, *Journal of Parallel and Distributed Computing*, Academic Press
- 1/89-12/91 Member, Eckert Mauchley Award Committee (Chair in 1991), ACM and IEEE Computer Society
- 2/89-8/04 Member, Board of Directors, ACM/SIGDA
- 7/90-7/01 Member, Design Automation Conference (DAC) Executive Committee; Pub. Chair, DAC'91; Tutorials Chair, DAC'92; ACM Rep., DAC'93, DAC'94 and DAC'95; Finance Chair, DAC'96 and DAC'97; Vice Chair, DAC'98; General Chair, DAC'99; Past Chair, DAC'00; Tutorials Chair, DAC'01
- 5/91- 4/93 Program Chair, ACM/SIGDA Physical Design Workshop (PDW), PDW'91; Proc. Chair, PDW'93
- 1/91-6/95 Member, Editorial Board, *IEEE Transactions on Computers*
- 7/91-6/03 Member (elected), Computer Research Association (CRA) Board of Directors, Vice Chair in 7/95-6/97
- 1/92-12/95 Member, Publication Board (Pubs/Press Planning Committee Chair in 92-93), IEEE Computer Society
- 1/93-12/95 Member (elected), IEEE Computer Society Board of Governors
- 7/93-6/03 Member (elected), Board of Directors, ACM/SIGARCH
- 7/94-6/97 Member (elected), ACM Council
- 6/96 General Chair, Federated Research Computing Conference (FCRC), Philadelphia, PA
- 7/96-6/98 Vice President (elected), ACM
- 8/97- Finance Chair and Program Committee Member, Inter. Symp. on Low Power Electronics and Design (ISLPED), ISLPED'97, ISLPED'98, ISLPED'99, and ISLPED'00; Technical Program Co-Chair, ISLPED'01; General Co-Chair, ISLPED'02; Steering Committee Member, ISLPED'03 - present
- 12/97 US Program Chair, Inter. Conf. on High Performance Computing (HiPC), Bangalore, India
- 1/98-12/09 Member, ACM/SIGARCH Wilkes Award Committee (1/98-12/00 & 1/07-12/09), Chair in 2000 & 2008
- 1/98-6/03 Member, NSF CISE Directorate Advisory Committee, Chair in 1/02-6/03
- 7/98 General Co-Chair, The CRA Conference at Snowbird, Snowbird, UT
- 10/98-8/04 Editor-in-Chief, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*
- 4/00 General Co-Chair, IEEE VLSI Workshop, Orlando, FL
- 5/00-8/04 Member, Army Research Lab Technical Advisory Board (ARLTAB), Chair of ARL/DCS Panel
- 12/00 Co-Chair, MICRO-33 Kool Chips Workshop, Monterey, CA
- 11/01-10/04 Program Committee Member, Compilers, Architectures and Synthesis for Embedded Systems (CASES) Conference, CASES'01 and CASES'02; General Co-Chair, CASES'04
- 5/02-6/08 Member, ACM Publications Board (Co-Chair, 1/05-6/07)
- 10/02- Program Committee Member, Languages, Compiler and Tools for Embedded Systems (LCTES) Conference, LCTES'03 and LCTES'04; General Chair, LCTES'06; Steering Committee Member, LCTES'07 - present
- 3/03-12/05 Member, NRC Committee on the Future of Supercomputing
- 1/04-12/06 Member, NAE Section 5 Peer Committee, Chair in 2006
- 1/07-12/08 NAE Section 5 Search Executive
- 3/04-12/06 Co Editor-in-Chief, *ACM Journal on Emerging Technology in Computing Systems (JETC)*
- 1/05- Member, IDA/Center for Computer Science (CCS) Program Review Committee
- 6/06-7/09 Member, NAE Russ Prize Committee, Chair in 2008, Past Chair in 2010
- 1/07- Member, Board on Army Science and Technology (BAST)
- 7/06- Member, Microsoft Research (MSR) External Research Advisory Board
- 9/08-8/13 Member, ACM Fellow Selection Committee

2/09-1/12 Member, NAE Committee on Membership (CoM), Vice Chair Class of 2011, Chair Class of 2012  
 3/09 Program Chair, Inter. Conf. on Architectural Support for Programming Languages and Operating Systems (ASPLOS)

Recent Program Committee Memberships: Conference on Computer Architectures for Machine Perception (CAMP), CAMP'97 and CAMP'00; Signal and Image Processing Systems (SIPS) Symposium, SIPS'01 through SIPS'05; Inter. Symposium on High Performance Computer Architecture (HPCA), HPCA'05; Inter. Parallel and Distributed Processing Symposium (IPDPS), IPDPS'06 and IPDPS'11; ACM/IEEE Microarchitecture Conference (MICRO), MICRO'06, MICRO'09, MICRO'10; ACM/IEEE Inter. Symposium on Computer Architecture (ISCA), ISCA'08; Inter. Conf. on High Performance Embedded Architectures and Compilers (HIPEAC), HIPEAC'09 and HIPEAC'10; Inter. Conf. on Parallel Architectures and Compilation Techniques (PACT), PACT'10

Recent External Department Review Committees: Electrical and Computer Engr, Purdue (2006), Computer Science, Syracuse (2008), Electrical and Computer Engr., UIUC (2008), Computer Science, Yale (2010)

### *Selected Educational Activities*

Conference and University Tutorials: Low Power Design for SoCs at ASIC, Washington, DC, 9/99 (half-day, sole presenter); Low Power Design: From Soup to Nuts at ISCA'00, Vancouver, BC, 06/00 (full-day, two presenters); Low Power Design Methodologies: Hardware and Software Issues at PACT'00, Philadelphia, PA, 10/00 (full-day, two presenters); Power-Efficient Design at ISCA'01, Goteborg, Sweden, 7/01 (full-day, four presenters); Low Power Design: From Circuits to Software, Tianan, Taiwan, 10/02 (half-day, sole presenter)  
 PSU Undergraduate Courses: Computer Programming for Engineers (201); Introduction to Digital Systems (271); Computer Organization and Design (331); Introduction to Systems Programming; Computer Systems Architecture (431); Operating Systems; VLSI Digital Circuits (477, now 411)  
 PSU Graduate Courses: Fundamentals of Computer Architectures (530); Architecture of Arithmetic Processors (575); VLSI Systems Design (577); Special Topics (598): Embedded Systems, Low Power Design, Emerging Computing Technologies, Reliable Low Power Systems Design

### Most recent seven years of Student Rating of Teaching Effectiveness (SRTEs)

Course/Num. Section	Enrollment	Elective %	Semester/ Year	Number of Respondents (%)	Overall Quality Of Course (out of 7.00)	Overall Quality Of Instruction (out of 7.00)
CSE 477.1	37	48%	Fa03	27 (73%)	5.92	6.38
CSE 598C.1*	19	38%	Fa03	16 (84%)	5.93	6.13
			Sp04**			
CSE 431.1	27	11%	Fa04	19 (70%)	5.00	5.63
CSE 431.2	70	2%	Fa04	53 (76%)	4.94	5.32
CSE 575.1	12	42%	Sp05	12 (100%)	5.83	6.50
CSE 431.1	18	31%	Fa05	16 (89%)	5.75	6.06
CSE 431.2	40	0%	Fa05	27 (68%)	4.96	5.59
			Sp06***			
CSE 331.1****	39	13%	Fa06	23 (59%)	5.43	5.70
			Sp07***			
CSE 331.1****	37	8%	Fa07	24(65%)	4.92	5.17
			Sp08***			
CMPEN 431.1	57	24%	Fa08	37 (65%)	5.32	5.73
CSE 575.1	15	60%	Fa08	10 (67%)	6.20	6.60
			Sp09***			
CSE 331.1****	53	38%	Fa09	24 (45%)	5.63	5.71
			Sp10***			

The normal teaching load for "research active" faculty in CSE is three courses a year.

\* With Narayanan and Kandemir

\*\* On sabbatical Leave

\*\*\* Course Buy Out

\*\*\*\* Section 331.2 taught by Graduate Teaching Intern under my direct supervision

Graduated more than twenty Ph.D. students and eighty M.S. students during the period 1978 to 2009 (see *Research Contributions* section for detailed listing of Ph.D. students)

#### *Selected Outreach Activities*

- 6/91- Member, Steering Committee of the Computing Research Association's Committee on the Status of Women in Computing Research (CRA-W), Co-Chair in 6/93-7/96, CRA-W Awards Chair, 1996-2009, CAPP Project Co-Chair, 2004-2008, Grad Cohort Co-Chair, 2005-2008, frequent presenter at CRA-W Career Mentoring Workshops, CRA-W Grad Cohort, and CRA-W CAPP
- 7/94-6/96 Chair, PSU Women in Science and Engineering (WISE) Network Executive Committee (Interim Director in 1/95-8/95)
- 7/96-6/01 Member, PSU Commission For Women (CFW); Member, CFW Executive Committee, Chair of the Faculty/Student Issues and Policies Committee, 7/97-6/98; Chair Elect, CFW, Member, CFW Executive Committee, Member, Faculty Issues and Policies Committee, Chair, CFW Banquet Committee, 7/98-6/99; Chair, 7/99-6/00; Past Chair, 7/00-6/01
- 7/97- Ex-Officio Member, Women in Engineering Program Advisory Committee
- 1/05- Member, College of Engineering, Women in Engineering Leadership Team
- 10/09 Panelist, Speaker, AAAS PAESMEM Workshop for Women: Building Science, Engineering, and Technology Leaders, Washington, D.C.

#### **Funding:**

- 5/89-590 ACM/SIGDA, DAC Graduate Academic Scholarships; \$22,000
- 7/94-6/97 NSF/CDA, 9416785, CRA Committee on the Status of Women in CSE (with F. Berman, UCSD); \$132,433
- 7/95-12/95 Sloan, Assessing Retention Data, Perceptions, Climate, and Mentoring for Women in Science and Engineering at Penn State (with L. Schiebinger); \$29,899
- 1/05-1/09 Microsoft and Google, CRA-W Grad Cohort Program (with M.L. Sofa, UVA); \$125,000 Microsoft and \$125,000 Google per year (2005, 2006, 2007, and 2008)
- 1/06-12/09 NSF/ADVANCE Leadership, 0545229, CRA-W CAPP-R and CAPP-E Program (with M.L. Sofa, UVA); \$268,602

#### *Selected Other Penn State University Academic and Administrative Activities*

- 9/79-8/80 Member, Provost's Committee for Administrative Review of the Office of the Dean, College of Science
- 9/79-6/82 Member, Computer Science Headship Search Committee
- 9/79-5/83 Chair, Computer Science Computing Facilities Committee
- 9/80-6/91 Advisor, Univ. Scholars Program
- 9/83-8/84 Graduate Officer, Computer Science
- 9/83-9/89 Member, Univ. Faculty Advisory Committee on Academic Computing
- 9/83-7/91 Member, Computer Science Promotion and Tenure Committee (9/83-7/85 and 8/88-7/91)
- 1/87-6/89 Member, College of Science Dean's Search Committee
- 6/88-6/89 Member, Center for Academic Computing Director's Search Committee
- 9/89-8/90 Member, College of Science Promotion and Tenure Committee
- 12/90-5/91 Chair, Computer Science Headship Search Committee
- 6/91-5/92 Member, College of Engineering Dean's Search Committee
- 6/92-10/92 Member, CmpSc/CmpEngr Future Committee
- 9/93- Member, Computer Science and Engineering (CSE) Promotion and Tenure Committee (9/93-7/97, 8/99-7/01, 8/02-7/04 and 8/06-8/10), Chair in 9/93-8/94, 8/99-7/00, 8/02-7/04, 8/06-7/07
- 8/94-6/99 Member (elected), College of Engineering (CoE) Promotion and Tenure Committee (8/94-9/96 & 7/97-6/99), Chair in 1997/98
- 8/94-6/98 Chair, CSE Climate Committee
- 9/95-3/96 Chair, Committee to Review the Office of The Department Head of Electrical Engineering
- 9/96-7/97 Chair, CSE Department Head Search Committee
- 9/96-8/98 Member, University Standing Joint Committee on Tenure
- 7/96-6/00 Member (elected), Graduate Council, Chair, Fellowships and Awards Committee in 7/97-8/00
- 8/97-10/97 Member, CoE Search Committee for the Associate Dean for Graduate Studies and Research
- 9/97-8/99 Member, University Information Science and Technology Programs Strategic Planning Group and Implementation Committee
- 8/98-7/99 Chair, CSE Curriculum Committee
- 7/98-7/02 Member, PA Pittsburgh Digital Greenhouse (PDG) Technical Advisory Board

- 9/99-3/00 Chair, Senior Associate Dean of the Graduate School Search Committee
- 9/00-6/01 Member, Eberly College of Science Promotion and Tenure Committee
- 10/00-5/00 Member, CSE Department Head Search Committee
- 9/01-6/02 Member, CSE Faculty Recruiting Committee
- 9/02-2/03 Chair, PSU RA10 Committee
- 2/05- Chair, CSE Teaching Committee and CSE Space Committee
- 1/06-12/08 Member, PSES Premier Research Award Selection Committee
- 1/06-12/08 Member, PSU Faculty Scholar Medal Selection Panel
- 9/07-8/08 Member, CoE Distinguished Professor Selection Committee
- 1/10- Member, PSU RA10 Investigatory Committee of Dr. Michael Mann

*Research Contributions (External Funding, PhD Students, Publications (journal publications in **bold**))*

*Influenced by her thesis advisor, Dr. James Robertson (the "R" in SRT division made (in)famous by Intel with their Pentium divider bug) and with support from NSF, Dr. Irwin's early work expanded on her dissertation research in **computer arithmetic**. Her professional service in the area includes continuing involvement in the bi-annual IEEE Computer Arithmetic Conference series, serving as program chair in 1987, program co-chair in 1993, and on the Steering Committee since 1999.*

**Funding:**

- 7/78-6/79 PSU ACOR Research Initiation Grant, Algorithms for On-Line Arithmetic; \$4,562
- 7/78-6/80 NSF/MCS Grant, 7809126, On-Line Algorithms for Computer Arithmetic; \$43,454
- 7/80-6/82 NSF/MCS Grant, 7809126A01, VLSI Architectures/Algorithms for Recursive Computations (with D. Heller); \$125,820
- 6/82 NSF/MCS Gant, 8203793, Computer Research Equipment (with D. Heller, R. M. Owens); \$55,653

**Ph.D. Students:**

Robert M. Owens, Ph.D. 8/80, Digit On-Line Algorithms for Pipeline Architectures, Professor, PSU (deceased)

**Publications:**

- M. J. Irwin, A Pipelined Processing Unit for On-Line Division, *Proc. of the 5th Annual Symp. on Computer Architecture (ISCA)*, pp. 24-30, April 1978. Also published in *Computer Architecture News*, 6:7, April 1978.
- M. J. Irwin, Reconfigurable Pipeline Systems, *Proc. of ACM '78*, pp. 86-92, Dec. 1978.
- R. M. Owens, M. J. Irwin, On-Line Algorithms for the Design of Pipeline Architectures, *Proc. of the 6th ISCA*, pp. 12-19, April 1979. Also published in *Computer Architecture News*, 7:6, April 1979.
- M. J. Irwin, D. Heller, On-Line Pipeline Systems for Recursive Numeric Computations, *Proc. of the 7th ISCA*, pp. 292-299, May 1980. Also published in *Computer Architecture News*, 8:3, May 1980.
- M. J. Irwin, D. Smith, A Rational Arithmetic Processor, *Proc. of the 5th Symp. on Computer Arithmetic (ARITH)*, pp. 241-244, May 1981.
- B. Mackay, M. J. Irwin, A Simulator for Digit Online Arithmetic, *Proc. of the Inter. Conf. on Parallel Processing (ICPP)*, pp. 304-306, Aug. 1982.
- M. J. Irwin, R. M. Owens, Fully Digit Online Networks, *IEEE Trans. on Computers*, C-32(4):402-406, April 1983. Also appeared in *Computer Arithmetic, II*, Ed. E. Swartzlander, IEEE Press, 1990.**
- R. M. Owens, M. J. Irwin, Numerical Limitations on the Design of Digit On-Line Networks, *Proc. of the ARITH-6*, pp. 156-161, June 1983.
- C. Zhang, M. J. Irwin, A Mesh-Connected VLSI Design for Binary Addition, *Proc. of the 1st Inter. Conf. on Computers and Applications*, June 1984.
- T-F Ngai, M. J. Irwin, Regular, Area-Time Efficient Carry-Lookahead Adders, *Proc. of the ARITH-7*, pp. 9-15, June 1985.
- T-F Ngai, M. J. Irwin, S. Rawat, Regular, Area-Time Efficient Carry-Lookahead Adders, *Journal of Parallel and Distributed Computing*, 3(1):92-105, Academic Press, March 1986.**

*In the fall of 1981, Dr. Irwin began an almost two decade long research collaboration with Robert M. Owens, her first PhD student who had joined the faculty at PSU, until his untimely death in 1997. Their research focused in **application specific architectures** supported by ONR, ARO, NSF, and industry. This work included the design, implementation, and field-testing of three very different board level designs - the Arithmetic Cube, the MGAP (two generations of boards), and SPARTA. The first two, that involved the design and fabrication of custom CMOS parts, were targeted at applications in the signal and image processing domain. They combined new algorithms and*

architectures for digital signal processing with novel computer arithmetic techniques to achieve high-speed processing in single board configurations. They also required the development of extensive system software. The Arithmetic Cube and both generations of the MGAP were demoed at the Supercomputing Conferences. The MGAP-2 was also demoed at the CNSF exhibit in Washington, DC before members of congress and their staff. The SPARTA board, based on FPGAs, was designed to do near real-time simulation of physical modeling transformations on deformable objects. Work in application specific architecture design, both custom and mapping to FPGAs continues with her colleague, N. Vijaykrishnan, and their students. Her professional service in the area includes being on the editorial board of the *Journal of VLSI Signal Processing* from 1988 to 2001 and on the SiPS program committee from 2001 to 2005.

#### **Funding:**

- 7/82-10/88 ONR Contract, N00014-80-C-0517, Fundamental Research Initiatives, Signal Processing (with J. Barlow, R. M. Owens, G. Schnitger, J. Simon); \$212,270
- 8/83-2/87 ARO Contract, DAAG29-83-K-0126, Digit Online Architectures (with R. M. Owens); \$349,206
- 1/85-12/85 HRB Singer Contract, A VLSI Video Processor (with R. M. Owens, J. Simon); \$37,500
- 6/85 NSF/DCR Grant, 8504847, Computer Research Equipment (with T. Maida, R. M. Owens, J. Simon); \$100,000
- 9/87-9/91 ARO Contract, DAAL03-87-K-0118, Signal Processing Algorithms for Heterogeneous Architectures (with R. M. Owens); \$456,287
- 5/89-4/92 NSF/MIP Grant, 8902636, The Arithmetic Cube System Prototype (with R. M. Owens); \$676,778
- 7/91-6/94 NSF/MIP Grant, 9102500, High Performance, Fine Grained, Application Specific, VLSI Architectures (with R. M. Owens); \$253,078
- 7/94-6/97 NSF/MIP Grant, 9408921, Architecture, Algorithms, and Software Issues in the Design of a Massively Parallel Fine-Grain Processor (with R. M. Owens); \$620,355
- 3/97-12/99 NSF/CDA Grant, 9617308, Prototyping Equipment for Application Specific Architectures (with R. M. Owens); \$80,770
- 1/00-9/00 PA/PDG Grant, SPARTA: Simulation of Physics on a Real Time Architecture (with B. Bishop); \$50,309

#### **Ph.D. Students:**

- Poras Balsara, Ph.D. 8/89, A VLSI-Based Architecture for Computer Vision, Professor, Univ. of Texas at Dallas
- Tom Kelliher, Ph.D. 12/92, High Performance Memory Architectures, Associate Professor, Goucher College, PA
- Paul Keltcher, Ph.D. 5/96, Performance Evaluation of Parallel Computers with Consideration to Large Design Spaces (co-advised with R.M. Owens), AMD, Foxborough, MA [American Indian]
- Heung-Nam Kim, Ph.D. 8/96, Motion Estimation Algorithms and Architectures, Head, Embedded Software Technology Center, Electronics and Telecommunications Research Institute (ETRI), KOREA
- Kevin Acken, Ph.D. 8/97, Low Power Architectural Optimizations for 3D Graphics Subsystems (co-advised with R.M. Owens), NVIDIA, San Jose, CA
- Ben Bishop, Ph.D. 12/00, Issues in High Performance Multimedia, Associate Professor, University of Scranton
- Theo Theocharides, Ph.D. 5/06, Embedded Hardware Face Detection (co-advised with N. Vijaykrishnan), Lecturer, University of Cyprus
- Joo-Heung Lee, Ph.D. (EE) 08/06, VLSI Architectures for Video Applications (co-advised with N. Vijaykrishnan), Assistant Professor, University of Central Florida

#### **Publications:**

- S. Rawat, P.T. Balsara, M. J. Irwin, T. Mackowiak, Design and Implementation of a Real Time Video Processor, *Proc. of Inter. Conf. on Acoustics, Speech, and Signal Processing (ICASSP)*, pp. 2215-2218, April 1986.
- S. Adams, M. J. Irwin, R. M. Owens, A Parallel, General Purpose CAM Architecture, *Proc. of the 4<sup>th</sup> MIT Conf. on Advanced Research in VLSI*, pp. 51-71, April 1986.
- R. M. Owens, M. J. Irwin, The Arithmetic Cube and Its Associated Algorithms, *Proc. of the Workshop on Future Directions in Computer Architecture and Software*, pp. 38-47, May 1986.
- R. M. Owens, M. J. Irwin, An Area Efficient VLSI FIR Filter, in *VLSI Signal Processing, II*, Ed. S-Y Kung, R.E. Owen, J.G. Nash, pp. 188-199, IEEE Press, 1986.
- T. Mackowiak, R. M. Owens, M. J. Irwin, The Arithmetic Cube Digital Signal Processor, *GOMAC-86 Digest*, pp. 395-398, Nov. 1986.
- P. Balsara, S. Rawat, M. J. Irwin, Design of Fast Pipelined Arithmetic Units in VLSI, *Proc. of the Platinum Jubilee Conf. on Systems and Signal Processing*, Dec. 1986. **Also appeared in *The Journal of the Indian Institute of Science*, 67:413-422, Nov. 1987.**
- M. J. Irwin, R. M. Owens, Digit Pipelined Processors, *The Journal of Supercomputing*, 1(1):61-86, Jan. 1987.**

- R. M. Owens, M. J. Irwin, The Arithmetic Cube, *IEEE Trans. on Computers*, C-36(11):1342-1348, Nov. 1987.**
- R. M. Owens, M. J. Irwin, Multidimensional Algorithms for VLSI Processors, *Proc. of ICASSP-88*, pp. 749-752, April 1988.
- M. J. Irwin, A Digit Pipelined Dynamic Time Warp Processor, *IEEE Trans. on ASSP*, 36(9):1412-1422, Sept. 1988.**
- M. J. Irwin, R. M. Owens, A Comparison of Two Digit Serial VLSI Adders, *Proc. of Inter. Conf. on Computer Design (ICCD)*, pp. 227-229, Oct. 1988.
- C-M Wu, R. M. Owens, M. J. Irwin, A VLSI Space Warper, in *VLSI Signal Processing, III*, Ed. R. Brodersen, H. Moscovitz, pp. 39-49, IEEE Press, 1988.
- M. J. Irwin, R. M. Owens, Design Issues in Digit Serial Signal Processors, *Proc. of Inter. Symp. on Circuits and Systems (ISCAS)*, pp. 441-444, May 1989.
- R. M. Owens, M. J. Irwin, Implementing Algorithms for Convolution on an Array of Adders, *Proc. of ICASSP-89*, pp. 1127-1130, May 1989.
- M. J. Irwin, R. M. Owens, Digit Serial Systolic VLSI Architectures, *Proc. of the Inter. Conf. on Systolic Arrays*, pp. 215-224, June 1989.
- P. Balsara, M. J. Irwin, Parallel Algorithms for Region Labeling on a Memory Array Architecture, *Proc. of the 1989 Conf. on Image Processing*, pp. 384-388, Sept. 1989.
- R. M. Owens, M. J. Irwin, The Arithmetic Cube: A Highly Parallel VLSI DSP Architecture, *Proc. of IFIP Workshop on Parallel Architectures on Silicon*, pp. 212-226, Dec. 1989.
- C-M Wu, R. M. Owens, M. J. Irwin, Distortion Processing in Image Matching Problems, *Proc. of ICASSP-90*, pp. 2181-2184, April 1990.
- M. J. Irwin, R. M. Owens, A Two-Dimensional Distributed Logic Processor for Vision Processing Algorithms, *Proc. of ICASSP-90*, pp. 945-948, April 1990.
- M. J. Irwin, R. M. Owens, A Case for Digit Serial VLSI Signal Processors, *The Journal of VLSI Signal Processing*, 1(4):321-334, Kluwer, April 1990.**
- R. M. Owens, M. J. Irwin, Being Stingy with Multipliers, *IEEE Trans. on Computers*, 39(6):809-818, June 1990.**
- C-M Wu, R. M. Owens, M. J. Irwin, Mapping High-Dimension Wavefront Computations to Silicon, *Proc. of Application Specific Array Processing Conf. (ASAP)*, pp. 78-89, Sept. 1990.
- R. M. Owens, M. J. Irwin, T. Kelliher, C-M Wu, The Design of the Arithmetic Cube II, in *VLSI Signal Processing, IV*, pp. 95-105, IEEE Press, Nov. 1990.
- P. Balsara, M. J. Irwin, R. M. Owens, Digit Serial Multipliers, *Journal of Parallel and Distributed Computing*, 11(2):156-162, Academic Press, Feb. 1991.**
- M. J. Irwin, R. M. Owens, T. Kelliher, K-K Leung, M. Vishwanath, The Arithmetic Cube II: A Second Generation VLSI DSP Processor, *Proc. of ICASSP-91*, pp. 1125-1128, May 1991.
- P. Balsara, M. J. Irwin, Image Processing on a Memory Array Architecture, *The Journal of VLSI Signal Processing*, 2(4):313-324, May 1991.**
- R. M. Owens, M. J. Irwin, Parallel uses for Serial Arithmetic in Signal Processors, *Proc. of SPIE Inter. Conf. on Advanced Signal Processing*, pp. 252-262, July 1991.
- M. Vishwanath, R. M. Owens, M. J. Irwin, The Arithmetic Cube: Error Analysis and Simulation, *Proc. of ASAP'91*, pp. 129-143, Sept. 1991.
- M. J. Irwin, R. M. Owens, A Two-Dimension, Distributed Logic Architecture, *IEEE Trans. on Computers*, 40(10):1094-1101, Oct. 1991.**
- M. Vishwanath, R. M. Owens, M. J. Irwin, ECube: An Efficient Architecture for Analyzing Time-Varying Spectra, *Proc. of VLSI'92*, pp. 221-226, Jan. 1992.
- M. J. Irwin, R. M. Owens, A Micro-Grained VLSI Signal Processor, *Proc. of ICASSP-92*, pp. 641-644, March 1992.
- M. Vishwanath, R. M. Owens, M. J. Irwin, Discrete Wavelet Transforms in VLSI, *Proc. of ASAP'92*, pp. 218-229, Aug. 1992.
- R. M. Owens, M. J. Irwin, T. Kelliher, M. Vishwanath, R. Bajwa, Implementing a Family of High Performance, Micrograined Architectures, *Proc. of ASAP'92*, pp. 191-205, Aug. 1992.
- M. Vishwanath, R. M. Owens, M. J. Irwin, The Computational Complexity of Time-Frequency Distributions, *Proc. of Signal Processing Workshop on Statistical and Array Processing*, pp. 444-446, Oct. 1992.
- M. Vishwanath, R. M. Owens, M. J. Irwin, An Efficient Systolic Architecture for QMF Filter Bank Trees, in *VLSI Signal Processing, V*, pp. 175-184, IEEE Press, 1992.
- R. M. Owens, M. J. Irwin, T. Kelliher, M. Vishwanath, R. Bajwa, Building a High Performance Signal Processing Architecture: ACII, *GOMAC-92 Digest*, pp. 97-100, Nov. 1992.

- R. Bajwa, R. M. Owens, M. J. Irwin, A Massively Parallel Micro-Grained VLSI, *Proc. of VLSI'93*, pp. 250-255, Jan. 1993.
- P. Balsara, M. J. Irwin, Intermediate-Level Vision Tasks on a Memory Array Architecture, *Machine Vision and Applications Journal*, 6(1):50-65, Springer-Verlag, Jan. 1993.**
- C. Nagendra, M. Borah, M. Vishwanath, R. M. Owens, M. J. Irwin, Edge Detection Using Fine-Grained Parallelism in VLSI, *Proc. of ICASSP-93*, pp. 401-404, April 1993. Also appeared in *Signal Processing Technology and Applications*, pp. 262-265, IEEE Technology Update Series, March 1995.
- T. Kelliher, M. J. Irwin, A Completely Systolic VLSI Architecture for Multi-Dimensional Transforms, *Proc. of ICASSP-93*, pp. 365-368, April 1993.
- C-M Wu, M. Vishwanath, R. M. Owens, M. J. Irwin, A New Blocked IIR Algorithm, *Proc. of ICASSP-93*, pp. 113-116, April 1993.
- R. Bajwa, R. M. Owens, M. J. Irwin, Image Processing with the MGAP: A Cost Effective Solution, *Proc. of Inter. Parallel Processing Symp. (IPPS)*, pp. 439-442, April 1993.
- C. Nagendra, R. M. Owens, M. J. Irwin, Digit Systolic Algorithms for Fine-Grain Architectures, *Proc. of ASAP'93*, pp. 466-477, Oct. 1993.
- R. M. Owens, M. J. Irwin, C. Nagendra, R. Bajwa, Computer Vision on the MGAP, *Proc. of Computer Architectures for Machine Perception (CAMP)*, pp. 337-341, Dec. 1993.
- R. M. Owens, T. Kelliher, M. J. Irwin, M. Vishwanath, R. Bajwa, W-L Yang, The Design and Implementation of the Arithmetic Cube II, A VLSI Signal Processing System, *IEEE Trans. on VLSI Systems*, 1(4):491-502, Dec. 1993.**
- M. Borah, C. Nagendra, R. M. Owens, M. J. Irwin, The MGAP: A High Performance, User Programmable, Multifunctional Architecture for DSP, *Proc. of HICSS-94*, pp. 96-104, Jan. 1994.
- C. Nagendra, M. J. Irwin, R. M. Owens, Digit Pipelined Discrete Wavelet Transforms, *Proc. of ICASSP-94*, pp. II-405-408, April 1994.
- H-N Kim, M. J. Irwin, R. M. Owens, C-M Wu, Dynamic Space Warping Algorithms on Fine-Grain Array Processors, *Proc. of IPPS'94*, pp. 921-925, April 1994.
- R. Bajwa, P. Keltcher, C. Nagendra, R. M. Owens, M. J. Irwin, Cost Effective Image and Signal Processing Using the MGAP, *Proc. of DSPx Exposition and Symp.*, pp. 504-516, June 1994.
- C. Nagendra, R. Bajwa, P. Keltcher, R. M. Owens, M. J. Irwin, Programming Micro-Grained Signal Processors Using C++, *Proc. of DSPx Exposition and Symp.*, pp. 575-584, June 1994.
- M. Borah, R. Bajwa, S. Hannenhalli, M. J. Irwin, An Efficient SIMD Solution to the Sequence Comparison Problem in Molecular Biology, *Proc. of ASAP'94*, pp. 336-345, Aug. 1994.
- R. Bajwa, C. Nagendra, P. Keltcher, M. J. Irwin, Rapid Prototyping with Programmable Control Paths, *Proc. of ASAP'94*, pp. 69-74, Aug. 1994.
- R. Bajwa, R. M. Owens, M. J. Irwin, Area Time Tradeoffs in Micro-Grained VLSI Array Architectures, *IEEE Trans. on Computers*, 43(10):1121-1128, Oct. 1994.**
- H-N Kim, M. Borah, M. J. Irwin, R. M. Owens, DCT on the MGAP for Data Compression, in *VLSI Signal Processing, VI*, pp. 356-367, Oct. 1994.
- R. Zhou, T. Kelliher, R. M. Owens, M. J. Irwin, Introducing the MGAP-2, *Proc. of Frontiers 1995*, pp. 281-288, Feb. 1995.
- R. Bajwa, R. Kasamsetty, R. M. Owens, M. J. Irwin, Experimental Studies of Fine Grain Reconfigurable Architectures, *Proc. of 1<sup>st</sup> Inter. Workshop on Parallel Processing*, pp. 575-579, Dec. 1994.
- C. Nagendra, R. M. Owens, M. J. Irwin, Digit Pipelined Arithmetic on Fine Grain Array Processors, *Journal of VLSI Signal Processing*, 9(3):193-209, April 1995.**
- T. Kelliher, E. Gayles, R. M. Owens, M. J. Irwin, The MGAP-2: An Advanced, Massively Parallel VLSI Signal Processor, *Proc. of ICASSP-95*, pp. 5:3219-3222, May 1995.
- M. Vishwanath, R. M. Owens, M. J. Irwin, VLSI Architectures for the Discrete Wavelet Transform, *IEEE Trans. on Circuits and Systems*, 42(5):305-316, May 1995.**
- R. M. Owens, M. J. Irwin, Reducing the Number of Counters Needed for Integer Multiplications, *Proc. of 12<sup>th</sup> ARITH*, pp. 38-41, July 1995.
- H-N Kim, M. J. Irwin, R. M. Owens, Motion Estimation Algorithms on Fine Grain Array Processors, *Proc. of ASAP'95*, pp. 204-213, July 1995.
- R. Bajwa, R. M. Owens, M. J. Irwin, The MGAP's Programming Environment and the \*C++ Language, *Proc. of ASAP'95*, pp. 121-124, July 1995.
- H-N Kim, M. J. Irwin, R. M. Owens, MGAP Applications in Machine Perception, *Proc. of CAMP'95*, pp. 67-73, Sept. 1995.

- E. Gayles, R. M. Owens, M. J. Irwin, The MGAP-2: A Micro-Grained Massively Parallel Array Processor, *Proc. of Application Specific Integrated Circuits (ASIC)*, pp. 333-337, Sept. 1995.
- P. Keltcher, M. J. Irwin, A Simulation Methodology for Evaluating Parallel Computers, *Proc. of Symp. of Parallel and Distributed Processing (SPDP)*, pp. 478-481, Oct. 1995.
- R. Bajwa, R. M. Owens, M. J. Irwin, Rapid Prototyping of Signal Processor in an Educational Environment, *Proc. of the 29<sup>th</sup> Asilomar Conf. on Signals, Systems, and Computers*, pp. 1321-1325, Nov. 1995.
- C. Nagendra, R. M. Owens, M. J. Irwin, Design Tradeoffs in High Speed Multipliers and FIR Filters, *Proc. of VLSI'96*, pp. 29-32, Jan 1996.
- C. Nagendra, M. J. Irwin, Design Tradeoffs in CMOS FIR Filters, *Proc. of ICASSP-96*, pp. 6:3261-3264, May 1996.
- K. Acken, H-N Kim, M. J. Irwin, R. M. Owens, An Architectural Design for Parallel Fractal Compression, *Proc. of ASAP'96*, pp.3-11, Aug. 1996.
- K. Acken, M. J. Irwin, R. M. Owens A. Garga, Architectural Optimizations for a Floating Point Multiply-Accumulate Unit in a Graphics Pipeline, *Proc. of ASAP'96*, pp. 65-71, Aug. 1996.
- C-M Wu, M. Vishwanath, R. M. Owens, M. J. Irwin, A New IIR Algorithm Based on the Overlap-Save Approach, *IEEE Trans. on Circuits and Systems*, 44(9):783-785, Sept. 1997.**
- M. Borah, C. Nagendra, M. Vishwanath, R. M. Owens, M. J. Irwin, An Optimal-Time Multiplication-Free Algorithm for Edge Detection on a Mesh, *Journal of VLSI Signal Processing*, 13(1):67-75, Aug. 1996.**
- K. Acken, E. Gayles, T. Kelliher, R. M. Owens, M. J. Irwin, The MGAP Family of Processor Arrays, *Proc. of Great Lakes Symposium on VLSI (GLS VLSI)*, pp. 105-110, March 1997.
- H-N Kim, M. J. Irwin, R. M. Owens, Motion Analysis on the MGAP Parallel Processor, *Journal of Real Time Imaging*, 3:101-110, June 1997.**
- B. Bishop, Y. Zhang, K. Acken, M. J. Irwin, R. M. Owens, Three Dimensional Graphics Algorithms on the Micro-Grain Array Processor-II, *Proc. of CAMP'97*, pp. 204-208, Oct. 1997.
- B. Bishop, R. M. Owens, M. J. Irwin, Aggressive Dynamic Execution of Decoded Traces, *Proc. of IEEE Workshop on Signal Processing Systems (SiPS)*, pp. 253-262, Nov. 1997.
- R. Bajwa, R. M. Owens, M. J. Irwin, Mixed-Autonomy Interconnect for Reconfigurable SIMD Arrays, *Proc. of Inter. Conf. on High Performance Computing (HiPC)*, pp. 428-431, Dec. 1997.
- B. Bishop, R. M. Owens, M. J. Irwin, Aggressive Dynamic Execution of Multimedia Kernel Traces, *Proc. of IPSP'98*, pp. 640-646, April 1998.
- K. Acken, M. J. Irwin, R. M. Owens, A Parallel ASIC Architecture for Efficient Fractal Image Coding, *Journal of VLSI Signal Processing*, 19(2): 97-114, July 1998.**
- B. Bishop, T. Kelliher, R. M. Owens, M. J. Irwin, Re-evaluating MPEG Motion Compensation Search Criteria, *Proc. of SiPS'98*, pp. 123-131, Oct. 1998.
- B. Bishop, T. Kelliher, M. J. Irwin, The Design of a Register Renaming Unit, *Proc. of GLS VLSI'99*, pp. 34-37, Mar. 1999.
- B. Bishop, T. Kelliher, R. M. Owens, M. J. Irwin, Aggressive Dynamic Execution of Decoded Traces, *Journal of VLSI Signal Processing*, 22(1):65-75, Aug. 1999.**
- B. Bishop, M. J. Irwin, A Detailed Analysis of Mediabench, *Proc. of SiPS'99*, pp. 448-455, Oct. 1999.
- B. Bishop, M. J. Irwin, T. Kelliher, SPARTA: Simulation of Physics on a Real-Time Architecture, *Proc. of GLS VLSI'2000*, pp. 177-182, Mar. 2000.
- B. Bishop, T. Kelliher, M. J. Irwin, Hardware/Software Co-design for Real-Time Physical Modelling, *Proc. of the IEEE Inter. Conf. on Multimedia and Expo*, pp. 3:1363-1366, Aug. 2000.
- E. Gayles, T. Kelliher, R. M. Owens, M. J. Irwin, The Design of the MGAP-2: A Micro-Grained Massively Parallel Array, *IEEE Trans. on VLSI Systems*, 8(6):709-716, Dec. 2000.**
- J. Lee, N. Vijaykrishnan, M. J. Irwin, R. Chandramouli, An Efficient Implementation of Hierarchical Image Coding, *Proc. of SIPS*, pp. 363-368, Aug. 2003.
- T. Theocharides, G. Link, N. Vijaykrishnan, M. J. Irwin, W. Wolf, Embedded Hardware Face Detection, *Proc. of VLSI Design*, pp. 133-138, Jan. 2004.
- J. Lee., N. Vijaykrishnan, M. J. Irwin, W. Wolf, An Architecture for Motion Estimation in the Transform Domain, *Proc. of VLSI Design*, pp. 1077-1083, Jan. 2004.
- T. Theocharides, G. Link, E. Swankoski, N. Vijaykrishnan, M. J. Irwin, H.Schmit, Evaluating Alternative Implementations for LDPC Decoder Check Node Function, *Proc. of ISVLSI'04*, pp. 77-82, Feb. 2004.
- E. Swankoski, R. Brooks, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, A Parallel Architecture for Secure FPGA Symmetric Encryption, *Proc. of the Reconfigurable Architectures Workshop (RAW)*, p. 132, Apr. 2004.
- J. Lee, N. Vijaykrishnan, M. J. Irwin, Efficient VLSI Implementation of Inverse Discrete Cosine Transform, *Proc. of ICASSP-04*, pp. 177-180, May 2004.

- T. Theocharides, G. Link, N. Vijaykrishnan, M. J. Irwin, V. Srikantam, A Generic Reconfigurable Neural Network Architecture Implemented as a Network on Chip, *Proc. of SoCC'04*, pp. 191-194, Sep. 2004.
- B. Kang, N. Vijaykrishnan, M. J. Irwin, T. Theocharides, Power-Efficient Implementation of Turbo Decoder in SDR Systems, *Proc. of SoCC'04*, pp. 119-122, Sep. 2004.
- J. Lee, N. Vijaykrishnan, M. J. Irwin, R. Radhakrishnan, Inverse Discrete Cosine Transform Architecture Exploiting Sparseness and Symmetry Properties, *Proc. of SIPS'04*, pp. 361-366, Oct. 2004.
- T. Theocharides, G. Link, N. Vijaykrishnan, M. J. Irwin, Implementing LDPC Decoding on Network-on-Chip, *Proc. of VLSI Design*, pp. 134-137, Jan. 2005.
- J. Lee, N. Vijaykrishnan, M. J. Irwin, High Performance Array Processor for Video Decoding, *Proc. of ISVLSI'05*, pp. 28-33, May 2005.
- E. Swankowski, N. Vijaykrishnan, R. Brooks, M. Kandemir, M. J. Irwin, Symmetric Encryption in Reconfigurable and Custom Hardware, *Inter. Journal of Embedded Systems*, 1(3/4):205-217, 2005.**
- J. Lee., N. Vijaykrishnan, M. J. Irwin, W. Wolf, An Efficient Architecture for Motion Estimation and Compensation in the Transform Domain, *IEEE Trans. on Circuits and Systems for Video Technology*, 16(2):191-201, Feb. 2006.**
- T. Theocharides, N. Vijaykrishnan, M. J. Irwin, A Parallel Architecture for Hardware Face Detection, *Proc. of ISVLSI'06*, Mar. 2006.
- J. Lee, N. Vijaykrishnan, M. J. Irwin, Efficient VLSI Implementation of Inverse Discrete Cosine Transform, *IEEE Trans. on Circuits and Systems for Video Technology*, 16(5):655-662, May 2006.**
- J. Lee, N. Vijaykrishnan, M. J. Irwin, Block-Based Frequency Scalable Technique for Efficient Hierarchical Coding, *IEEE Trans. on Signal Processing*, 54(7):2559-2566, July 2006.**
- T. Theocharides, C. Nicopoulos, K. Irick, N. Vijaykrishnan, M.J. Irwin, An Exploration of Hardware Architectures for Face Detection, *The VLSI Handbook, 2<sup>nd</sup> Edition*, Chapter 83, pp. 1-27, 2006.
- K. Irick, T. Theocharides, N. Vijaykrishnan, M. J. Irwin, Real Time Embedded Face Detection, *Proc. of the Asilomar Conf. on Signals, Systems, and Computers*, CDROM-6pps, Oct 2006.

*Due to the lack of tools to support their design efforts, in 1984 Drs. Irwin and Owens began a research effort to develop a suite of **architecture, logic, and circuit design tools** ranging from module layout (ARTIST and PERFLEX), to logic synthesis (LOGICIAN), to VHDL behavioral synthesis (DECOMPOSER). The tools were used to synthesize the custom CMOS parts for the Arithmetic Cube (from behavioral VHDL to layout) and portions of the MGAP architecture. The innovative approach to logic synthesis focused on minimizing communication complexity, the heuristics developed for performance driven custom module generation, and the routing algorithms developed for module generation based on an elegant Steiner routing heuristic (now referred to as the BOI algorithm) have all found their way into commercial products. Another outcome of this work was the discovery (by the communication complexity based logic synthesis program) of a new parallel prefix adder design (the ELM adder) that has superior energy-delay characteristics to other prefix adders that is reputed to be used in a number of commercial parts. Dr. Irwin's professional service in this area included membership on the Executive Committee of the annual Design Automation Conference (a conference with about 4,000 technical attendees and a large commercial exhibition) from 1990 to 2001, with Dr. Irwin serving as conference general chair in 1999. She also served for four years as the Editor-in-Chief of ACM's Transactions on the Design Automation of Electronic Systems (TODAES).*

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#### **Publications:**

- R. M. Owens, M. J. Irwin, Towards Designing, Testing, and Validating High Performance VLSI Signal Processors, *Proc. of Inter. Conf. On Computer Aided Design (ICCAD)*, pp. 94-96, Nov. 1985.
- R. M. Owens, M. J. Irwin, A System for Designing, Simulating, and Testing High Performance VLSI Signal Processors, *IEEE Trans. on CAD, CAD-5(3):420-428, July 1986.***
- D. Reeves, M. J. Irwin, Functional Verification of Digital MOS Circuits, *Proc. of ICCAD-86*, pp. 496-499, Nov. 1986.
- M. J. Irwin, R. M. Owens, Digit Pipelined Arithmetic as Illustrated by the Paste-Up System: A Tutorial, *IEEE Computer, 20(4):61-73, April 1987.***
- R. M. Owens, M. J. Irwin, An Overview of the Penn State Design System, *Proc. of 24th Design Automation Conf. (DAC)*, pp. 516-522, June 1987.
- J. Beekman, R. M. Owens, M. J. Irwin, Mesh Arrays and LOGICIAN: A Tool for Their Efficient Generation, *Proc. of 24th DAC*, pp. 516-522, June 1987.
- S. Rawat, M. J. Irwin, C-Testability of Unilateral and Bilateral Sequential Arrays, *Proc. of 1987 Inter. Test Conf.*, pp. 181-188, Sept. 1987.
- D. Reeves, M. J. Irwin, Fast Methods for Switch-Level Verification of MOS Circuits, *IEEE Trans. on CAD, CAD- 6(5):766-779, Sept. 1987.***
- R. M. Owens, C-S Fuh, M. J. Irwin, VLSI Layout Expectations, *IEEE VLSI Technical Bulletin*, 2(3):57-64, Sept. 1987.
- P-P Hou, R. M. Owens, M. J. Irwin, A High-Level Synthesis Tool for Systolic Designs, *Proc. of the Inter. Conf. on Systolic Arrays*, pp. 665-673, May 1988.
- P-P Hou, R. M. Owens, M. J. Irwin, DECOMPOSER: A Synthesizer for Systolic Systems, *Proc. of 25th DAC*, pp. 650- 653, June 1988.
- M. J. Irwin, R. Chen, Dynamic Circuit Synthesis Using the Owen's Tool Set, *Proc. of ASIC'98*, pp. 205-211, Sept. 1998.
- R. M. Owens, M. J. Irwin, A VLSI Design System for Signal Processors, in *VLSI Signal Processing, III*, Ed. R. Brodersen, H. Moscovitz, pp. 283-294, IEEE Press, 1988.
- J. Beekman, R. M. Owens, M. J. Irwin, A Rapid Turn-Around System for Designing Signal Processors, *Proc. of the Hawaii Inter. Conf. on System Science (HICSS)*, pp. 102-110, Jan. 1989.
- S. Levitan, R. M. Owens, M. J. Irwin, A VLSI CAD System for VHDL, *Proc. of the 1989 Colorado Microelectronics Conf.*, March 1989.
- S. Levitan, A. Martello, R. M. Owens, M. J. Irwin, Using VHDL as a Language for Synthesis of CMOS VLSI Circuits, *Proc. of the 1989 Symp. on Computer Hardware Description Languages (CHDL)*, pp. 331-346, June 1989.
- M. J. Irwin, R. M. Owens, A Comparison of Four Two-Dimensional Gate Matrix Layout Tools, *Proc. of 26th DAC*, pp. 698-701, June 1989.
- T-T Hwang, R. M. Owens, M. J. Irwin, Multi-Level Logic Synthesis Using Communication Complexity, *Proc. of 26th DAC*, pp. 215-220, June 1989.
- G. Lee, M. J. Irwin, R. M. Owens, Test Generation in Circuits Constructed by Input Decomposition, *Proc. of ICCD'90*, pp. 107-111, Sept. 1990.
- T-T Hwang, R. M. Owens, M. J. Irwin, Logic Synthesis for Programmable Logic Devices, *Proc. of ICCD'90*, pp. 364-367, Sept. 1990.
- T-T Hwang, R. M. Owens, M. J. Irwin, Exploiting Communication Complexity for Multi-Level Logic Synthesis, *IEEE Trans. on CAD, 9(10):1017-1027, Oct 1990.***
- P-P Hou, R. M. Owens, M. J. Irwin, Synthesizing Sequential Logic Modules From Behavioral VHDL, *Proc. of CHDL-91*, pp. 111-122, April 1991.
- S. Kim, M. J. Irwin, R. M. Owens, A Module Generator for High Performance CMOS Circuits, *Proc. of ISCAS'92*, pp. 1266-1269, May 1992.
- T-T Hwang, R. M. Owens, M. J. Irwin, Efficiently Computing Communication Complexity for Multi-Level Logic Synthesis, *IEEE Trans. on CAD, 11(5):545-554, May 1992.***

- S. Kim, M. J. Irwin, R. M. Owens, A Module Generator for High Performance CMOS Circuits, *Proc. of MCNC Workshop on Layout Synthesis*, pp. 245-253, May 1992.
- S. Kim, M. J. Irwin, R. M. Owens, Experiments with a Performance Driven Module Generator, *Proc. of 29th DAC*, pp. 687-690, June 1992.
- S. Kim, R. M. Owens, M. J. Irwin, PERFLEX: A Performance Driven Module Generator, *Proc. of European Design Automation Conf. (EuroDAC)*, pp. 154-159, Sept. 1992.
- T. Kelliher, R. M. Owens, M. J. Irwin, T-T Hwang, ELM - A Fast Addition Algorithm Discovered by a Program, *IEEE Trans. on Computers*, 41(9):1181-1184, Sept. 1992.**
- C-L Ding, C-Y Ho, M. J. Irwin, A New Optimization Driven Clustering Algorithm for Large Circuits, *Proc. of 4th Physical Design Workshop*, pp. 13-19, Apr. 1993.
- G. Lee, Y. Chang, T-T Hwang, M. J. Irwin, R. M. Owens, Synthesis of Multi-Level Reed Muller Circuits using Matrix Transformations, *Proc. of ICEIC'93*, pp. T159-T163, Aug. 1993.
- W-L Yang, R. M. Owens, M. J. Irwin, Multi-Way FSM Decomposition Based on Interconnect Complexity, *Proc. of EuroDAC'93*, pp. 390-395, Sept. 1993.
- G. Lee, H Hwang, M. J. Irwin, R. M. Owens, Testability of a Class of Multi-Level Reed Muller Circuit Transformations, *Proc. of IFIP Workshop on Applications of Reed Muller Expansions for Circuit Design*, pp. 34-41, Sept. 1993.
- G. Lee, J. Chang, T-T Hwang, M. J. Irwin, R. M. Owens, Synthesis of Multi-Level Reed Muller Circuits using Matrix Transformations, *Proc. of IFIP Workshop on Applications of Reed Muller Expansions for Circuit Design*, pp. 61-68, Sept. 1993.
- T. Kelliher, R. M. Owens, M. J. Irwin, Building High Performance Signal Processor Cheaply and Quickly, *Proc. of VLSI Signal Processing*, pp. 251-259, Oct. 1993.
- G. Lee, Y. Chang, T-T Hwang, M. J. Irwin, R. M. Owens, Logic Synthesis for Multi-Level Reed Muller Circuits using Matrix Transformations, *Proc. of ICVC'93*, pp. 193-196, Nov. 1993.
- G. Lee, M. J. Irwin, R. M. Owens, Polynomial Time Testability of Circuits Generated by Input Decomposition, *IEEE Trans. on Computers*, 43(2):201-210, Feb. 1994.**
- W. Yang, R. M. Owens, M. J. Irwin, FPGA-Based Synthesis of FSMs through Decomposition, *Proc. of GLS VLSI'94*, pp. 97-100, March 1994.
- T-T Hwang, R. M. Owens, M. J. Irwin, K. Wang, Logic Synthesis for FPGAs, *IEEE Trans. on CAD*, 13(10):1280-1287, Oct. 1994.**
- M. Borah, R. M. Owens, M. J. Irwin, An Edge-Based Heuristic for Steiner Routing, *IEEE Trans. on CAD*, 13(12):1563-1568, Dec. 1994.**
- M. Borah, R. M. Owens, M. J. Irwin, Fast Algorithms for Performance-Oriented Steiner Routing, *Proc. of GLS VLSI'95*, pp. 198-203, March 1995.
- W-L Yang, R. M. Owens, M. J. Irwin, Lower Bound Study on the Interconnect Complexity of the Decomposed Finite State Machines, *Journal of IEEE Proc. of Computer and Digital Techniques*, 142(5):332-336, Sept. 1995.**
- M. Borah, R. M. Owens, M. J. Irwin, Recent Developments in Performance Driven Steiner Routing, *Proc. of the GLS VLSI'96*, pp. 137-142, March 1996.
- M. Borah, R. M. Owens, M. J. Irwin, A Fast Routing Algorithm for Minimizing Elmore Delay to Identified Critical Sinks, *IEEE Trans. on CAD*, 16(6):753-759, July 1997.**
- M. Borah, R. M. Owens, M. J. Irwin, An Elegant Steiner Routing Heuristic, *Discrete Applied Mathematics*, 90(1999):51-67, 1999.**

*In late 1993, recognizing that energy consumption was fast becoming the next important design constraint, Dr. Irwin began a focused research effort in the area of **resource constrained systems design** including embedded systems that have limited battery life and limited memory space and sensor network systems that have extremely limited resources. She works with a team of researchers including Dr. Vijay Narayanan (N. Vijaykrishnan), Dr. Kandemir, and Dr. Xie. Their work has been supported by NSF, DARPA/MARCO/GSRC, PA/PDG, and industry. The uniqueness of their research is an holistic approach that spans the space from low power circuit design, to micro-architecture design, to system software design (compilers, operating systems, Java virtual machines), to application system design (databases, sparse matrix solvers) along with the design and implementation of the simulation tools necessary to support the design of resource constrained systems. Their architectural level power simulator, SimplePower, was made publicly available in November 2000 and has been distributed to over 200 sites worldwide. Dr. Irwin's professional service in the area includes continuing involvement in the annual International Low Power Symposium on Electronics and Design series, serving as program co-chair in 2001, as general co-chair in 2002, and on the*

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#### **Publications:**

- C. Nagendra, H. Mehta, R. M. Owens, M. J. Irwin, A Comparison of the Power-Delay Characteristics of CMOS Adders, *Proc. of Inter. Workshop on Low Power Design*, pp. 231-236, April 1994.
- C. Nagendra, R. M. Owens, M. J. Irwin, Power-Delay Characteristics of CMOS Adders, *IEEE Trans. on VLSI Systems*, 2(3):377-381, Sept. 1994. Also appeared in *High Performance Systems Design*, Ed. V. Oklobdzija, IEEE Press, July 1999.
- C. Nagendra, M. J. Irwin, R. M. Owens, Low Power Tradeoffs in Signal Processing Hardware Primitives, in *VLSI Signal Processing*, VI, pp. 276-285, Oct. 1994.
- M. Borah, M. J. Irwin, R. M. Owens, Minimizing Power Consumption of Static CMOS Circuits by Transistor Sizing and Input Reordering, *Proc. of VLSI'95*, pp. 294-298, Jan. 1995.
- C. Nagendra, R. M. Owens, M. J. Irwin, Unifying Carry-Sum and Signed-Digit Number Representations for Low Power, *Proc. of Inter. Symp. on Low Power Design (ISLPD)*, pp. 15-20, April 1995.
- M. Borah, R. M. Owens, M. J. Irwin, High-Throughput and Low-Power DSP Using Clocked-CMOS Circuitry, *Proc. of ISLPD'95*, pp. 139-144, April 1995.

- M. Borah, R. M. Owens, M. J. Irwin, Transistor Sizing for Minimizing Power Consumption of CMOS Circuits under Delay Constraints, *Proc. of ISLPD'95*, pp. 167-172, April 1995.
- H. Mehta, M. Borah, R. M. Owens, M. J. Irwin, Accurate Estimation of Combinational Switching Activity, *Proc. of 32<sup>nd</sup> DAC*, pp. 618-622, June 1995.
- H. Mehta, R. M. Owens, M. J. Irwin, Small Signal Model for Low Power DSP, *Proc. of the IEEE Symp. on Low Power Electronics*, pp. 28-29, Oct. 1995.
- C. Nagendra, R. M. Owens, M. J. Irwin, Low Power Considerations in the Design of Pipelined FIR Filters, *Proc. of the IEEE Symp. on Low Power Electronics*, pp. 32-33, Oct. 1995.
- H. Mehta, R. M. Owens, M. J. Irwin, Some Issues in Gray Code Addressing, *Proc. of the GLSVLSI'96*, pp. 178-181, March 1996.
- H. Mehta, R. M. Owens, M. J. Irwin, Instruction-Level Power Profiling, *Proc. of ICASSP'96*, pp. 6:3327-3330, May 1996.
- H. Mehta, R. M. Owens, M. J. Irwin, Energy Characterization Based on Clustering, *Proc. of 33<sup>rd</sup> DAC*, pp. 702-707, June 1996.
- M. Borah, R. M. Owens, M. J. Irwin, Transistor Sizing for Low Power CMOS Circuits, *IEEE Trans. on CAD*, 15(6):665- 571, June 1996.**
- K. Acken, M. J. Irwin, R. M. Owens, Power Comparisons for Barrel Shifters, *Proc. of the Inter. Symp. on Low Power Electronics and Design (ISLPED)*, pp. 209-214, Aug. 1996.
- E. Gayles, R. M. Owens, M. J. Irwin, Low Power Circuit Techniques for Fast Carry-Skip Adders, *Proc. of 1996 Midwest Symp. on Circuits and Systems*, pp. 87-90, Aug. 1996.
- E. Gayles, R. M. Owens, M. J. Irwin, A Fast Compact Addition Architecture for Low Power Microprocessors and DSP Chips, *Proc. of IEEE Inter. Conf. on VLSI Systems Solutions*, pp. 41-44, Sept. 1996.
- C. Nagendra, M. J. Irwin, R. M. Owens, Area Time Power Tradeoffs in Parallel Adders, *IEEE Trans. on Circuits and Systems*, 43(10):689-702, Oct. 1996.**
- H. Mehta, R. M. Owens, M. J. Irwin, A Simulation Methodology for Software Energy Evaluation, *Proc. of VLSI'97*, pp. 509-510, Jan. 1997.
- M-F Chang, M. J. Irwin, R. M. Owens, Power-Area Trade-Offs in Memory Arrays with Dual Word Lines, *Journal of Circuits, Systems, and Computers*, special issue on Applications of Low Power Design, 7(1):49-67, Feb. 1997.**
- E. Gayles, K. Acken, R. M. Owens, M. J. Irwin, A Clocked, Static Circuit Technique for Building Efficient High Frequency Pipelines, *Proc. of GLSVLSI'97*, pp. 182-187, March 1997.
- A. Kalambur, M. J. Irwin, An Extended Addressing Mode for Low Power, *Proc. of ISLPED'97*, pp. 208-213, Aug. 1997.
- H. Mehta, R. M. Owens, M. J. Irwin, Techniques for Low Energy Software, *Proc. of ISLPED'97*, pp. 72-75, Aug 1997.
- Y. Zhang, W. Ye, R. M. Owens, M. J. Irwin, The Power Analysis of Interconnects, *Proc. of ASIC'97*, pp. 25-29, Sept. 1997.
- E. Gayles, K. Acken, R. M. Owens, M. J. Irwin, A Robust CMOS Logic Technique for Building High Frequency Circuits with Efficient Pipelining, *Proc. of ASIC'97*, pp. 168-172, Sept. 1997.
- J. Sacha, M. J. Irwin, Number Representations for Reduced Switched Capacitance in Subband Coding, *Proc. of ICASSP'98*, May 1998.
- R. Chen, M. J. Irwin, R. M. Owens, R. Bajwa, Validation of an Architectural Level Power Analysis Technique, *Proc. of 35<sup>th</sup> DAC*, pp. 242-245, June 1998.
- R. Chen, M. J. Irwin, R. Bajwa, An Architectural Level Power Estimator, *Proc. of the Power-Driven Microarchitecture Workshop*, held in conjunction with ISCA'98, pp. 87-91, June 1998.
- J. Sacha, M. J. Irwin, The Logarithmic Number System for Strength Reduction in Adaptive Filtering, *Proc. of ISLPED'98*, pp. 256-261, Aug 1998.
- R. Chen, M. J. Irwin, R. Bajwa, Architectural Level Hierarchical Power Estimation of Control, *Proc. of ASIC'98*, pp. 211-215, Sept. 1998.
- Y. Zhang, W. Ye, R. Chen, M. J. Irwin, System Level Interconnect Power Modeling, *Proc. of ASIC'98*, pp. 289-293, Sept. 1998.
- J. Sacha, M. J. Irwin, Input Recoding for Reducing Power in Distributed Arithmetic, *Proc. of SiPS'98*, pp. 599-608, Oct. 1998.
- J. Sacha, M. J. Irwin, Number Representations for Reducing Data Bus Power Dissipation, *Proc. of 32<sup>nd</sup> Asilomar Conf. on Signals, Systems, and Computers*, pp. 213-217, Nov. 1998.

- Y. Zhang, W. Ye, M. J. Irwin, An Alternative Architecture for On Chip Global Interconnect: Segmented Bus Power Modeling, *Proc. of 32<sup>nd</sup> Asilomar Conf. on Signals, Systems, and Computers*, pp. 1062-1065, Nov. 1998.
- Y. Zhang, M. J. Irwin, Energy-Delay Analysis for On-Chip Interconnect at the System Level, *Proc. of Workshop on VLSI (WVLSI)*, pp. 26-31, Apr. 1999.
- R. Chen, N. Vijaykrishnan, M. J. Irwin, Clock Power Issues in Systems-on-a-Chip Designs, *Proc. of WVLSI'99*, pp. 48-53, Apr. 1999.
- M. J. Irwin, N. Vijaykrishnan, A Transition Sensitive, Architectural Level Power Analysis Approach, *IEEE Computer Society TCVLSI Technical Bulletin*, pp. 6-11, Summer 1999.
- B. Bishop, M. J. Irwin, Databus Charge Recovery: Practical Considerations, *Proc. of ISLPED'99*, pp. 85-87, Aug. 1999.
- Y. Wu, M. J. Irwin, Power Analysis of Gated Pipeline Registers, *Proc. of ASIC'99*, pp. 281-285, Sept. 1999.
- M. J. Irwin, N. Vijaykrishnan, Energy Issues in Multimedia Systems, Invited, *Proc. of SiPS'99*, pp. 24-33, Oct. 1999.
- W. Ye, K. Li, M. Cheng, M. J. Irwin, Power Characterization of Functional Units, *Proc. of 33<sup>rd</sup> Asilomar Conf. on Signals, Systems, and Computers*, Oct. 1999.
- Y. Zhang, M. J. Irwin, Power and Performance Characteristics of Crossbars and Buses in On-Chip Interconnect Structures, *Proc. of 33<sup>rd</sup> Asilomar Conf. on Signals, Systems, and Computers*, Oct. 1999.
- J. Hezavei, N. Vijaykrishnan, M. J. Irwin, A Comparative Study of Power Efficient SRAM Designs, *Proc. of GLSVLSI'00*, pp. 117-122, Mar. 2000.
- H.S Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Multiple Access Caches: Energy Implications, *Proc. of the WVLSI'00*, pp. 37-42, Apr. 2000.
- A. Parikh, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Instruction Scheduling Based on Energy and Performance Constraints, *Proc. of WVLSI'00*, pp. 53-58, Apr. 2000.
- M. Kandemir, N. Vijaykrishnan, M. J. Irwin, W. Ye, Influences of Compiler Optimizations on System Power, *Proc. of 37<sup>th</sup> DAC*, pp. 304-307, June 2000.
- W. Ye, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, The Design and Use of SimplePower: A Cycle-Accurate Energy Estimation Tool, *Proc. of 37<sup>th</sup> DAC*, pp. 340-345, June 2000.
- N. Vijaykrishnan, M. Kandemir, M. J. Irwin, H.S. Kim, W. Ye, Energy-Driven Integrated Hardware-Software Optimization Using SimplePower, *Proc. of 27<sup>th</sup> ISCA*, pp. 95-106, June 2000.
- M. Kandemir, N. Vijaykrishnan, M. J. Irwin, H.S. Kim, Towards Energy Aware Iteration Space Tiling, *Proc. of ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, p. 108, June 2000. Also appeared in Springer-Verlag Lecture Notes in Computer Science (LNCS) 1985, pp. 211-215, 2001.
- G. Esakkimuthu, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Memory System Energy: Influence of Hardware-Software Optimizations, *Proc. of ISLPED'00*, pp. 244-246, July 2000.
- M. Kandemir, N. Vijaykrishnan, M. J. Irwin, H.S. Kim, Experimental Evaluation of Energy Behavior of Iteration Space Tiling, *Proc. of the 13<sup>th</sup> Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, To appear in Springer-Verlag LNCS, Aug. 2000.
- D. Duarte, M. J. Irwin, N. Vijaykrishnan, Modeling Energy of the Clock Generation and Distribution Circuitry, *Proc. of ASIC'00*, pp. 261-265, Sep. 2000.
- V. Lyuboslavsky, B. Bishop, N. Vijaykrishnan, M. J. Irwin, Design of Databus Charge Recovery Mechanisms, *Proc. of ASIC'00*, pp. 283-287, Sep. 2000.
- M. J. Irwin, M. Kandemir, N. Vijaykrishnan, A. Sivasubramaniam, A Holistic Approach to System Level Energy Optimization, Invited, *Proc. of the 10<sup>th</sup> Inter. Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, Ed. D. Soudris, P. Pirsch, E. Barke, Springer-Verlag LNCS, 1918:88-107, Sep. 2000.
- M. Kandemir, N. Vijaykrishnan, M. J. Irwin, W. Ye, I. Demirkiran, Register Relabeling: A Post Compilation Technique for Energy Reduction, *Proc. of the Workshop on Compilers and Operating Systems for Low Power (COLP)*, Oct. 2000.
- H.S. Kim, M. J. Irwin, N. Vijaykrishnan, M. Kandemir, Effect of Compiler Optimizations on Memory Energy, *Proc. of SiPS'00*, pp. 663-672, Oct. 2000.
- V. Delaluz, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Energy-Oriented Compiler Optimizations for Partitioned Memory Architectures, *Proc. of the 3<sup>rd</sup> Inter. Conf. on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pp. 138-147, Nov. 2000.
- A. Parikh, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Energy-Aware Instruction Scheduling, *Proc. of HiPC'2000*, Springer-Verlag LNCS 1970:335-344, Dec. 2000.
- V. Delaluz, M. Kandemir, N. Vijaykrishnan, A. Sivasubramaniam, M. J. Irwin, DRAM Energy Management Using Software and Hardware Directed Power Mode Control, *Proc. of the 7<sup>th</sup> Inter. Symp. on High Performance Computer Architecture (HPCA)*, pp. 159-169, Jan. 2001.

- R. Chen, M. J. Irwin, R. Bajwa, Architecture Level Power Estimation and Design Experiments, *ACM Trans. on Design Automation of Electronic Systems*, 6(1):50-66, Jan. 2001.**
- B. Bishop, V. Lyuboslavsky, N. Vijaykrishnan, M. J. Irwin, Design Considerations for Databus Charge Recovery, *IEEE Trans. on VLSI Systems*, 9(1):104-106, Jan. 2001.**
- D. Duarte, N. Vijaykrishnan, M. J. Irwin, M. Kandemir, Formulation and Validation of an Energy Dissipation Model for the Clock Generation Circuitry and Distribution Networks, *Proc. of VLSI Design*, pp. 248-253, Jan. 2001.
- G. Esakkimuthu, H.S. Kim, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Investigating Memory System Energy Behavior Using Software and Hardware Optimizations, *VLSI Design Journal*, 12(2):151-165, Feb. 2001.**
- N. Vijaykrishnan, N., M. Kandemir, S.T. Kim, S. Tomar, A. Sivasubramaniam, M. J. Irwin, Energy Behavior of Java Applications from the Memory Perspective, *Proc. of the Java Virtual Machine Research & Technology Symposium (JVM)*, pp. 207-220, Apr. 2001.
- R. Athavale, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Influence of Array Allocation Mechanisms on Memory System Energy, *Proc. of the 15<sup>th</sup> International Parallel and Distributed Processing Symposium (IPDPS)*, p. 3 (full paper on CD-ROM), Apr. 2001.
- A. Parikh, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, VLIW Scheduling for Energy and Performance, *Proc. of WVLSI*, pp. 111-117, Apr. 2001.
- S. Tomar, N. Vijaykrishnan, M. Kandemir, R. Shetty, M. J. Irwin, Energy Optimization Using Object Co-Location in Java, *Proc. of Java Optimization Strategies for Embedded Systems Workshop (JOSES)*, held in conjunction with ETAPS'2001, pp. 9-15, Apr. 2001.
- H.S. Kim, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Characterization of Memory Energy Behavior, in *Characterization of Contemporary Workloads*, pp. 165-180, Ed. John and Grizzaffi-Maynard, Kluwer, May 2001.
- P. Khosla, H. Schmit, T. Cain, S. Levitain, M. J. Irwin, N. Vijaykrishnan, D. Landis, SoC Design Skills: Collaboration Builds a Stronger SoC Design Team, *Proc. of the 2001 Inter. Conf. on Microelectronic Systems Education (MSE)*, pp. 42-43, June 2001.
- M. Kandemir, J. Ramanujam, M. J. Irwin, V. Narayanan, I. Kadayif, A. Parikh, Dynamic Management of Scratch-pad Memory Space, *Proc. of 38<sup>th</sup> DAC*, pp. 690-695, June 2001.
- I. Kadayif, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, J. Ramanujam, Morphable Cache Architectures: Potential Benefits, *Proc. of LCTES'2001*, pp. 128-137, June 2001.
- I. Kadayif, T. Chinoda, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, A. Sivasubramaniam, vEC: Virtual Energy Counters, *Proc. ACM Workshop on Program Analysis for Software Tools and Engineering (PASTE)*, pp. 28-31, June 2001.
- A. Parikh, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, and I. Kadayif. Energy-Conscious Instruction Scheduling for VLIW Architectures, *Proc. of the 9<sup>th</sup> Workshop on Compilers for Parallel Computers (CPC)*, pp. 303-312, June 2001.
- S.T. Kim, N. Vijaykrishnan, M. Kandemir, A. Sivasubramaniam, M. J. Irwin, E. Geethanjali, Power-aware Partitioned Cache Architectures, *Proc. of ISLPED'01*, pp. 64-67, Aug. 2001.
- N. An, A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, S. Gurumurti, Analyzing Energy Behavior of Spatial Access Methods for Memory-Resident Data, *Proc. of the Inter. Conf. on Very Large Databases*, pp. 411-420, Sep. 2001.
- G. Thirugnanam, N. Vijaykrishnan, M. J. Irwin, A Novel Low Power CAM Design, *Proc. of ASIC'01*, Sep. 2001.
- D. Duarte, N. Vijaykrishnan, M. J. Irwin, M. Kandemir, Evaluating the Impact of Architectural-Level Optimizations on Clock Power, *Proc. of ASIC'01*, Sep. 2001.
- H.S. Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, A Framework for Exploring Energy-Efficient VLIW Architectures, *Proc. of ICCD'01*, pp. 40-45, Sep. 2001.
- S. Tomar, S.T. Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Use of Local Memory for Efficient Java Execution, *Proc. of ICCD'01*, pp. 468-473, Sep. 2001.
- J. Hezavei, N. Vijaykrishnan, M. J. Irwin, M. Kandemir, Input Sensitive High-Level Power Analysis, *Proc. of SiPS'01*, pp. 149-156, Sep. 2001.
- V. Delaluz, M. Kandemir, N. Vijaykrishnan, A. Sivasubramaniam, M. J. Irwin, Hardware and Software Techniques for Controlling DRAM Power Modes, *IEEE Trans. on Computers*, 50(11):1154-1173, Nov. 2001.**
- S. Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Energy-Efficient Instruction Cache Using Page-Based Placement, *Proc. of CASES 01*, pp. 229-237, Nov. 2001.
- W. Zhang, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, D. Duarte, Y. Tsai, Exploiting VLIW Schedule Slacks for Dynamic and Leakage Energy Reduction, *Proc. of the 34<sup>th</sup> Inter. Sym., on Microarchitecture (MICRO-34)*, pp. 102-113, Dec. 2001.

- N. Kirubanandan, A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Memory Energy Characterization and Optimization for the SPEC2000 Benchmarks, *Proc. of the IEEE 4<sup>th</sup> Workshop on Workload Characterization (WWC)*, held in conjunction with *MICRO-34*, pp. 193-201, Dec. 2001.
- M. Kandemir, N. Vijaykrishnan, M. J. Irwin, W. Ye, Influence of Compiler Optimizations on System Power, *IEEE Trans. on VLSI Systems*, 9(6):801-804, Dec. 2001.**
- V. Delaluz, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, A. Sivasubramaniam, I. Kolcu, Compiler-Directed Array Interleaving for Reducing Energy in Multi-Bank Memories, *Proc. of the Seventh Asia and South Pacific Design Automation Conf. (ASP-DAC) and VLSI'02*, pp. 288-293, Jan. 2002.
- D. Duarte, Y-F. Tsai, N. Vijaykrishnan, M. J. Irwin, Evaluating Run-Time Techniques for Leakage Power Reduction, *Proc. of ASP-DAC '02 and VLSI'02*, pp. 31-38, Jan. 2002.
- G. Chen, R. Shetty, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, M. Wolczko, Tuning Garbage Collection in an Embedded Java Environment, *Proc. of HPCA-8*, pp. 92-103, Feb. 2002.
- S. Gurumurthi, A. Sivasubramaniam, M. J. Irwin, N. Vijaykrishnan, M. Kandemir, T. Li, L. K. John, Using Complete Machine Simulation for Software Power Estimation: The SoftWatt Approach, *Proc. of HPCA-8*, pp. 141-150, Feb. 2002.
- I. Kadayif, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, A. Sivasubramaniam, EAC: A Compiler Framework for High-Level Energy Estimation and Optimization, *Proc. of the Inter. Conf. on Design Automation and Test in Europe (DATE)*, pp. 436-442, Mar. 2002.
- J. Hu, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Power-Efficient Trace Caches, *Proc. of DATE'02*, p. 1091, Mar. 2002.
- D. Duarte, N. Vijaykrishnan, M. J. Irwin, A Complete Phase-Locked Loop Power Consumption Model, *Proc. of DATE'02*, p. 1108, Mar. 2002.
- I. Kadayif, N. Orr, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Instruction Selection/Scheduling Using an Energy-aware Instruction Set Architecture, *Proc. of 6<sup>th</sup> Workshop of Languages, Compilers, and Runtime Systems for Scalable Computers (LCR)*, pp. 1-10, Mar. 2002.
- A. Sivasubramaniam, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Designing Energy-Efficient Software, *Proc. of the Next Generation Software Workshop*, held in conjunction with IPDPS, p. 176, April 2002.
- D. Duarte, N. Vijaykrishnan, M. J. Irwin, Y-F Tsai, Impact of Technology Scaling on the Clock System Power, *Proc. of the IEEE Inter. Symp. on VLSI (ISVLSI)*, pp. 59-64, Apr. 2002.
- I. Kadayif, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Hardware-Software Co-Adaption for Data-Intensive Embedded Applications, *Proc. of ISVLSI'02*, pp. 20-25, Apr. 2002.
- B-T Kang, N. Vijaykrishnan, M. J. Irwin, R. Chandramouli, Power Efficient Adaptive M-QAM Design Using Adaptive Pipelined Analog-to-Digital Converter, *Proc. of ICASSP'02*, (CD ROM), May 2002.
- G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, W. Wolf, Energy Savings Through Compression in Embedded Java Environments, *Proc. of 10<sup>th</sup> Inter. Conf. on Hardware/Software Codesign (CODES)*, pp. 163-168, May 2002.
- H. Saputra, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, J. S. Hu, C-H. Hsu, U. Kremer, Energy-Conscious Compilation Based on Voltage Scaling, *Proc. of LCTES'02 and Software and Compilers for Embedded Systems (SCOPE5)*, pp. 2-10, June 2002.
- J. Hu, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, H. Saputra, W. Zhang, Compiler-Directed Cache Polymorphism, *Proc. of LCTES'02 and SCOPE5'02*, pp. 165-174, June 2002.
- V. Delaluz, A. Sivasubramaniam, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Scheduler-Based DRAM Energy Management, *Proc. of 39<sup>th</sup> DAC*, pp. 697-702, June 2002.
- G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, M. Wolczko, Adaptive Garbage Collection for Battery-Operated Environments, *Proc. of 2<sup>nd</sup> JVM Conf.*, pp. 1-12, Aug. 2002.
- D. Duarte, N. Vijaykrishnan, M. J. Irwin, H. Kim, G. McFarland, Scaling of the Effectiveness of Power Reduction Schemes and the Impact of Temperature Management, *Proc. of ICCD'02*, pp. 382-387, Sep. 2002.
- L. Lin, I. Kadayif, Y-F. Tsai, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, A. Sivasubramaniam, Leakage Energy Management in Cache Hierarchies. *Proc. of 11<sup>th</sup> Inter. Conf. on Parallel Architectures and Compilation Techniques (PACT)*, pp. 131-140, Sep. 2002.
- S. Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Predictive Precharging for Bitline Leakage Energy Reduction. *Proc. of ASIC'02*, pp. 36-40, Sep. 2002.
- D. Duarte, N. Vijaykrishnan, M. J. Irwin, Impact of Technology Scaling and Packaging on Dynamic Voltage Scaling Techniques, *Proc. of ASIC'02*, pp. 244-248, Sep. 2002.
- R. Ramanarayanan, N. Vijaykrishnan, M. J. Irwin, Characterizing Dynamic and Leakage Power Behavior in Flip-Flops, *Proc. of ASIC'02*, pp. 433-437, Sep. 2002.

- G. Essakimuthu, N. Vijaykrishnan, M. J. Irwin, An Analytical Power Estimation Model for Crossbar Interconnects, *Proc. of ASIC'02*, pp.119-123, Sep. 2002.
- J. Zhao, R. Chandramouli, N. Vijaykrishnan, M. J. Irwin, B. Kang, S. Somasundaram, Influence of MPEG-4 Parameters on System Energy, *Proc. of ASIC'02*, pp. 137-142, Sep. 2002.
- W. Xu, A. Parikh, M. Kandemir, M. J. Irwin, Fine-Grain Instruction Scheduling for Low Energy, *Proc. of SiPS'02*, pp. 258-263, Oct. 2002.
- M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Compiler Optimizations for Low-Power Systems, in *Power Aware Computing*, Ed. by Graybill and Melhem, pp. 191-210, Kluwer, 2002.
- N. Vijaykrishnan, M. Kandemir, A. Sivasubramaniam, M. J. Irwin, Tools and Techniques for Integrated Hardware-Software Energy Optimizations, in *Power Aware Design Methodologies*, Ed. by Rabaey and Pedram, pp. 277-295, Kluwer, 2002.
- W. Zhang, J. Hu, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Compiler-directed Instruction Cache Leakage Optimization, *Proc. of MICRO-35*, pp. 208-218, Nov. 2002.
- G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, W. Wolf, Using Memory Compression for Energy Reduction in an Embedded Java System, *Journal of Circuits, Systems and Computers*, 11(5):537-556, Oct. 2002.**
- G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, M. Wolczko, Tuning Garbage Collection for Reducing Memory System Energy in an Embedded Java Environment, *ACM Trans. on Embedded Computer Systems*, 1(1):27-55, Nov. 2002.**
- G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, PennBench: A Benchmark Suite for Embedded Java, *Proc. of the 5<sup>th</sup> IEEE Workshop on Workload Characterization (WWC'02)*, Nov. 2002.
- N. An, S. Gurumurthi, A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Energy-Performance Trade-Offs for Spatial Access Methods on Memory-Resident Data, *Inter, Inter. Journal on Very Large Databases*, 11(3):179-197, Dec. 2002.
- D. Duarte, N. Vijaykrishnan, M. J. Irwin, A Clock Power Model to Evaluate Impact of Architectural and Technology Optimizations, *IEEE Trans. on VLSI Systems*, 10(6):844-855, Dec. 2002. IEEE/CAS Best Paper Award Winner.**
- N. Vijaykrishnan, M. Kandemir, M. J. Irwin, H. Kim, W. Ye, Evaluating Integrated Hardware-Software Optimizations Using a Unified Energy Estimation Framework, *IEEE Trans. on Computers*, 52(1):59-76, Jan. 2003.**
- J. Hu, N. Vijaykrishnan, M. J. Irwin, M. Kandemir, Using Dynamic Branch Behavior for Power-Efficient Instruction Fetch, *Proc. ISVLSI'03*, pp. 127-132, Feb. 2003.
- L. Li, I. Kadayif, Y-F Tsai, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, A. Sivasubramaniam, Managing Leakage Energy in Cache Hierarchies, *Journal of Instruction-Level Parallelism*, Vol. 5, Feb. 2003.**
- S. Gurumurthi, J. Zhang, A. Sivasubramaniam, M. Kandemir, H. Franke, N. Vijaykrishnan, M. J. Irwin, Interplay of Energy and Performance for Disk Arrays Running Transaction Processing Workloads, *Proc. of the Inter. Symp. on Performance Analysis of Systems and Software (ISPASS)*, pp. 123-132, Mar. 2003.
- H. Saputra, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, R. Brooks, S. Kim, W. Zhang, Masking the Energy Behavior of DES Encryption, *Proc. of DATE'03*, pp. 10084-10089, Mar. 2003.
- W. Zhang, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, V. De, Compiler Support for Reducing Leakage Energy Consumption, *Proc. of DATE'03*, pp. 11146-11147, Mar. 2003.
- M. Kandemir, M. J. Irwin, G. Chen, J. Ramanujam, Address Register Assignment for Reducing Code Size, *Proc. of 12<sup>th</sup> Inter. Conf. on Compiler Construction (CC)*, Springer-Verlag LNCS 2622:273-289, Apr. 2003.
- S. Gurumurthi, N. An, A. Sivasubramaniam, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Energy and Performance Considerations in Work Partitioning for Mobile Spatial Queries, *Proc. of the IPDPS'03*, CD-ROM, Apr. 2003.
- G. Chen, B. T. Kang, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, R. Chandramouli, Energy-Aware Compilation and Execution in Java-Enabled Mobile Devices, *Proc. of IPDPS'03*, (CD-ROM), Apr. 2003.
- S. Kim, N. Vijaykrishnan, M. Kandemir, A. Sivasubramaniam, M. J. Irwin, Partitioned Instruction Cache Architecture For Energy Efficiency, *ACM Trans. on Embedded Computing Systems*, 2(2):163-185, May 2003.**
- Y-F Tsai, D. Duarte, N. Vijaykrishnan, M. J. Irwin, Implications of Technology Scaling on Leakage Reduction Techniques, *Proc. of 40<sup>th</sup> DAC*, pp. 187-190, June 2003.
- H. S. Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Adapting Instruction Level Parallelism for Optimizing Leakage in VLIW Architectures, *Proc. of LCTES'03*, pp. 275-283, June 2003.
- A. Bhatkar, R. Chandramouli, N. Vijaykrishnan, M. J. Irwin, Computation and Transmission Energy Modeling Through Profiling For MPEG4 Video Transmission, *Proc. IEEE Inter. Conf. on Multimedia & Expo*, pp. 281-284, July 2003.

- H. S. Kim, N. Vijaykrishnan, M. Kandemir, E. Brockmeyer, F. Catthoor, M. J. Irwin, Estimating Influence of Data Layout Optimizations on SDRAM Energy Consumption, *Proc. of ISLPED'03*, pp. 40-43, Aug. 2003.
- S. Kim, N. Vijaykrishnan, M. J. Irwin, L. K. John, On Load Latency in Low-Power Caches, *Proc. of ISLPED'03*, pp. 258-261, Aug. 2003.
- J. Hu, A. Nadgir, N. Vijaykrishnan, M. J. Irwin, M. Kandemir, Exploiting Program Hotspots and Code Sequentiality for Instruction Cache Leakage Management, *Proc. of ISLPED'03*, pp. 402-407, Aug. 2003.
- E. J. Kim, K. H. Yum, G. M. Link, C. R. Das, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Energy Optimization Techniques in Cluster Interconnects, *Proc. of ISLPED'03*, pp. 459-464, Aug. 2003.
- H. Saputra, N. Vijaykrishnan, M. Kandemir, R. Brooks, M.J Irwin, Exploiting Value Locality for Secure-Energy Aware Communication, *Proc. of SIPS'03*, pp. 116-121, Aug. 2003.
- H. Saputra, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, R. Brooks, S. Kim, W. Zhang, Masking the Energy Behavior of Encryption Algorithms, *IEEE Proceedings: Computers and Digital Techniques*, 150(5):274-284, Sep. 2003. Invited among best papers at DATE 2003.**
- V. Delaluz, M. Kandemir, A. Sivasubramaniam, M.J. Irwin, N. Vijaykrishnan, Reducing dTLB Energy Through Dynamic Resizing, *Proc. of ICCD'03*, Sep. 2003.
- L. Li, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, I. Kadayif, CCC: Crossbar Connected Caches for Reducing Energy Consumption of On-Chip Multiprocessors, *Proc. of EUROMICRO Symp. on Digital System Design, Architectures, Methods and Tools (DSD'03)*, pp. 41-48, Sep. 2003.
- G. Chen, Guangyu Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Energy-Aware Code Cache Management for Memory-Constrained Java Devices, *Proc. of Inter. SOC Conf. (ASIC/SOC)*, pp. 179-182, Sep. 2003.
- D. Duarte, N. Vijaykrishnan, M. J. Irwin, Energy and Timing Characterization of VLSI Charge-pump Phase-locked Loops, *Proc. of ASIC/SOC'03*, pp. 341-344, Sep. 2003.
- A. Hegde, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Variable Line Sized Cached DRAMs, *Proc. of ISSS/CODES'03*, pp. 132-137, Oct. 2003.
- G. Chen, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, M. Wolczko, Tracking object life cycle for leakage energy optimization, *Proc. of ISSS/CODES'03*, pp. 213-218, Oct. 2003.
- V. De La Luz, M. Kandemir, G. Chen, M. J. Irwin, I. Kolcu, Energy-conscious Memory Allocation and Deallocation for Pointer-intensive Applications, *Proc. of the Third Inter. Conf. on Embedded Software (EMSOFT'03)*, pp. 156-172, Oct 2003.
- V. De La Luz, A. Sivasubramaniam, M. Kandemir, M. J. Irwin, N. Vijaykrishnan, Reducing dTLB Energy Through Dynamic Resizing, *Proc. of ICCD'03*, pp. 358-363, Oct. 2003.
- G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, B. Mathiske, M. Wolczko, Heap Compression for Memory-constrained Java Environments, *Proc. of the 18<sup>th</sup> Annual ACM Conf. on Object-Oriented Programming, Systems, Languages, and Applications (OOPSLA)*, pp. 282-301, Oct. 2003.
- U. Sezer, G. Chen, M. Kandemir, H. Saputra, M. J. Irwin, Exploiting Bank Locality in Multi-bank Memories, *Proc. of CASES '03*, pp. 287-297, Oct. 2003.
- N. Kim, T. Austin, D. Blaauw, T. Mudge, K. Flautner, J. S. Hu, M. J. Irwin, M. Kandemir, N. Vijaykrishnan, Leakage Current: Moore's Law Meets Static Power, *IEEE Computer, Special Issue on Power and Temperature-Aware Computing*, 36(12):68-75, Dec. 2003.**
- S. Kim, S. Tomar, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Energy-Efficient Java Execution Using Local Memory and Object Co-location, *IEEE Proceedings: Computers and Digital Techniques*, 151(1):33-42, Jan. 2004.**
- M. Derenzo, M. J. Irwin, N. Vijaykrishnan, Designing Leakage-Aware Multipliers, *Proc. of VLSI Design*, pp. 654-657, Jan. 2004.
- J. Hu, N. Vijaykrishnan, M. J. Irwin, Exploring Wakeup-Free Instruction Scheduling, *Proc. of HPCA-10*, pp. 232-243, Feb. 2004.
- J. Hu, N. Vijaykrishnan, S. Kim, M. Kandemir, M. J. Irwin, Scheduling Reusable Instructions for Power Reduction, *Proc. of DATE'04*, pp. 148-153, Feb. 2004.
- A. Gayasen, Y. Tsai, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, T. Tuan, Reducing Leakage Energy in FPGAs Using Region-constrained Placement, *Proc. of the ACM Inter. Symp. on Field-Programmable Gate Arrays (FPGA)*, pp. 51-58, Feb. 2004.
- M. Kandemir, J. Ramanujam, M. J. Irwin, N. Vijaykrishnan, I. Kadayif, A. Parikh, A Compiler Based Approach for Dynamically Managing Scratch-pad Memories in Embedded Systems, *IEEE Trans. on CAD*, 23(2): 243-260, Feb. 2004.**

- W. Zhang, J. Hu, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Reducing Instruction Cache Energy Consumption using a Compiler-Based Strategy, *ACM Trans. on Architecture and Code Optimizatio (TACO)*, 1(1):3-33, Mar. 2004.
- A. Parikh, S. Kim, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Instruction Scheduling for Low Power, *Journal of VLSI Signal Processing Systems*, 37(1):129-150, May 2004.
- Y-F. Tsai, D. Duarte, N. Vijaykrishnan, M.J. Irwin, Impact of Process Scaling on the Efficacy of Leakage Reduction Scheme, *Proc. of Inter. Conf. on IC Design and Technology*, pp. 3-11, May 2004.
- O. Ozturk, M. Kandemir, I. Demirkiran, G. Chen, M. J. Irwin, Data Compression for Improving SPM Behavior, *Proc. of 32<sup>nd</sup> DAC*, pp. 401-406, Jun. 2004.
- H. Saputra, G. Chen, R. Brooks, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Code Protection for Resource-constrained Embedded Devices, *Proc. of the Conf. on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, pp. 240-248, Jun. 2004.
- W. Hung, Y. Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Y. Tsai, Total Power Optimization through Simultaneously Multiple-VDD Multiple-VTH Assignment and Device Sizing with Stack Forcing, *Proc. of ISLPED'04*, pp. 144-159, Aug. 2004.
- A. Gayasen, K. Lee, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, T. Tuan, A Dual-Vdd Low Power FPGA Architecture, *Proc. of the Inter. Conf. on Field-Programmable Logic and its Applications (FPL)*, Springer-Verlag LNCS 3203(1): 145-147, Aug. 2004.
- M. Kandemir, O. Ozturk, M. J. Irwin, I. Kolcu, Using Data Compression to Increase Energy Savings in Multi-bank Memories, *Proc. of the Inter. Conf. on Parallel and Distributed Computing (Euro-Par)*, Springer-Verlag LNCS 3149(1):310-317, Aug.-Sep. 2004.
- V. De La Luz, M. Kandemir, A. Sivasubramaniam, M. J. Irwin, Exploring the Possibility of Operating in the Compressed Domain, *Proc. of Euro-Par'04*, Springer-Verlag LNCS 3149(1):507-515, Aug.-Sept. 2004.
- G. Chen, B. T. Kang, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, R. Chandramouli, Studying Energy Tradeoffs in Off-loading Computation/Compilation in Java-enabled Mobile Devices, *IEEE Trans. on Parallel and Distributed Systems*, 15(9):795-809, Sep. 2004.
- Y-F. Tsai, A. Hegde, N. Vijaykrishnan, M. J. Irwin, T. Theocharides, ChipPower: An Architecture-Level Leakage Simulator, *Proc. of the Inter. Systems-on-Chip Conf. (SoCC)*, pp. 395-398, Sep. 2004.
- G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Field-level Analysis for Heap Space Optimization in Embedded Java, *Proc. of the Inter. Symp. on Memory Management (ISMM)*, pp. 131-142, Oct. 2004.
- Y-F. Tsai, D. Duarte, N. Vijaykrishnan, M. J. Irwin, Characterization and Modeling of Run-Time Techniques for Leakage Power Reduction, *IEEE Trans. on VLSI Systems*, 12(11):1221-1233, Nov. 2004.
- M. Kandemir, M. J. Irwin, G. Chen, I. Kolcu, Banked Scratch-pad Memory Management for Reducing Leakage Energy Consumption, *Proc. of ICCAD'04*, pp. 120-124, Nov. 2004.
- Y-F. Tsai, N. Vijaykrishnan, M. J. Irwin, Y. Xie, Influence of Leakage Reduction Techniques on Delay/Leakage Uncertainty, *Proc. of VLSI Design*, pp. 374-379, Jan. 2005.
- S. Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Optimizing Leakage Energy Consumption in Cache Bitlines, *Journal of Design Automation for Embedded Systems*, 9(1):5-18, Mar. 2005.
- O. Ozturk, M. Kandemir, M. J. Irwin, BB-GC: Basic-block Level Garbage Collection, *Proc. of DATE'05*, pp. 1032-1037, Mar. 2005.
- I. Kadayif, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, An Integer Linear Programming Based Tool for Wireless Sensor Networks, *Journal of Parallel and Distributed Computing*, 65(3):247-260, Mar. 2005.
- W. Zhang, Y-F. Tsai, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Leakage-Aware Compilation for VLIW Architectures, *IEE Proceedings: Computers and Digital Techniques*, 152(2): 251-260, Mar. 2005.
- G. Chen, M. Kandemir, M. J. Irwin, Exploiting Frequent Field Values in Java Objects for Reducing Heap Memory Requirements, *Proc. of the 1<sup>st</sup> ACM/USENIX Conf. on Virtual Execution Environments (VEE)*, pp. 68-78, June 2005.
- S. Kim, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Exploiting Temporal Loads for Low Latency and High Bandwidth Memory, *IEE Proceedings: Computers and Digital Techniques*, 152(4): 457-465, July 2005.
- G. Wang, M. J. Irwin, P. Berman, H. Fu, T. F. La Porta, Optimizing Sensor Movement Planning for Energy Efficiency, *Proc. of ISLPED'05*, pp. 215-220, Aug. 2005.
- M. Kandemir, M. J. Irwin, G. Chen, I. Kolcu, Compiler-Guided Leakage Optimization for Banked Scratch-Pad Memories, *IEEE Trans. on VLSI Systems*, 13(10):1136-1146, Oct. 2005.
- J. Hu, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Analyzing Data Reuse for Cache Reconfiguration, *ACM Trans. on Embedded Computing Systems*, 4(4):851-576, Nov. 2005.

- I. Kadayif, M. Kandemir, G. Chen, N. Vijaykrishnan, M. J. Irwin, A. Sivasubramaniam, Compiler-directed High-level Energy Estimation and Optimization, *ACM Trans. on Embedded Computing Systems*, 4(4):819-850, Nov. 2005.**
- N. Vijaykrishnan, M. J. Irwin, M. Kandemir, L. Li, G. Chen, B. T. Kang, Designing Energy-aware Sensor Systems, *Frontiers in Distributed Sensor Networks*, pp. 653-666, Ed. by Brooks and Iyengar, CRC Press, 2005.
- H. Saputra, N. Vijaykrishnan, M. Kandemir, R. Brooks, M. J. Irwin, An Energy-aware Approach for Sensor Data Communication, *Frontiers in Distributed Sensor Networks*, pp. 697-720, Ed. by Brooks and Iyengar, CRC Press, 2005.
- I. Kadayif, M. Kandemir, A. Choudhary, M. Karakoy, N. Vijaykrishnan, M. J. Irwin, Compiler-directed Communication Energy Optimizations for Microsensor Networks, *Frontiers in Distributed Sensor Networks*, pp. 711-734, Ed. by Brooks and Iyengar, CRC Press, 2005.
- W. Zhang, Y-F. Tsai, D. Duarte, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Reducing Dynamic and Leakage Energy in VLIW Architectures, *ACM Trans. on Embedded Computing Systems*, 5(1):1-28, Feb. 2006.**
- G. Chen, M. Kandemir, M. J. Irwin, J. Ramanujam, Reducing Code Size Through Address Register Assignment, *ACM Trans. on Embedded Computing Systems*, 5(1):225-258, Feb. 2006.**
- J. Hu, N. Vijaykrishnan, M. J. Irwin, M. Kandemir, Optimizing Power Efficiency in Trace Cache Fetch Unit, *IET Computers and Digital Techniques*, 1(4):334-348, July 2007.**
- S. Kim, N. Vijaykrishnan, M. J. Irwin, Reducing Non-Deterministic Loads in Low-Power Caches via Early Cache Set Resolution, *Microprocessors and Microsystems*, 31(5):293-301, August 2007.**
- W-L Hung, Y. Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Total Power Optimization for Combinational Logic Using Genetic Algorithms, *Journal of VLSI Signal Processing System*, 58(2):145-160, February 2010.**

*Work in the area of leakage controlled SRAM cells in the summer of 2002 revealed that such structures, like many leakage optimized vDSM (very Deep SubMicron) circuits, are susceptible to an increased rate of soft errors (errors from alpha particle or cosmic ray hits that cause the memory bit to change state but that do not permanently damage the circuit). Other issues in system reliability also arise due to the relative increases in process variations and chip temperature variations, aging effects (such as electro migration and NBTI), and wire cross talk with technology scaling below 130 nanometers and due to the presence of substrate noise in mixed-signal circuits. Thus, the study of reliable, energy-efficient circuits in the face of transient and permanent errors has become another line of research.*

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#### **Publications:**

- V. Degalahal, N. Vijaykrishnan, M. J. Irwin, Soft Error Susceptibility of Low Power SRAM Designs, *Proc. of VLSI Design*, pp. 539-545, Jan. 2003.
- B. Kang, N. Vijaykrishnan, M. J. Irwin, D. Duarte, Substrate Noise Detector for Noise Tolerant Mixed-Signal IC, *Proc. of ASIC/SOC'03*, pp. 279-282, Sep. 2003.
- R. Ramanarayanan, V. Degalahal, N. Vijaykrishnan, M. J. Irwin, D. Duarte, Analysis of Soft Error Rate in Flip-Flops and Scannable Latches, *Proc. of ASIC/SOC'03*, pp. 231-234, Sep. 2003.
- W. Zhang, M. Kandemir, A. Sivasubramaniam, M. J. Irwin, Performance, Energy, and Reliability Tradeoffs in Replicating Hot Cache Lines, *Proc. of CASES '03*, pp. 309-317, Oct 2003.
- L. Li, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Adaptive Error Protection for Energy Efficiency, *Proc. of ICCAD'03*, pp. 2-7, Nov. 2003.
- L. Li, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, A Crosstalk Aware Interconnect with Variable Cycle Transmission, *Proc. of DATE'04*, pp. 102-107, Feb 2004.

- M. Pirreti, M., G. Link, R. Brooks, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Fault-tolerant Algorithms for Network-on-chip Interconnect, *Proc. of ISVLSI'04*, pp. 46-51, Feb 2004.
- V. Degalahal, R. Rajaram, N. Vijaykrishnan, Y. Xie, M. J. Irwin, The Effect of Threshold Voltages on Soft Error Rates, *Proc. of ISQED'04*, pp. 503-508, March 2004.
- L. Li, V. Degalahal, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Soft Error and Energy Consumption Interactions: A Data Cache Perspective, *Proc. of ISLPED'04*, pp. 132-137, Aug. 2004.
- G. Chen, M. Kandemir, N. Vijaykrishnan, A. Sivasubramaniam, M. J. Irwin, Analyzing Heap Error Behavior in Embedded JVM Environments, *Proc. of the Inter. Conf. on Hardware/Software Codesign and Systems Synthesis (CODES+ISSS)*, pp. 230-235, Sep. 2004.
- Y. Xie, L. Li, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Reliability-aware Cosynthesis for Embedded Systems, *Proc. of ASAP'04*, pp. 41-50, Sep. 2004.
- S. Srinivasan, A. Gayasen, N. Vijaykrishnan, M. Kandemir, Y. Xie, M. J. Irwin, Improving Soft-error Tolerance of FPGA Configuration Bits, *Proc. of ICCAD'04*, pp. 107-110, Nov. 2004.
- B. Kang, N. Vijaykrishnan, M. J. Irwin, Analyzing Software Influences on Substrate Noise: An ADC Perspective, *Proc. of ICCAD'04*, pp. 916-922, Nov. 2004.
- K. Unlu, V. Degalahal, M. S. Cetiner, N. Vijaykrishnan, M. J. Irwin, Testing Neutron-induced Soft Errors in Semiconductors, *Proc. of the American Nuclear Society Winter Meeting*, pp. 825-826, Nov. 2004.
- G. Chen, M. Kandemir, M. J. Irwin, Compiler-directed Selective Data Protection Against Soft Errors, *Proc. of ASP-DAC'05*, pp. 713-716, Jan. 2005.
- J. Hu, F. Li, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Compiler-directed Instruction Duplication for Soft Error Detection, *Proc. of DATE'05*, pp. 1056-1057, Mar. 2005.
- W-L. Hung, Y. Xie, N. Vijaykrishnan, C. Addo-Quaye, T. Theocharides, M. J. Irwin, Thermal-Aware Floorplanning Using Genetic Algorithms, *Proc. of ISQED'05*, pp. 634-639, Mar. 2005.
- W-L. Hung, Y. Xie, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Thermal-Aware Allocation and Scheduling for Systems-on-a-Chip Design, *Proc. of DATE'05*, pp. 898-899, Mar. 2005.
- S. Mourali, T. Theocharides, L. Benini, G. DeMicheli, N. Vijaykrishnan, M. J. Irwin, Analysis of Error Recovery Schemes for Networks-On-Chips, *IEEE Design and Test of Computers*, 22(5):434-442, Oct. 2005.**
- V. Degalahal, L. Li, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, Soft Error Issues in Low-Power Caches, *IEEE Trans. on VLSI Systems*, 13(10):1157-1166, Oct. 2005.**
- R. Ramanarayanan, J. S. Kim, N. Vijaykrishnan, Y. Xie, M. J. Irwin, SEAT-LA: A Soft Error Analysis Tool for Combinational Logic, *Proc. of VLSI Design*, pp. 499-502, Jan. 2006.
- G. Chen, G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Object Duplication for Improving Reliability. *Proc. of ASP-DAC'06*, pp. 140-145, Jan. 2006.
- F. Wang, Y. Xie, N. Vijaykrishnan, M. J. Irwin, On-chip Bus Thermal Analysis and Optimization, *Proc. of DATE'06*, Vol. 1, pp. 850-855, Mar. 2006.
- R. Ramanarayanan, Krishnan, N. Vijaykrishnan, Y. Xie, M. J. Irwin, Temperature and Voltage Scaling Effects on Electrical Masking, *Proc. of the 2<sup>nd</sup> Workshop on System Effects of Logic Soft Errors (SELSE)*, 4 pages, Apr. 2006.
- V. Degalahal, R. Ramanarayanan, N. Vijaykrishnan, Y. Xie, M. J. Irwin, Effect of Power Optimizations on Soft Error Rate, *IFIP Series on VLSI-SoC*, Ed. by Reis, May 2006.
- M. Mutyam, F. Li, N. Vijaykrishnan, M. Kandemir, M.J. Irwin, Compiler-Directed Thermal Management for VLIW Functional Units, *Proc. of LCTES'06*, pp. 163-172, June 2006.
- R. Ramakrishnan, S. Srinivasan, N. Vijaykrishnan, M. J. Irwin, Impact of NBTI on FPGAs, *Proc. of VLSI Design*, pp. 717-722, Jan. 2007.
- A. Mupid, M. Mutyam, N. Vijaykrishnan, Y. Xie, M.J. Irwin, Variation Analysis of CAM Cells, *Proc. of ISQED'07*, pp. 333-338, Mar. 2007.
- R. Krishnan, R. Ramanarayanan, S. Srinivasan, N. Vijaykrishnan, Y. Xie, M.J. Irwin, Variation Impact on SER of Combinational Circuits, *Proc. of ISQED'07*, pp. 911-916, Mar. 2007.
- A. Ricketts, M. Mutyam, N. Vijaykrishnan, M. J. Irwin, Investigating Simple Low Latency Reliable Multiported Register Files, *Proc. of ISVLSI'07*, pp. 375-382, May 2007.
- K. Unlu, N. Vijaykrishnan, S. M. Cetiner, V. Degalahal, M. J. Irwin, Neutron-induced Soft Error Rate Measurements in Semiconductor Memories, *Nuclear Instructions & Methods in Physics Research*, pp. 252-255, Aug. 2007.**
- F. Wang, F., M. Debole, X. Wu, Y. Xie, N. Vijaykrishnan, M.J. Irwin, On-chip Bus Thermal Analysis and Optimization, *IET Computer & Digital Techniques*, 1(5):590-599, Sept. 2007.**

- Y. Xie, L. Li, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Reliability-Aware Co-synthesis for Embedded Systems, *Journal of VLSI Signal Processing*, 49(1):87-99, October 2007.
- N. Soundararajan, A. Yanamandra, C. Nicopoulos, N. Vijaykrishnan, A. Sivasubramaniam, M.J. Irwin, Analysis and Solutions to Issue Queue Process Variation, *Proc. of DSN*, pp. 11-21, June 2008.
- S. Srinivasan, N. Vijaykrishnan, R. Krishnan, P. Mangalagiri, Y. Xie, M. J. Irwin, K. Sarpatwari, Toward Increasing FPGA Lifetime, *IEEE Trans. on Dependable and Secure Computing*, 5(2):115-127, June 2008.
- C. Celik, K. Unlu, K. Ramakrishnan, R. Rajaraman, N. Vijaykrishnan, M. J. Irwin, Y. Xie, Thermal Neutron Induced Soft Error Rate Measurement in Semiconductor Memories and Circuits, *Journal of Radioanalytical and Nuclear Chemistry*, 278(2):509-512, August 2008.
- J. Hu, F. Li, V. Degalahal, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Compiler-Assisted Soft Error Detection under Performance and Energy Constraints in Embedded Systems, *ACM Trans. on Embedded Computing Systems*, 8(4):Article 27 (30 pages), July 2009.
- M. Mutyam, F. Wang, R. Krishnan, N. Vijaykrishnan, M. Kandemir, Y. Xie, M. J. Irwin, Process-Variation-Aware Adaptive Cache Architecture and Management, *IEEE Trans. on Computers*, 58(7):865-877, July 2009.
- R. Rajaraman, V. Degalahal, J. S. Kim, N. Vijaykrishnan, Y. Xie, M.J. Irwin, Modeling Soft Errors at Device and Logic Level for Combinatorial Circuits, *IEEE Trans. on Dependable and Secure Computing*, 6(3):202-216, July-Sept. 2009.

With the emergence of promising new “nano” technologies another new line of multidisciplinary research has emerged – that of mixed technology circuits. The initial focus is on **nanotechnologies** that are used to augment CMOS circuitry such as new input/output technologies, new non-volatile memory structures, etc. Another “advanced technology” issue is that of **3D integrated circuits** – where a stack of multiple device layers with direct vertical interconnections between the layers (through silicon vias (TSVs)) are put together in the same package. As fabrication of 3D ICs becomes a reality, developing CAD tools to support their design and exploring new architectural alternatives have become an interest.

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#### Ph.D. Students:

#### Publications:

- W. Xu, N. Vijaykrishnan, Y. Xie, M. J. Irwin, Design of a Nanosensor Array Architecture, *Proc. of GLSVLSI'04*, pp. 298-303, Apr. 2004.
- R. Hernandez, Y. Cao, H. Prakasam, T. Mallouk, M. J. Irwin, Conducting Polymer Nanowires for Chemical Sensor Arrays, *Abstracts of Papers of the American Chemical Society*, 228:U869, 588-INOR Part 1, Aug. 2004.
- K. Irick, W. Xu, N. Vijaykrishnan, M. J. Irwin, A Nanosensor Array Based VLSI Gas Discriminator, *Proc. of VLSI Design*, pp. 241-248, Jan. 2005.
- A. Gayasen, N. Vijaykrishnan, M. J. Irwin, Exploring Technology Alternatives for Nano-Scale FPGA Interconnects, *Proc. of DAC'05*, pp. 921-926, Jun. 2005.
- Y-F. Tsai, Y. Xie, N. Vijaykrishnan, M. J. Irwin, Three-dimensional Cache Design using 3DCacti, *Proc. of ICCD'05*, pp. 519-524, Oct. 2005.
- A. Ricketts, K. Irick, N. Vijaykrishnan, M. J. Irwin, Priority Scheduling in Digital Microfluidics-Based Biochips, *Proc. of DATE'06*, Vol. 1, 329-335, Mar. 2006.
- W-L. Hung, G. Link, Y. Xie, N. Vijaykrishnan, M. J. Irwin, Interconnect and Thermal-aware Floorplanning for 3D Microprocessors, *Proc. of ISQED'06*, pp. 98-104, Mar. 2006.
- B. Vaidyanathan, W. Hung, F. Wang, Y. Xie, N. Vijaykrishnan, M.J. Irwin, Architecting Microprocessor Components in 3D Design Space, *Proc. of VLSI Design*, CDROM-6pps, Jan. 2007.
- Y. Tsai, F. Wang, Y. Xie, N. Vijaykrishnan, M. J. Irwin, Design Space Exploration for Three-Dimensional Cache, *IEEE Trans. on VLSI Systems*, 16(4):444-455, April 2008.
- P. Mangalagiri, P., K. Sarpatwari, A. Yanamandra, N. Vijaykrishnan, Y. Xie, M. J. Irwin, O. A. Karim, A Low-power Phase Change Memory Based Hybrid Cache Architecture, *Proc. of GLSVLSI'08*, pp. 395-398, May 2008.
- Y. Xie, S. Eachempati, A. Yanamandra, N. Vijaykrishnan, M. J. Irwin, Power and Area Reduction using Carbon Nanotube Bundle Interconnect in Global Clock Tree Distribution Network, *Proc. of the IEEE/ACM Inter. Symp. on Nanoscale Architectures (NANOARCH'09)*, pp. 51-56, July 2009.

J. Ouyang, G. Sun, Y. Chen, L. Duan, T. Zhang, Y. Xie, M. J. Irwin, Arithmetic Unit Design Using 180nm TSV-based 3D Stacking Technology, *Proc. of the IEEE Inter. 3D Systems Integration Conf. (3DIC'09)*, CDROM-4 pps, Sept 2009.

*While the original motivation for research in the design of power aware systems was in the mobile and embedded space, it has also become an issue in the server and high-performance computing space where both energy consumption and thermal (cooling) have become major constraints. Thus, the research with Dr. Vijay Narayanan (N. Vijaykrishnan), Dr. Kandemir, and Dr. Xie has expanded to cover that space with a focus on the design of high performance, power-efficient, resilient **chip multiprocessors** (CMPs) and multiprocessor systems on a chip (MPSoC). A project with Dr. Raghavan - called *pxp* - focused on optimizing the performance and power of computational science applications on high-performance systems. This work has been supported by NSF and DARPA/MARCO/GSRC.*

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- 9/04-8/07 NSF/STHEC Grant, 0444345, Adaptive Software for Extreme-Scale Scientific Computing: Co-Managing Quality-Performance-Power Tradeoffs (with P. Raghavan, Norris, and McInnes); \$749,755
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- 5/07-5/10 NSF/CCF, 0702519, A Self-Regulating Compiler Framework for NoC Based CMPs (with M. Kandemir), \$425,000
- 8/07-8/10 NSF/CSR-SMA, 0720749, Toward Model-Driven Multilevel Analysis and Optimization of Multicomponent Computer Systems (with P. Raghavan, M. Kandemir, S. Shontz, L. Li), \$750,000
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- 8/08-7/11 NSF/CPA-CPL, 0811687, REEact: A Robust Execution Environment for Fragile Multicore Systems (with M. Kandemir), \$599,999

#### **Ph.D. Students:**

- Konrad Malkowski, Ph.D., 8/09, Design Explorations in High-Performance, Low Power Systems (co-advised with P. Raghavan), Mathworks, Natick, MA
- Aditya Yanamandra, Ph.D., 8/10, Exploring Power Reliability Tradeoffs in On-Chip Networks, (co-advised with V. Narayanan), Intel, Portland, Oregon

#### **Publications:**

- I. Kadayif, I. Kolcu, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, Exploiting Processor Workload Heterogeneity for Reducing Energy Consumption in Chip Multiprocessor, *Proc. of DATE'04*, pp. 1158-1163, Feb 2004.
- O. Ozturk, M. Kandemir, M. J. Irwin, I. Kolcu, Tuning Data Replication for Improving Behavior of MPSoC Applications, *Proc. of GLSVLSI'04*, pp. 170-173, Apr. 2004.
- M. J. Irwin, L. Benini, N. Vijaykrishnan, M. Kandemir, Techniques for Designing Energy-aware MPSoCs, *Multiprocessor Systems-on-Chips*, Chpt. 2, pp. 21-47, Ed. by Jerraya and Wolf, Sep. 2004.
- W. Hung, C. Addoquay, T. Theocharides, Y. Xie, N. Vijaykrishnan, M. J. Irwin, Thermal Aware IP Virtualization and Placement for Networks On Chip Architecture, *Proc. of ICCD'04*, pp. 430-437, Oct. 2004.
- I. Kadayif, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, I. Kolcu, Reducing Energy Consumption in Chip Multiprocessors using Workload Variation, *Ultra-Low Power Electronics and Design*, pp. 123-140, Ed. by Macii, 2004.
- O. Ozturk, M. Kandemir, G. Chen, M. J. Irwin, Customized On-chip Memories for Embedded Chip Multiprocessors, *Proc. of ASP-DAC'05*, pp. 743-748 Vol. 2, Jan. 2005.
- Y-F. Tsai, N. Vijaykrishnan, Y. Xie, M. J. Irwin, Leakage-Aware Interconnect for On-Chip Networks, *Proc. of DATE'05*, pp. 230-231, Mar. 2005.
- C. Liu, A. Sivasubramaniam, M. Kandemir, M. J. Irwin, Exploiting Barriers to Optimize Power Consumption of CMPs, *Proc. of IPDPS'05*, (CD ROM), Apr. 2005.
- O. Ozturk, M. Kandemir, M. J. Irwin, Using Data Compression in an MPSoC Architecture for Improving Performance, *Proc. of GLSVLSI'05*, pp. 353-356, Apr. 2005.
- P. Raghavan, M. J. Irwin, L. C. McInnes, B. Norris, Adaptive Software for Scientific Computing: Co-Managing Quality-Performance-Power Tradeoffs, *Proc. of the NSF Next Generation Software Workshop*, in conjunction with IPDPS'05, Apr. 2005.

- E.-J. Kim, G. Link, K. H. Yum, N. Vijaykrishnan, M. Kandemir, M. J. Irwin, C. R. Das, A Holistic Approach to Designing Energy-Efficient Cluster Interconnects, *IEEE Trans. on Computers*, 54(6):660-671, June 2005.**
- O. Ozturk, M. Kandemir, M. J. Irwin, On-Chip Memory Management for Embedded MPSoC Architectures Based on Data Compression, *Proc. of SoCC'05*, pp. 175-178, Sep. 2005.
- S. Akioka, S. Kennedy, K. Malkowski, M. J. Irwin, P. Raghavan, L. McInnes, B. Norris, Co-Managing Performance and Power for High-Performance Scientific Computing, *Proc. of the ACM/IEEE Conf. on Supercomputing (SC)*, Poster, Nov. 2005.
- T. Theocharides, G. Link, N. Vijaykrishnan, M. J. Irwin, Networks on Chip: Interconnects for the Next Generation Systems on Chip, *Advances in Computers*, 63(1):35-89, Ed. by Zelkowitz and Hurson, 2005.
- C. Liu, A. Sivasubramaniam, M. Kandemir, M. J. Irwin, Enhancing L2 Organization for CMPs with a Center Cell, *Proc. of IPDPS'06*, CDROM-10pps, Apr. 2006.
- K. Malkowski, I. Lee, P. Raghavan, M.J. Irwin, Conjugate Gradient Sparse Solvers: Performance-power Characteristics, *Proc. of the 20<sup>th</sup> IEEE Inter. Parallel and Distributed Processing Symposium (IPDPS'06)*, (CD-ROM) 8 pages, Apr. 2006.
- K. Malkowski, I. Lee, P. Raghavan, M.J. Irwin, On Improving Performance and Energy Profiles of Sparse Scientific Applications, *Proc. of IPDPS'06*, CDROM-8pps, Apr. 2006.
- S. Akioka, K. Malkowski, P. Raghavan, M. J. Irwin, L. C. McInnes, B. Norris, Characterizing the Performance and Energy Attributes of Scientific Simulations, *Proc. of the Inter. Conf. on Computer Science (ICCS)*, Springer-Verlag LNCS 3991(1):242-249, May 2006.
- O. Ozturk, M. Kandemir, M. J. Irwin, S. Tosun, Multi-level On-chip Memory Hierarchy Design for Embedded Chip Multiprocessors, *Proc. of the 12<sup>th</sup> Inter. IEEE Conf. on Parallel and Distributed Systems (ICPADS'06)*, pp. 383-390, July 2006. **Best Paper Award Winner**
- Y. Ding, M. Kandemir, P. Raghavan, M.J. Irwin, Adapting Application Execution to Reduced CPU Availability, *Proc. of the Annual Workshop on the Interaction Between Compilers and Computer Architecture (Interact-11)*, pp. 24-31, Feb. 2007.
- K. Malkowski, P. Raghavan, M.J. Irwin, Memory Optimizations for Fast Power-Aware Sparse Computations, *Proc. of the Next Generation Software Workshop*, held in conjunction with *IPDPS'07*, CDROM-7pps, Mar. 2007.
- S. Conner, S. Akioka, M.J. Irwin, P. Raghavan, Link Shutdown Opportunities During Collective Communications in 3-D Torus Nets, *Proc. of IPDPS'07*, CDROM-8pps, Mar. 2007.
- K. Malkowski, G. Link, P. Raghavan, M.J. Irwin, Load Miss Prediction - Exploiting Power Performance Trade-offs, *Proc. of IPDPS'07, 3<sup>rd</sup> Workshop on High-Performance, Power-Aware Computing (HP-PAC'07)*, held in conjunction with *IPDPS'07*, CDROM-8pps, Mar. 2007.
- K. Malkowski, P. Raghavan, M. Kandemir, M. J. Irwin, Phase-aware Adaptive Hardware Selection for Power-Efficient Scientific Computations, *Proc. of ISLPED'07*, pp. 403-406, Aug. 2007.
- S. Akioka, F. Li, M. Kandemir, P. Raghavan, M. J. Irwin, Ring Prediction for Non-Uniform Cache Architectures, *Proc. of the 16<sup>th</sup> Inter. Conf. on Parallel Architecture and Compilation Techniques (PACT'07)*, p. 401, Sept. 2007.
- A. Yanamandra, B. Cover, P. Raghavan, M.J. Irwin, M. Kandemir, K. Malkowski, Evaluating the Role of Scratchpad Memories in Multi-cores for Sparse Matrix Computations, *Proc. of SC'07*, Nov. 2007. **Nominated as a Finalist for the Best Poster Award.**
- S. Srikantaiah, M. Kandemir, M.J. Irwin, Adaptive Set-Pinning: Managing Shared Caches in Chip Multiprocessors, *Proc. of ASPLOS*, pp. 135-144, Mar. 2008.
- Y. Ding, M. Kandemir, P. Raghavan, M.J. Irwin, A Helper Thread Based EDP Reduction Scheme for Adapting Application Execution in CMPs, *Proc. of IPDPS'08*, 14 pages, Apr. 2008. **Best Paper Award Winner**
- B. Cover, A. Yanamandra, P. Raghavan, M.J. Irwin, M. Kandemir, Evaluating the Role of Scratchpad Memories in Chip Multiprocessors for Sparse Matrix Computations, *Proc. of IPDPS'08*, 10 pages, Apr. 2008.
- P. Raghavan, M. Kandemir, M. J. Irwin, K. Malkowski, Managing Power, Performance and Reliability Trade-offs, *Proc. of the Next Generation Software (NGS) Workshop*, in conjunctions with *IPDPS'08*, CD-ROM-5 ppgs, April 2008.
- F. Li, M. Kandemir, M.J. Irwin, Implementation and Evaluation of a Migration-based NUCA Design for Chip Multiprocessors, *Proc. of SIGMETRICS*, pp. 449-450, June 2008.
- T. Yemliha, S. Srikantaiah, M. Kandemir, M. Karakoy, M. J. Irwin, Integrated Code and Data Placement in Two-Dimensional Mesh Based Chip Multiprocessors, *Proc. of ICCAD'08*, 6 pages, Nov. 2008.
- M. Kandemir, F. Li, M. J. Irwin, S. W. Son, A Novel Migration-based NUCA Design for Chip Multiprocessors, *Proc. of SC'08*, 12 pages, Nov. 2008.

- A. Yanamandra, M.J. Irwin, N. Vijaykrishnan, M. Kandemir, In-Network Caching for Chip Multiprocessors, *Proc. of Inter. Conf. on High-Performance Embedded Architectures and Compilers (HiPEAC)*, Springer-Verlag LNCS 5409:373-388, Jan. 2009.
- Y. Ding, M. Kandemir, M.J. Irwin, P. Raghavan, Adapting Application Mapping to Systematic Within-Die Process Variations on Chip Multiprocessors, *Proc. of HiPEAC*, Springer-Verlag LNCS 5409:231-247, Jan. 2009.
- O. Ozturk, M. Kandemir, M. J. Irwin, Using Data Compression for Increasing Memory System Utilization, *IEEE Trans. on CAD*, 28(6):901-914, June 2009.**
- Y. Ding, M. Kandemir, P. Raghavan, M. J. Irwin, Adapting Application Execution in CMPs Using Helper Threads, *Journal of Parallel and Distributed Computing* 69(9):790-806, Sept. 2009.**
- M. Kandemir, O. Ozturk, S. Narayanan, M. J. Irwin, Compiler Directed Communication Reliability Enhancement for Chip Multiprocessors, *Proc. of LCTES'10*, pp. 85-94, April 2010. Also published in *SIGPLAN Notices*, 45(4):85-94, April 2010.
- Y. Ding, M. Kandemir, M. J. Irwin, P. Raghavan, Dynamic Core Partitioning for Energy Efficiency, *Proc. of the Workshop on High-Performance, Power-Aware Computing (HPPAC 2010)*, in conjunction with IPDPS 2010, April 2010.
- K. Malkowski, P. Raghavan, M. Kandemir, M. J. Irwin, T-NUCA – A Novel Approach to Non-Uniform Access Latency Cache Architectures for 3D CMPs, *Proc. of the HPPAC'10*, in conjunction with IPDPS 2010, April 2010.
- M. Kandemir, T. Yemliha, S. Muralidhara, S. Srikantaiah, M. J. Irwin, Y. Zhang, Cache Topology Aware Computation Mapping for Multicores, *Proc. of the ACM Conf. on Programming Language Design and Implementation (PLDI'10)*, pp. 74-85, June 2010.