

LCTES 2009 Technical Program

Friday, June 19, 2009

Breakfast (7:30am - 8:30am)

Opening Remarks (8:30am - 8:40am)

Invited Talk (8:40-10:00)

Break (10:00-10:20)

Paper Session 1: Scheduling (10:20-12:00)

- **Modulo Scheduling without Overlapped Lifetimes**
 - Eric Stotzer and Ernst Leiss
- **Synchronous Objects with Scheduling Policies, Introducing safe shared memory in Lustre**
 - Paul Caspi, Jean-louis Colaço, Léonard Gérard, Marc Pouzet and Pascal Raymond
- **Recurrence Cycle Aware Modulo Scheduling for Coarse-Grained Reconfigurable Architectures**
 - Taewook Oh, Bernhard Egger, Hyunchul Park and Scott Mahlke
- **PTIDES on Flexible Task Graph: Real-Time Embedded System Building from Theory to Practice**
 - Jia Zou, Joshua Auerbach, David F. Bacon and Edward A. Lee

Lunch (12:00-1:30)

Paper Session 2: Programming languages and Compiler Optimizations (1:30-3:10)

- **A Compiler Optimization to Reduce Soft Errors in Register Files**
 - Jongeun Lee and Aviral Shrivastava
- **Raced Profiles: Efficient Selection of Competing Compiler Optimizations**
 - Hugh Leather, Michael O'Boyle and Bruce Warton
- **Eliminating the Call Stack to Save RAM**
 - Xuejun Yang, Nathan Coopriker and John Regehr
- **Live-range Unsplitting for Faster Optimal Coalescing**
 - Sandrine Blazy and Benoît Robillard

Break (3:10-3:40)

Student Poster Session (3:40-5:30)

Saturday, June 20, 2009

Breakfast (7:30-8:30)

Paper Session 3: Architecture and Multicores (8:30-10:10)

- **Push-Assisted Migration of Real-Time Tasks in Multi-Core Processors**
 - Abhik Sarkar, Frank Mueller, Harini Ramaprasad and Sibin Mohan
- **Software Transactional Memory for Multicore Embedded Systems**
 - Jennifer Mankin, David Kaeli and John Ardini
- **Synergistic Execution of Stream Programs on Multicores with Accelerators**
 - Abhishek Udupa, R. Govindarajan and Matthew J. Thazhuthaveetil
- **Towards device emulation code generation**
 - Thomas Heinz and Reinhard Wilhelm

Break (10:10-10:40)

Invited Talk (10:40-12:00)

Lunch (12:00-1:30)

Paper Session 4: Runtime System Support (1:30-3:10)

- **Guaranteeing Instruction Fetch Behavior with a Lookahead Instruction Fetch Engine (LIFE)**
 - Stephen Hines, Yuval Peress, Peter Gavin, David Whalley and Gary Tyson
- **Debugging FPGA-based Packet Processing Systems through Transaction-level Communication-centric Monitoring**
 - Paul McKechnie, Michaela Blott and Wim Vanderbauwhede
- **Tracing Interrupts in Embedded Software**
 - Giovanni Gracioli and Sebastian Fischmeister
- **Addressing the Challenges of DBT for the ARM Architecture**
 - Ryan W. Moore, Jose A. Baiocchi, Bruce R. Childers, Jack W. Davidson and Jason D. Hiser

Break (3:10-3:40)

Paper Session 5: Validation and Verification (3:40-4:30)

- **Integrating Hardware and Software Information Flow Analyses**
 - Colin Fidge and Diane Corney
- **Specification and Verification of Time Requirements with CCSL and Esterel**
 - Charles André and Frédéric Mallet