CMPEN 475
Functional Verification
Elective in Computer Engineering

Catalog Data: Functional Verification (3) Introduce concepts, methods, and technology for effective functional verification of modern electronic systems. Prerequisite: CMPEN 331.


Course Objectives: The objective of this course is to introduce techniques for verification of hardware designs, writing test benches and provide a hands-on feel for verification of designs. This course will provide an understanding of verification languages. This course will be broad enough to focus on principles of verification that can be applied to verification using various languages. We will also introduce formal verification.

Primary Course Outcomes: Upon completion of the course, students should possess the following skills:

- Learn to use verification tools and experiment on actual designs used in industry such as Verisity Specman, IBM Rulebase and Cadence NC-Sim VHDL simulation framework.
- Learn to plan and carry out effective functional verification of an electronic system design in a systematic fashion.
- Learn to work in teams to debug designs.

Relationship to Undergraduate Program Outcomes: This course collectively supports the following program outcomes:

- Demonstrate independent learning by using unfamiliar computer systems and software tools to solve technical problems.
- Write clear and effective technical prose for a technical audience.
- Analyze the performance of hardware systems using probabilistic, simulation and statistical methods.

Required Topics: (38 hours total)

- What is verification? - Introduction (3 hrs)
- Behavioral HDL - refresher and writing testbenches (3 hrs)
- Verification tools; Coverage metrics (3 hrs)
- Behind the simulation engine – event and cycle simulation (3 hrs)
- Introduction to Specman and e language basics (3 hrs)
- Verification plan – strategies/testcases/testbenches (3 hrs)
- Modeling structs;I/O blocks; data items (3 hrs)
- Modeling input relations/intervals/events (3 hrs)
- Introduction to Formal Verification (3 hrs)
- Verification Trends. (~3 hrs)
- Lab overview and review (~5 hrs)
- Exams and Review (~3 hrs)

Class Format: Lecture: 75 minutes, 2 lectures a week, 15 week/semester.
Laboratory: Open Lab. 24hr. access, first-come-first-served, appointment for demonstration.

Professional Component: Verifying design correctness of increasingly complex system-on-chip designs poses a major challenge to the semiconductor industry. As much as 70% of effort in a complex IC design project is now attributed to verification. Various case studies on actual industry and research designs will be provided in the lectures. The course will also be supplemented by lab-assignments that provide hands-on-experience to experiment with methodologies taught in the lectures and tools used in industry.
Evaluation: ~50% proctored assessments (exams)
~~50% unproctered assignments (homeworks, programming projects)

Suggested breakdown based of 100 pts as follows:

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<td>Exam 1</td>
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<td>Final</td>
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<td>Assignments (Lab projects and homeworks)</td>
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Last Revised: January 18, 2008