Adaptive Power Management in Software Radios using Resolution Adaptive Analog to Digital Converters

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Abstract

The popularity of Software Radios is increasing, as they have become one of the important emerging technologies in mobile communications. One of the major challenges during development of mobile communications hardware is the inevitable low power requirement. In this paper, we investigate power management for software radios. The use of resolution adaptive analog to digital converters as well as the flexibility of the modulation schemes that a re-configurable radio provides is investigated. The concept of a resolution adaptive analog to digital converter is to trade performance for energy efficiency. The energy delay product is used to evaluate the performance versus energy tradeoffs and an adaptive power management method is proposed.

1. Introduction

Software configurable receivers, often called software radios or software defined radios [1], have been growing in popularity since the mid 1990s. Software radios have several advantages over their purely analog counter parts. Their re-configurability allows for adaptations to changing requirements and environments. These changes can be made both pre and post deployment. On the contrary, in analog receivers, the architecture, communications protocol, and other performance requirements have to be fixed prior to the hardware design. Another advantage of software radios is that they provide the ability to do digital processing of the incoming signal. Digital signal processors can analyze the received signal for a vast number of parameters without requiring any additional hardware for each parameter. However, one of the major challenges during development of software radios is the power consumption.

Figure 1 shows the major components found in a typical digital receiver chain. Initial signal conditioning is done to provide isolation for the antenna and possibly filter out-of-band signals. In applications where a high frequency carrier is used, the signal must be down converted to an intermittent frequency that can be handled by the rest of the receiver chain. Often this down converted signal then requires an additional signal conditioning stage prior to being digitized, which is done by the analog to digital converter (ADC). The ADC provides a stream of data for analysis by the digital signal processor (DSP).

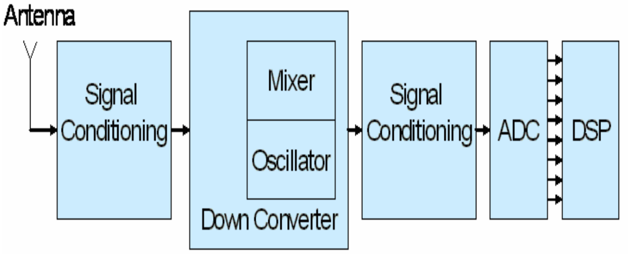

Figure 1. A typical digital receiver configuration

The power distribution for the generic receiver chain shown in Figure 1 depends on the number of down converter stages and the amount of gain in the signal conditioning blocks. A survey of components that are typically used in such receivers yielded the following trends: In the case of narrow band receivers, in which a low speed ADC could be used, the power was distributed evenly among the ADC stage, the down converter stage, and combined signal conditioning stages. For wideband receivers, in which a high performance ADCs are required, the ADC accounts for the majority of the power budget. It is clear that as the performance requirement increases from narrow to wider bands, so does the portion of the power budget consumed by the ADC. In applications that use direct conversion at the antenna, which is the ultimate goal of software radios [13], the power dissipation of the entire receiver is approximately that of the ADC (excluding the DSP power dissipation).

In this paper, we investigate power management techniques in soft radios (and applicable to generic digital receiver applications), using resolution adaptive

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ADCs. The paper is organized in the following manner. Section 2 provides a survey of related work. Section 3 discusses the effects of ADC resolution on performance and energy consumption, then presents the general concept behind a resolution adaptive ADC. In Section 4, we discuss the use of the resolution adaptive ADC in a digital receiver application. Section 5 presents a method for determining the most energy efficient configuration for our application. Section 6 concludes the paper.

2. Related work

Research targeted at lowering the power dissipation of analog to digital converters has been an effort that spans both industry and academics. All major ADC chip suppliers have a version with the words "Low Power" in the title of the data sheet. Typically these versions of the chip operate at lower supply voltages. Academic research has produced a handful of publications and chips that demonstrate techniques for lowering the power dissipation of converters. In general the techniques used to improve energy efficiency can be broken down into three levels. The lowest is at the circuit level were bias currents and component values are optimized [5]. The next level of abstraction is to change the ADC architecture. This work is mostly academic and includes hybrid [6], reconfigurable [7], and scalable architectures [4, 8]. The highest level of abstraction focuses on adjusting system performance in order to conserve the energy consumed by the ADC. Tools that allow system designers to make performance vs. power tradeoffs had been lacking until recent. Analog Devices recently released ADIsimADC, which includes device specific performance models that can be loaded into system level simulators such as MATLAB. Also the architecture level power estimator tool [3] is aimed at aiding systems designers in choosing the correct architecture for their needs. Such tools will need to be merged in the future.

Of course some research spans all three categories. A great example of this is the reconfigurable ADC proposed by Gulanti and Lee [7]. At the system level, the user selects from a range of operating frequencies and resolutions that best suit the application. Based on these performance specifications the ADC internal architecture can then be configured for either delta-sigma mode for high resolution and low speed applications, or pipeline mode for high speed and low resolution applications. Within each architecture configuration, parameters such as pipeline length and oversampling ratio can be adjusted. At the circuit level bias currents and capacitor sizes can be adjusted to obtain the most energy efficient configuration possible for the given performance requirements. The Gulanti and Lee ADC is a viable solution for applications with maximum sampling rates less than 10Mhz. However as the sampling rate increases, designers will be forced into using high end pipelined and eventually flash based architectures.

3. The Effect of ADC Resolution on Power and Performance

In this section, we describe the relationship between ADC resolution and power consumption as well as SNR (Signal to Noise Ratio).

Signal to noise ratio (SNR), also noted as Eb/No, is the amount of power contained in the desired information signal (Eb) versus the total amount of power contained in all other spectral components excluding harmonics (No). A theoretical estimation of an ADCs SNR performance can be found by the following equation (for complete derivation of this equation refer to [2]):

$$SNR_{ADC} = 6.02 * Bits + 1.76 \tag{1}$$

Note from equation 1 that a one bit increase in ADC resolution will result in a 6.02 dB increase in SNR performance (theoretically).

Recent research by Huang *et al.* [3] has shown that the energy consumption of an ADC can be accurately modeled at the architectural level. Their power estimation tool bases its results on the underlying ADC architecture, fabrication technology and clock frequency. For Pipeline based ADCs the authors found a linear relationship between ADC resolution and ADC power. Thus a 12 Bit Pipelined ADC would draw 2x the power of a 6 Bit Pipelined ADC. Advancements in design and fabrication technology has allowed Pipeline ADCs to be operated at clock speeds of several hundred megahertz. However, if performance requirements go beyond the capabilities of pipelined ADCs, designers are forced to use ADCs with flash based architectures. Flash ADCs have ability to operate at clock frequencies of several gigahertz. The power estimation for Flash ADCs is given by the equation:

$$P_{flash} = 2^{Bits-1} * P_{comparator} + P_{encoder} \tag{2}$$

Note in equation 2 that the power grows exponentially with ADC resolution. So for flash based ADC architectures, a two bit increase in resolution results in a 4x power increase. The potential for power savings in flash ADCs by reducing resolution is well captured by the authors of [4]. They developed a High Speed Power and Resolution Adaptive Analog to Digital Converter (HSPRA-ADC), which allows the user to change resolutions of the ADC at run time. An example of this will be discussed in more detail. Table 1 shows the performance results of the HSPRA-ADC.

Bits	Power (mW)	Speed (GSPS)	Switching Time (ns)
5	51.53	3.05	0.321 (5bit-to-8-bit)
6	97.25	2.66	0.277 (8bit-to-7bit)
7	185.78	2.05	0.279 (7bit-to-6bit)
8	367.12	1.82	0.277 (6bit-to-5bit)

Table 1. Power Dissipation of the HSPRA-ADC

Note in Table 1 that the difference in power dissipation is inline with the previous equation for flash based ADC architectures.

From equations 1 and 2 we can see that good signal to noise performance at the input of the receiver can be exploited by the DSP. When the received signal is strong, the DSP can reduce the resolution of the ADC, in order to save energy. In situations where the received signal is weak, the DSP can increase the resolution of the ADC in order to improve SNR performance.

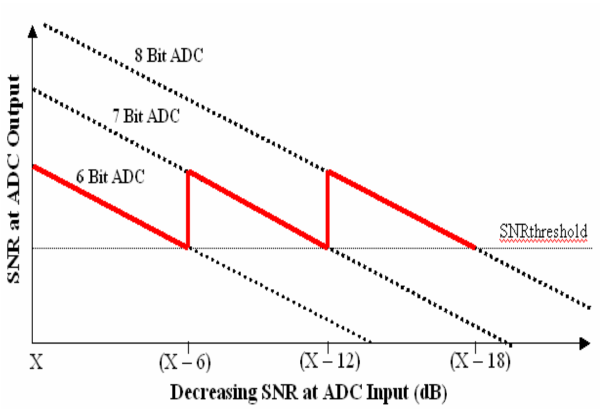

Figure 2. Dynamic ADC Resolution Adjustment

Figure 2 illustrates how a selected SNR threshold can be used to determine when to change resolutions of the ADC. The black dashed lines indicate the SNR performance of the corresponding ADC resolution. The solid line indicates which resolution is selected at a given time. At position X, the received signal is strong, so the ADC can operate in the 6bit mode. As the amplitude of the received signal decreases, the ADC resolution is increased in order to maintain a SNR performance above the desired threshold.

The potential energy savings from dynamically changing the ADC resolution is greatly dependent on the application. In applications were the distance between the transmitter and receiver is constantly changing, the DSP can keep the receiver in the most energy efficient mode possible. Consider a receiver designed with the HSPRA-ADC that operates for 1 minute. In 6 bit mode, the receiver consumes 5.8 Joules. In 8 bit mode, the receiver consumes 22.0 Joules, approximately 4x more energy. A second advantage exists for applications were the distance between transmitter and receiver is fixed, but not known until after deployment. An example of this would be randomly placed sensor fields. All of the sensors could be built identically, and then adjusted to the most energy efficient mode during initialization.

4. An Application of the Resolution Adaptive ADC

To investigate the effects of resolution scaling, we will consider protocols used in modern digital communications systems. Specifically, protocols which have the ability to change the number of information bits contained in each sample (usually stated as modulation order or bits per symbol). A good example of this is Phase Shift Keying (PSK). In PSK, at the transmitter end, consecutive bits are grouped into symbols. Each symbol is then assigned a phase offset from the reference signal. The transmitted signal is then phase shifted based on the symbol stream. The number of bits composing each symbol is called the modulation order.

On the receiver end of a PSK system, the received signal is compared against a reference. The phase difference is then computed and used to determine the correct symbol and thus the transmitted bit stream. Figure 3 illustrates the phase difference in symbols on what is called a constellation plot for PSK4 and PSK8 [9].

The symbols shown as white circles are used for PSK4, while both the white and black symbols are used for PSK8. From the constellation plot, it is easy to see that PSK8 will require a better SNR than its PSK4 counter part. The Communications Toolbox for MATLAB was used to model the following digital modulation schemes. Phase Shift Keying (PSK), Quadrature Amplitude Modulation (QAM) and Phase Amplitude Modulation (PAM). Each protocol was simulated with modulation orders of 4, 8, 16, and 32. Each of the modulation protocols was analyzed for Bit Error Rate (BER) versus SNR.

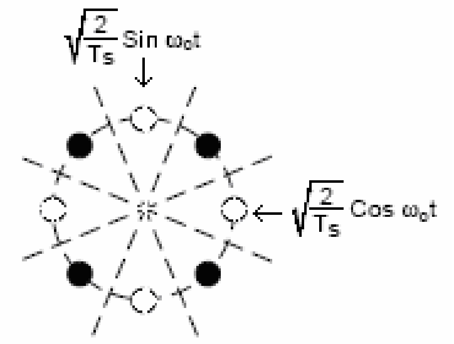

Figure 3. Symbol Distance for PSK4 and PSK8

BER is often used to measure the quality of a digital communication system. A typical test involves comparing the received data sequence versus the known transmitted sequence. There is a direct correlation between BER and SNR [10]. Figure 4 shows the simulation results for the PSK modulation scheme.

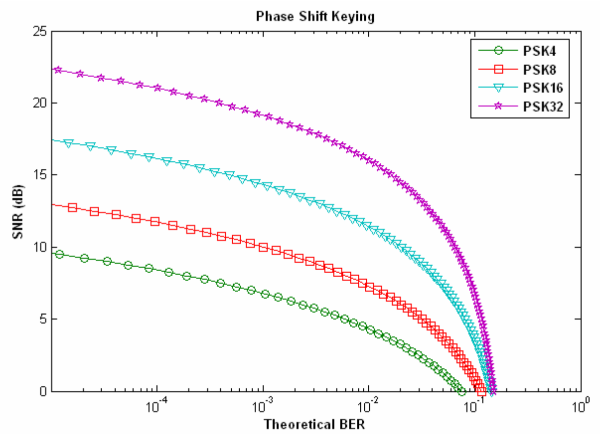

Figure 4. Theoretical BER vs. SNR of a PSK system

Note in Figure 4 that for a BER of 1 in 10^3 bits, PSK4 required a SNR of 6.25 dB. This was approximately 3.5 dB less than PSK8, 8 dB less than PSK16, and 13 dB less than PSK32 for the same BER. It can also be seen that these distances are constant, regardless of the selected BER [12]. Similar results were obtained from the simulations of the QAM (shown in Figure 5) and PAM systems.

In typical applications, the modulation order is selected based on desired throughput and bandwidth of the system. However here we consider changing the modulation order as a means of conserving energy in the system. The receiver operation can be broken down in to three areas according to input SNR levels of low, mid, and high.

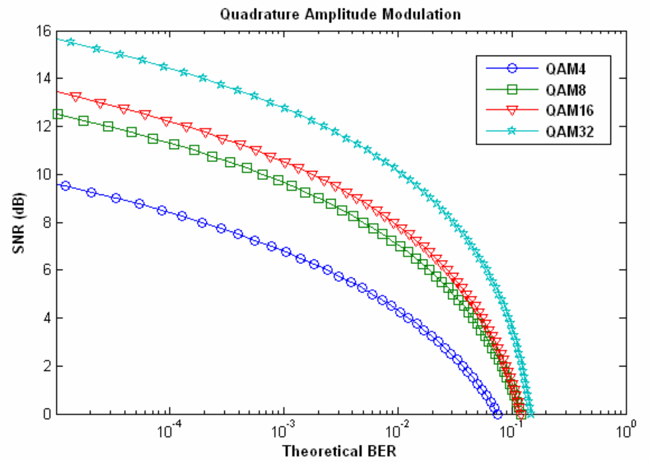

Figure 5. Theoretical BER vs SNR of a QAM system

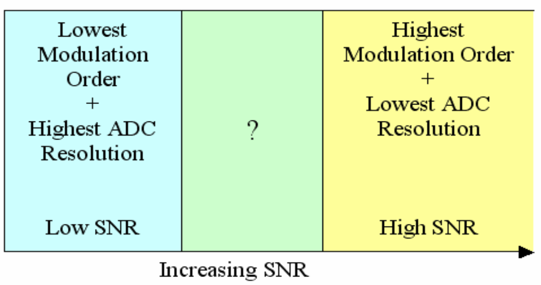

Figure 6. Receiver Configuration based on SNR

For extremely low SNR at the input to the receiver, the ADC would be operated in the highest resolution possible in order to maintain the best signal quality. Also the lowest modulation order would be selected since it is has the highest noise immunity.

For situations with relatively high SNR, the ADC would be operated in the lowest resolution possible, in order to conserve energy, and the highest modulation order would be selected in order to maximize throughput.

The middle region is not as straight forward. The question becomes “Is it more energy efficient to use a low resolution and low modulation order, or a high resolution and a high modulation order?” and “When is the appropriate time to transition between ADC resolutions and modulation orders? The next section discusses a method to answer these questions.

5. Resolution Adaptive ADC Power Management

The Energy Delay Product is a metric used to evaluate energy saving enhancements made to a particular system. It helps differentiate between improvements that trade system performance for energy efficiency.

$$EDP = P_{average} * Delay^2 \qquad (3)$$

For these calculations a fixed transfer size of 20MB was used. The *Delay* was then calculated base on the number of samples that would be required for each modulation order. We assumed a constant sampling frequency.

The average power dissipation $P_{average}$ is based on the mode of the ADC. Since higher modulation orders require better SNR performance, the resolution of the ADC would have to be increased in order to maintain a comparable BER. This is a worst case scenario that assumes any increase in SNR will require an increase in ADC resolution. If we normalize the power dissipation of the ADC to its lowest resolution, and apply a penalty based on how much SNR performance is required, we get the following equation for flash based ADCs:

$$P_{penalty} = 2^{\lceil \Delta SNR / 6.02 \rceil} \qquad (4)$$

Note that this is derived from combining equations 1 and 2. When the ADC is in its lowest resolution the penalty is 1. Any increase in SNR up to 6.02dB would incur a penalty of 2. A SNR increase greater than 6.02 but less than 12.04 would incur a penalty of 4 and so on.

The EDP for a given configuration of ADC resolution and modulation order is then given by the following equation.

$$EDP = P_{penalty} * \# samples^2 \qquad (5)$$

The results for each digital modulation protocol are shown in tables 2 through 4.

It can be seen that in each instance, paying the penalty of increased ADC power resulted in a more energy efficient transfer. This stems from fact that when comparing the performance penalty of a one bit change in resolution, to the intrinsic SNR between each of modulation orders, 6 dB is extremely large.

Mod Order	Δ SNR	Power Penalty	Samples	EDP
PSK4	0	1	262144	6.87E+10
PSK8	3.4	2	131072	3.44E+10
PSK16	7.9	4	65536	1.72E+10
PSK32	12.8	8	32768	8.59E+09

Table 2. Simulation Results for PSK (with Gray Coding)

Order	Δ SNR	Power Penalty	Samples	EDP
QAM4	0	1	262144	6.87E+10
QAM8	2.9	2	131072	3.44E+10
QAM16	3.9	2	65536	8.59E+09
QAM32	6.1	4	32768	4.29E+09

Table 3. Simulation Results for QAM

Order	Δ SNR	Power Penalty	Samples	EDP
PAM2	0	1	524288	2.75E+11
PAM4	3.8	2	262144	1.37E+11
PAM8	8.3	4	131072	6.87E+10
PAM16	13	8	65536	3.44E+10
PAM32	18	8	32768	8.59E+09

Table 4. Simulation Results for PAM (with Gray Coding)

These results can now be used to answer our original question in section 4, about the most energy efficient configuration for the middle SNR regions in Figure 6.

Recall that at strong signal levels the receiver is configured to use the lowest resolution ADC and the transmitter/receiver combination is configured to use the highest possible modulation order. As the signal level drops, the receiver should increase the resolution of the ADC in order to maintain the highest possible modulation order. Once the input signal level drops to a level that an acceptable BER can no longer be maintained, the receiver and transmitter must coordinate a decrease in modulation order. As the input signal continues to decrease, the same is done for modulation order until finally the receiver is configured with the highest resolution ADC and the lowest modulation order selected.

The inverse of this is true for an increasing signal. First the modulation order should be increased until the highest number of bits per symbol is reached. Then the ADC resolution can be decreased while still maintaining the highest modulation order.

6. Conclusions and Future Work

In this paper, we propose an adaptive power management method for software radios, taking advantage of the resolution adaptive analog to digital converter as well as the flexibility of the modulation schemes that software radios provide. In digital communications systems, adaptive resolution ADCs can be utilized to maintain the highest level of energy efficiency over a wide range of received signal amplitudes. Using the energy delay product as the determinant metric, the following power management scheme is proposed. For decreasing signals, increase the ADC resolution until a tolerable BER can no longer be attained. Then begin decreasing the modulation order to take advantage of the lower orders higher noise immunity. For increasing signals, maintain the ADC in the highest resolution possible until the maximum modulation order is achieved. Then begin reducing the ADC resolution as it can be done without affecting the modulation order.

Our analysis has some limitation. The MATLAB simulations did not take into account the processing power of the DSP for encoding and decoding the different digital communication protocols. Also this analysis only looks at the BER performance inherent to the modulation schemes. Other components in the system, such as the amplifiers may induce higher distortions to the higher order modulation schemes than they did to the low order modulation schemes. Effects such as this would cause greater separation in SNR dependence between the high order modulation and low order modulation protocols. This may change the results of the simulation. Also in these simulations, the receiver and transmitter are perfectly synchronized. There is no over sampling, symbol interference, or clock jitter. In all simulations a AWGN channel was used to perturb the transmitted signal using MATLAB's base band models. To fully weight system level trade offs, a pass band simulation would be required. Our future work will attempt to take all these factors into consideration such that a more accurate analysis is achieved.

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